Analysis and Design of Analog Integrated Circuits
Lecture 24

Bipolar Devices and Their Applications

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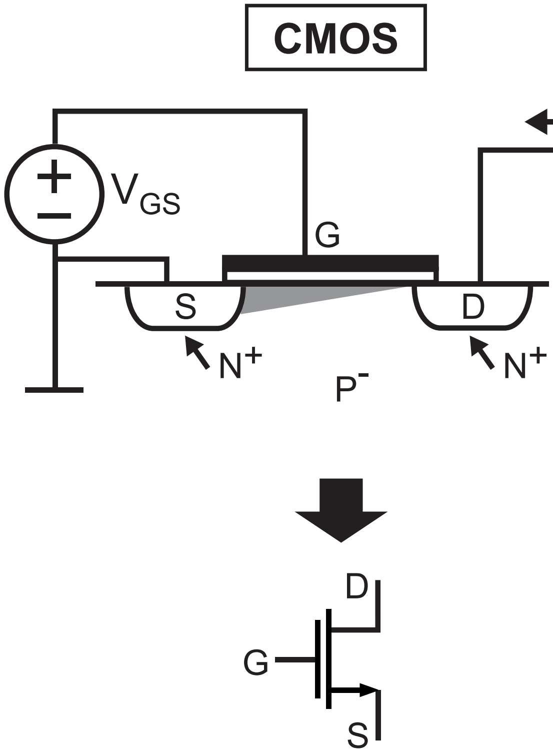
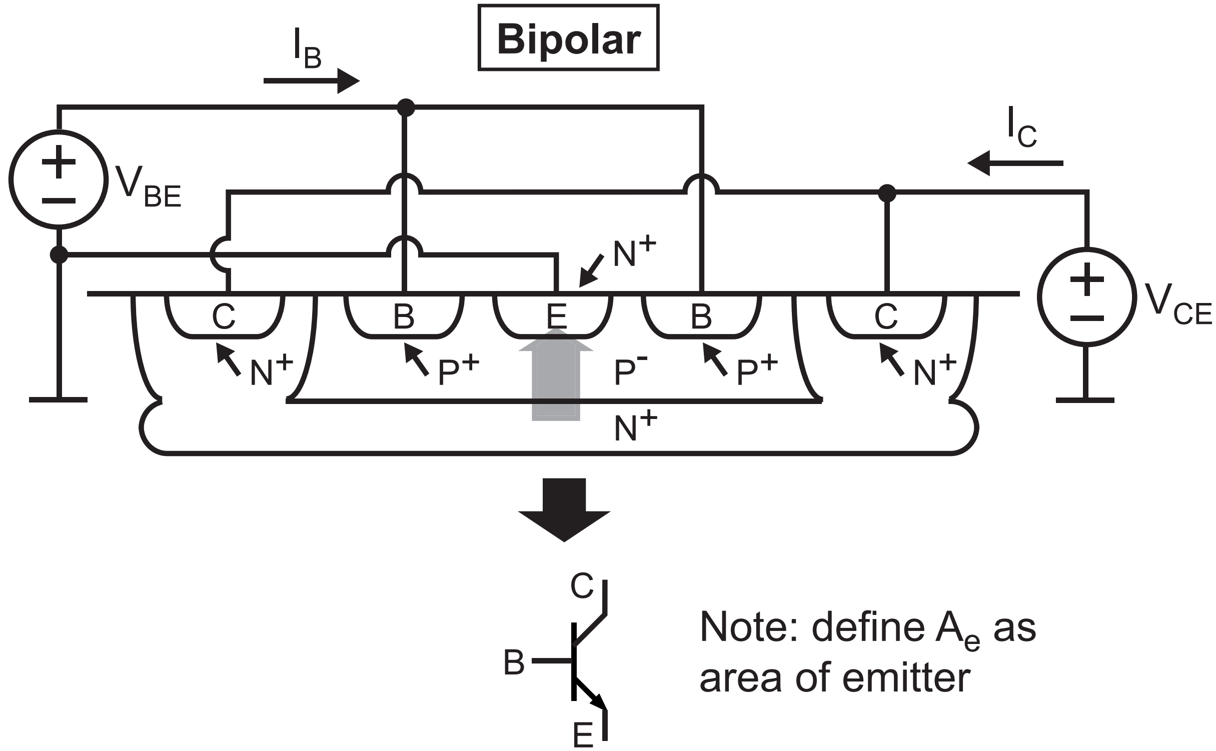
Introducing Bipolar Devices (Within CMOS Processes)



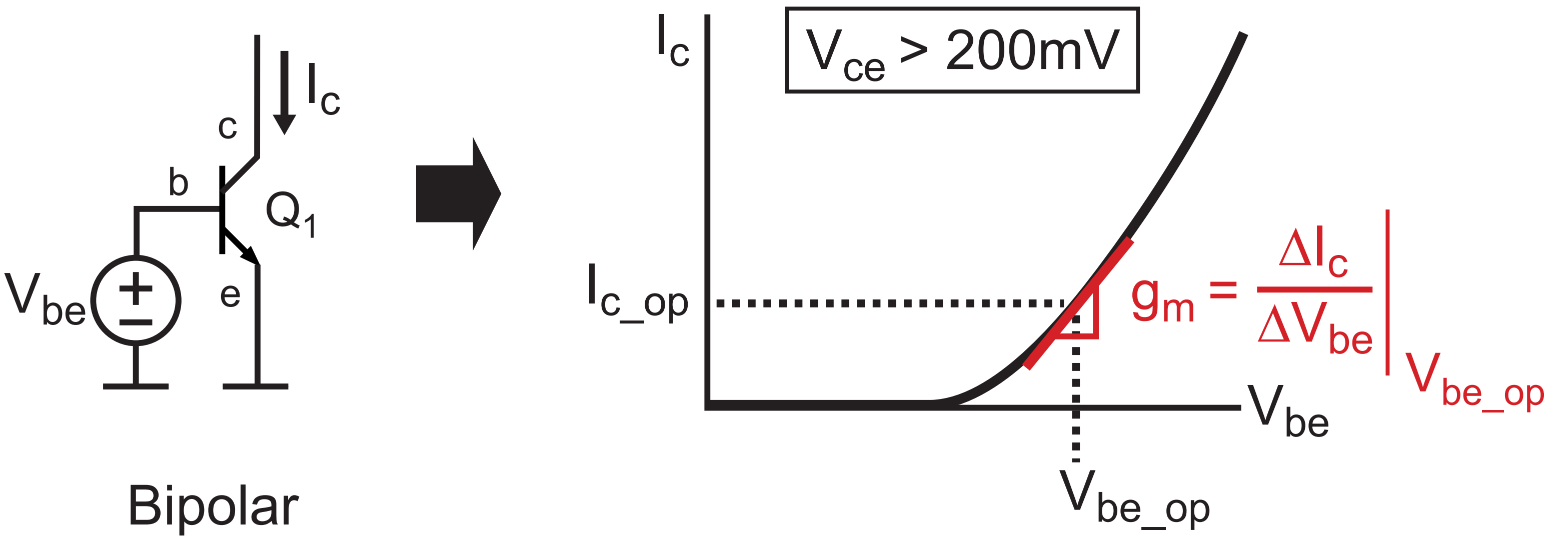


Note: define A_e as area of emitter

- **Modern CMOS processes often offer Deep NWELL**
  - **Allows a buried N+ layer to be implanted**
  - **Vertical NPN bipolar device can be achieved**

This lecture will discuss modeling and applications of such "parasitic" bipolar devices

Collector Current as a Function of V_{be}



- **For 0 < V_{ce} < 200mV, V_{be} > 0, device is in saturation**
  - **This region of operation is typically avoided**
- **For V_{ce} > 200mV, V_{be} > 0, device is in forward active mode**

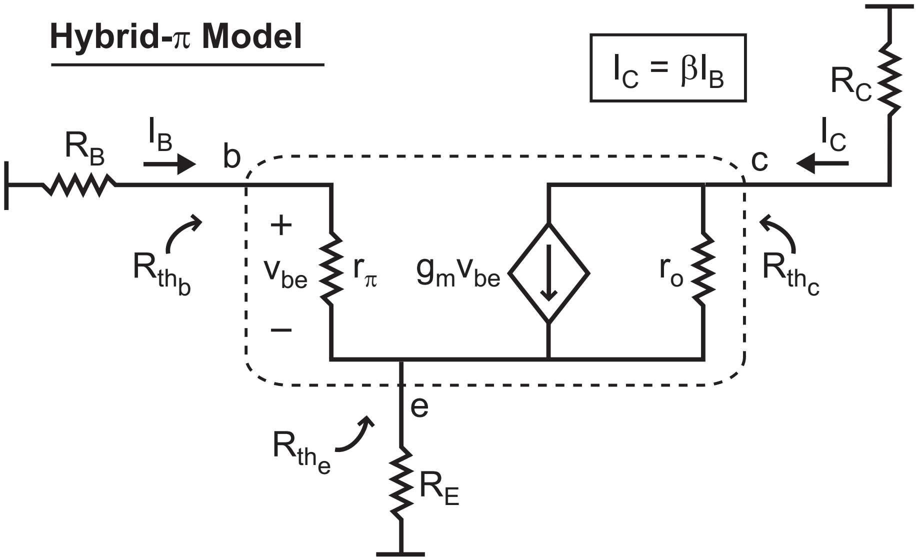
$$I_c = \beta I_b$$

$$I_c = A_e I_s (e^{V_{be}/V_t} - 1), \quad \text{where } V_t = kT/q$$

$$\Rightarrow \quad g_m = \frac{\delta I_c}{\delta V_{be}} \approx \frac{I_c}{V_T}$$

Thevenin Modeling of Bipolar Device

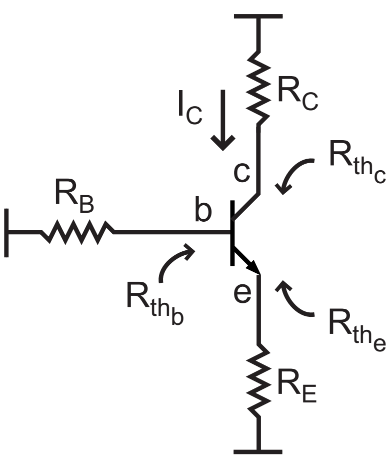
Hybrid-π Model



Key Small-Signal Parameters

Parameter	Forward Active	Definition
g_m	$\frac{I_C}{V_t}$	$V_t = \frac{kT}{q} \approx 26\text{mV at } 25^oC$
r_π	$\frac{\beta}{g_m}$	β is Current Gain
r_o	$\frac{V_A}{I_C}$	V_A is Early Voltage

Thevenin Resistances



Approximation

$R_{th_c} = r_o(1+g_m(r_\pi \| R_E))$

$(\mathbf{R_B << r_\pi, R_B << R_E})$

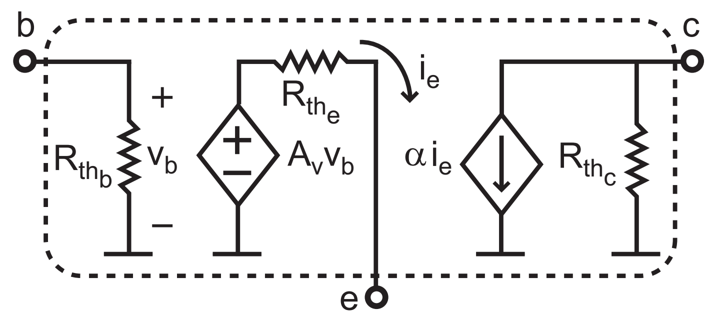
$R_{th_b} = r_\pi + (\beta+1)R_E$

$(\mathbf{R_C << r_o, R_E << r_o})$

$R_{th_e} = \frac{1}{g_m} + \frac{R_B}{1+\beta}$

$(\mathbf{R_B + R_C << \beta r_o})$

Proposed Small Signal Transistor Model



Exact

$A_v = \frac{1}{1+(1+R_C)/(r_\pi+\beta r_o)}$

$\alpha = \frac{\beta}{\beta+1}(1+R_C/R_{th_c})$

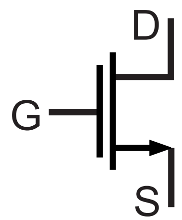
Approximation

$A_v = 1 \ (\mathbf{R_C << \beta r_o})$

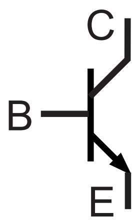
$\alpha = 1 \ (\mathbf{R_C << R_{th_c}})$

Bipolar Versus CMOS Devices

CMOS



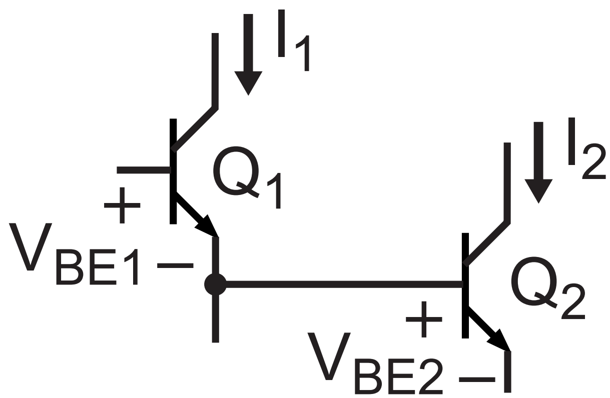
Bipolar



- **Bipolar has higher g_m for a given amount of current**
  - **Useful for high speed applications**
- **Bipolar has lower 1/f noise and lower offset issues**
  - **Useful for high precision analog**
- **Bipolar has well defined behavior over a wide operating range: $I_c = A_e I_s(e^{Vbe/Vt}-1)$**
- **Exponential behavior allows analog multipliers and dividers to be realized using translinear principle**

**CMOS is the preferred device for low cost,
high density, and high complexity digital circuits**

Consider Adding V_{BE} Voltages



- **In general**

$$I_c = A_e I_s \left(e^{V_{BE}/V_t} - 1\right) \approx A_e I_s e^{V_{BE}/V_t}$$

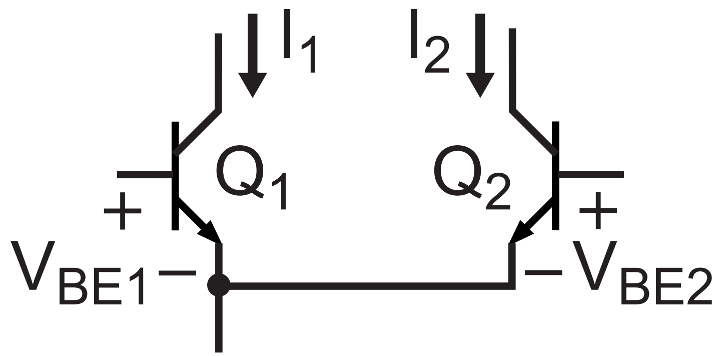
$$\Rightarrow \quad V_{BE} \approx V_t \ln\left(\frac{I_c}{A_e I_s}\right)$$

- **Addition of V_{BE} voltages corresponds to *multiplication* of collector currents**

$$V_{BE1} + V_{BE2} = V_t \ln\left(\frac{I_1}{A_{e1} I_s}\right) + V_t \ln\left(\frac{I_2}{A_{e2} I_s}\right)$$

$$= V_t \ln\left(\frac{I_1 I_2}{A_{e1} A_{e2} I_s^2}\right)$$

Consider Subtracting V_{BE} Voltages



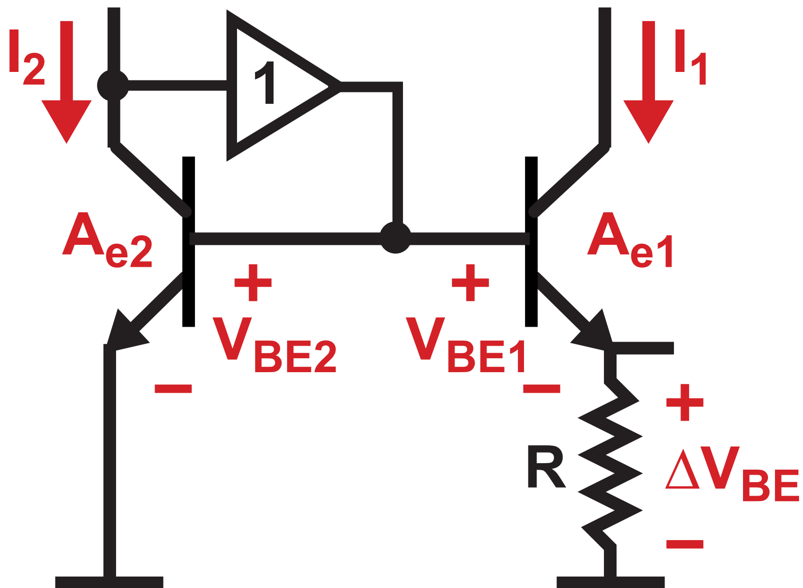
- **Subtraction of V_{BE} voltages corresponds to *division* of collector currents**

$$-V_{BE1} + V_{BE2} = -V_t \ln\left(\frac{I_1}{A_{e1} I_s}\right) + V_t \ln\left(\frac{I_2}{A_{e2} I_s}\right)$$

$$= V_t \ln\left(\frac{I_2}{I_1}\frac{A_{e1}}{A_{e2}}\right)$$

Translinear circuits can be built which achieve multiplication, division, and power-law relationships (see: http://en.wikipedia.org/wiki/Translinear_circuit)

A Closer Look at Subtracting V_{BE} Voltages



- **Subtract V_{BE} of bipolar devices**
  - Different emitter areas/currents

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = V_t \ln\left(\frac{I_2}{I_1} \cdot \frac{A_{e1}}{A_{e2}}\right)$$

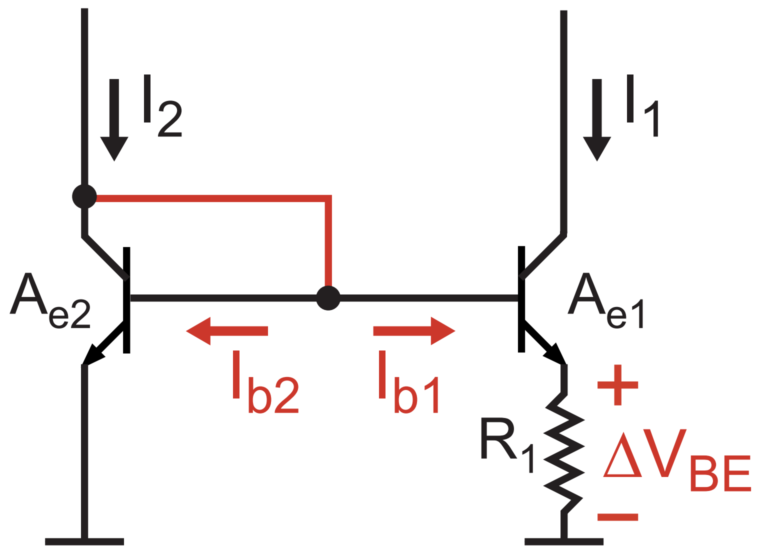
$$= \frac{kT}{q} \ln\left(\frac{I_2}{I_1} \cdot \frac{A_{e1}}{A_{e2}}\right)$$

- **Assume ΔV_{BE} varies 0.18mV/°C**
  - **True if $(I_2/I_1)(A_{e1}/A_{e2}) \sim 10$**

- **In general, we see that ΔV_{BE} is a PTAT voltage source**
  - **PTAT : Proportional to Absolute Temperature**
- **The current through resistor *R* is also PTAT**
  - **This ignores changes in the resistance due to temperature**

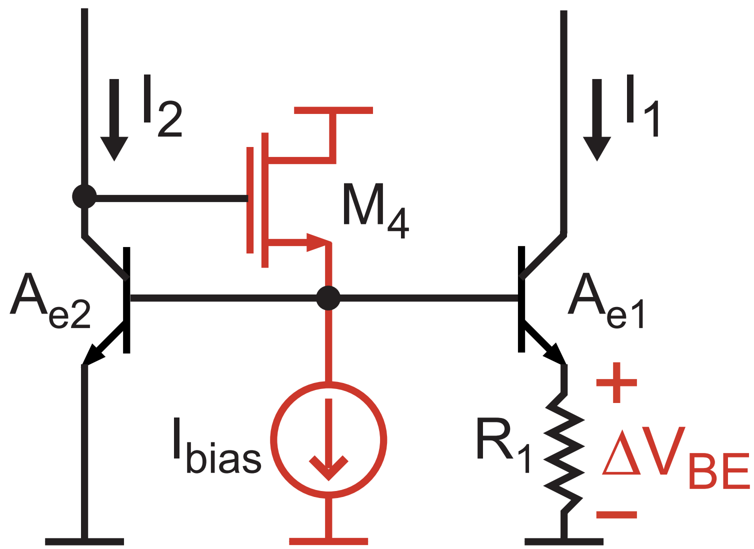
Implementation Details of PTAT Current Source

- **Let us walk through various issues and circuit approaches for realizing our PTAT current source**



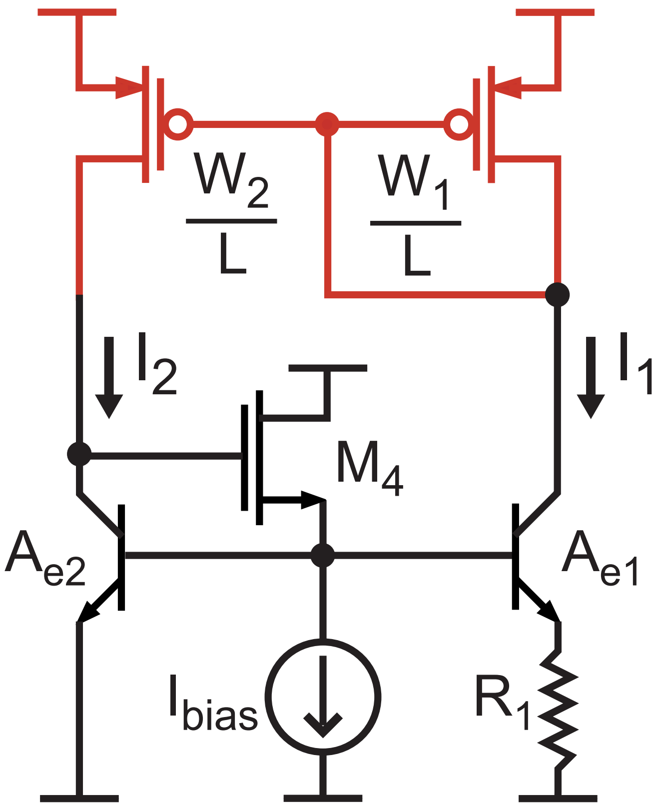
- **Simple diode connection leads to $I_{c2} \neq I_2$**
  - **This leads to $I_{c2} = I_2 - I_{b2} - I_{b1}$**
  - **But, we want $I_{c2} = I_2$ so that $I_2 \approx A_{e2} I_s e^{Vbe2/Vt}$**

NMOS Source Follower Mitigates Base Current Issue



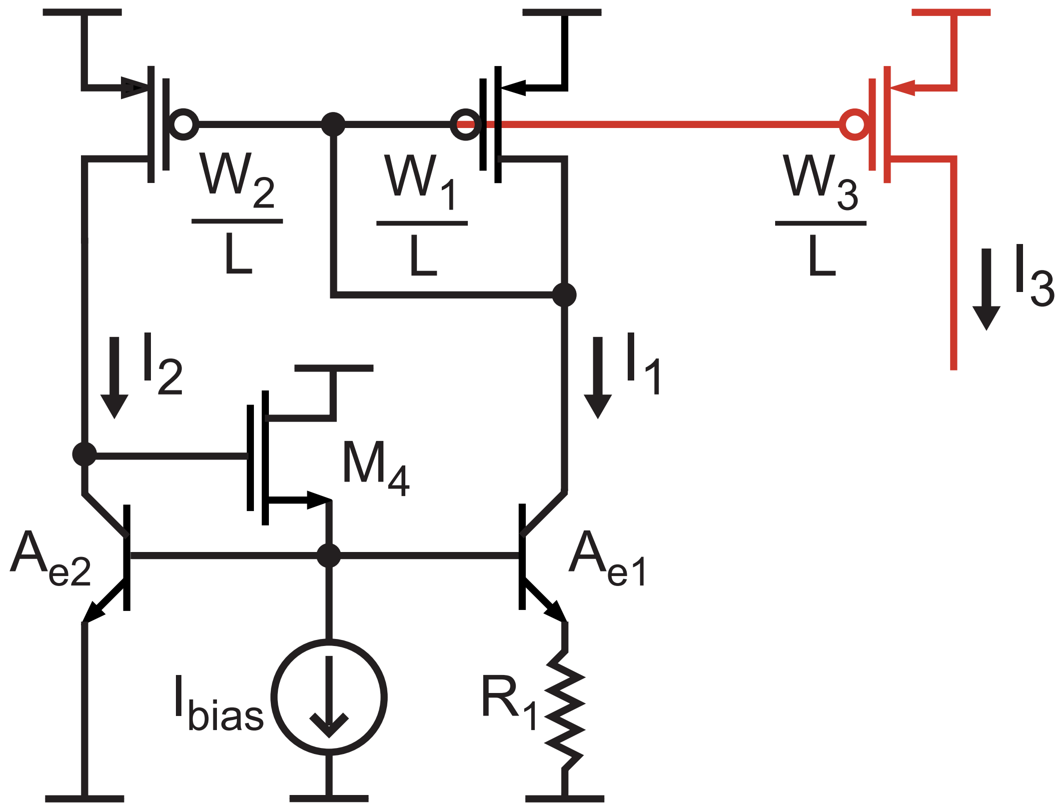
- **Simple NMOS source follower allows us to supply base current without corrupting I_2**
  - **If available in the fabrication process, use a Native NMOS device which has $V_{TH} \approx 0$**
    - Leads to improved headroom (lower V_{DD} possible)

Ratioed Currents Achieved with Current Mirror



- **We can scale I_2 relative to I_1 by proper choice of W_2/W_1**
  - **Cascoding technique can be used to achieve better current ratio accuracy**

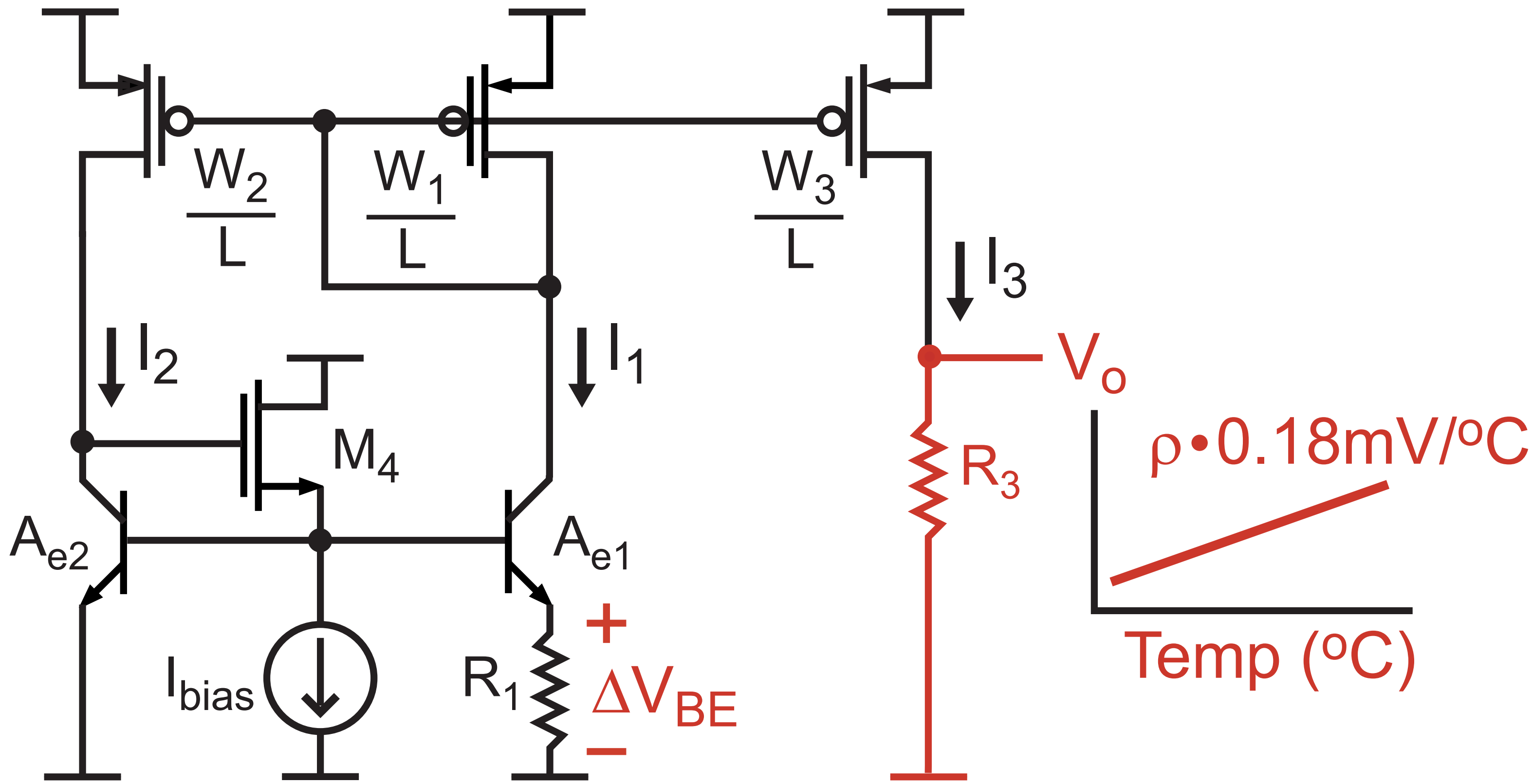
PTAT Current Output Is Simple Extension of Mirror



$$I_3 = \frac{W_3}{W_1} I_1 = \frac{W_3}{W_1}\left(\frac{\Delta V_{BE}}{R_1}\right)\frac{\beta}{\beta+1}$$

- **Issue: temperature variability of R_1 and β**
  - **R_1 is biggest concern assuming β is large**

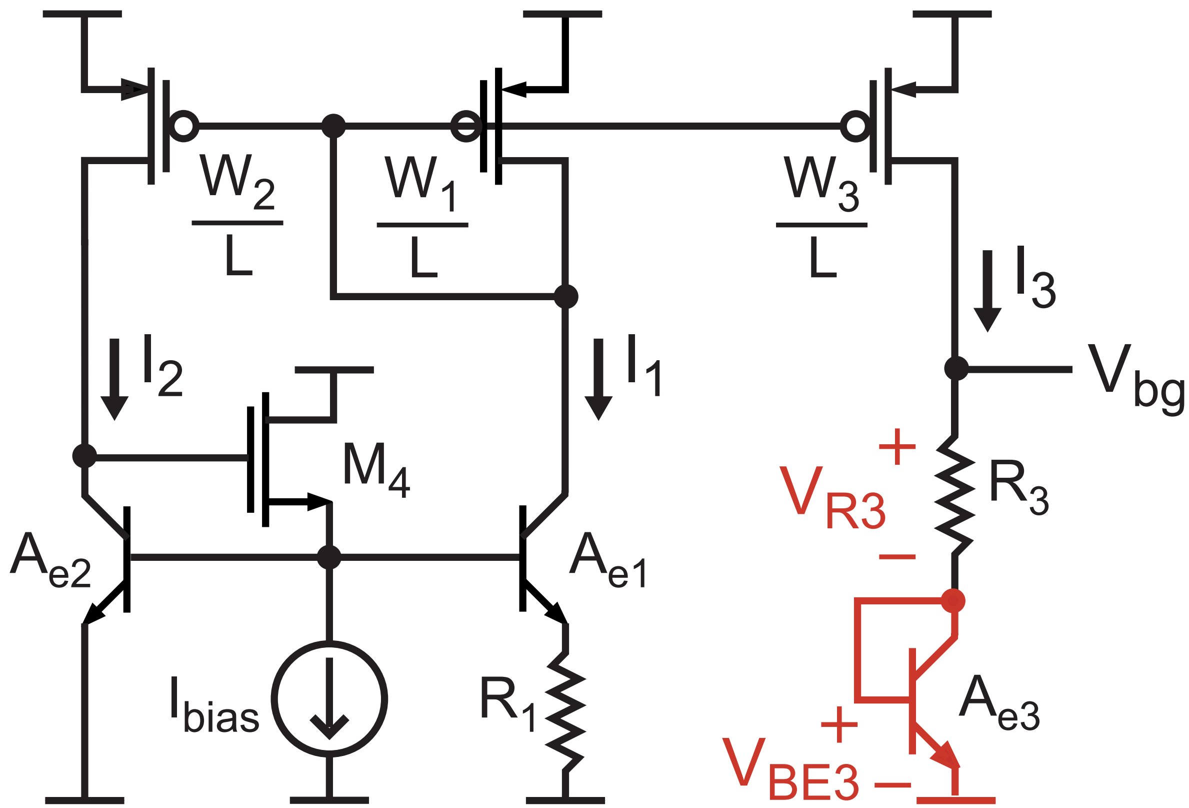
PTAT Current Output Can Be Converted to Voltage



$$V_o = I_3 R_3 = \frac{W_3}{W_1}\left(\frac{\Delta V_{BE}}{R_1}\right)\frac{\beta}{\beta+1}R_3 \;\approx\; \frac{W_3}{W_1}\frac{R_3}{R_1}\Delta V_{BE}$$

- **Output voltage set by *ratio* of resistor values R_3/R_1**
  - **Greatly reduces impact of *R* variation with temperature**

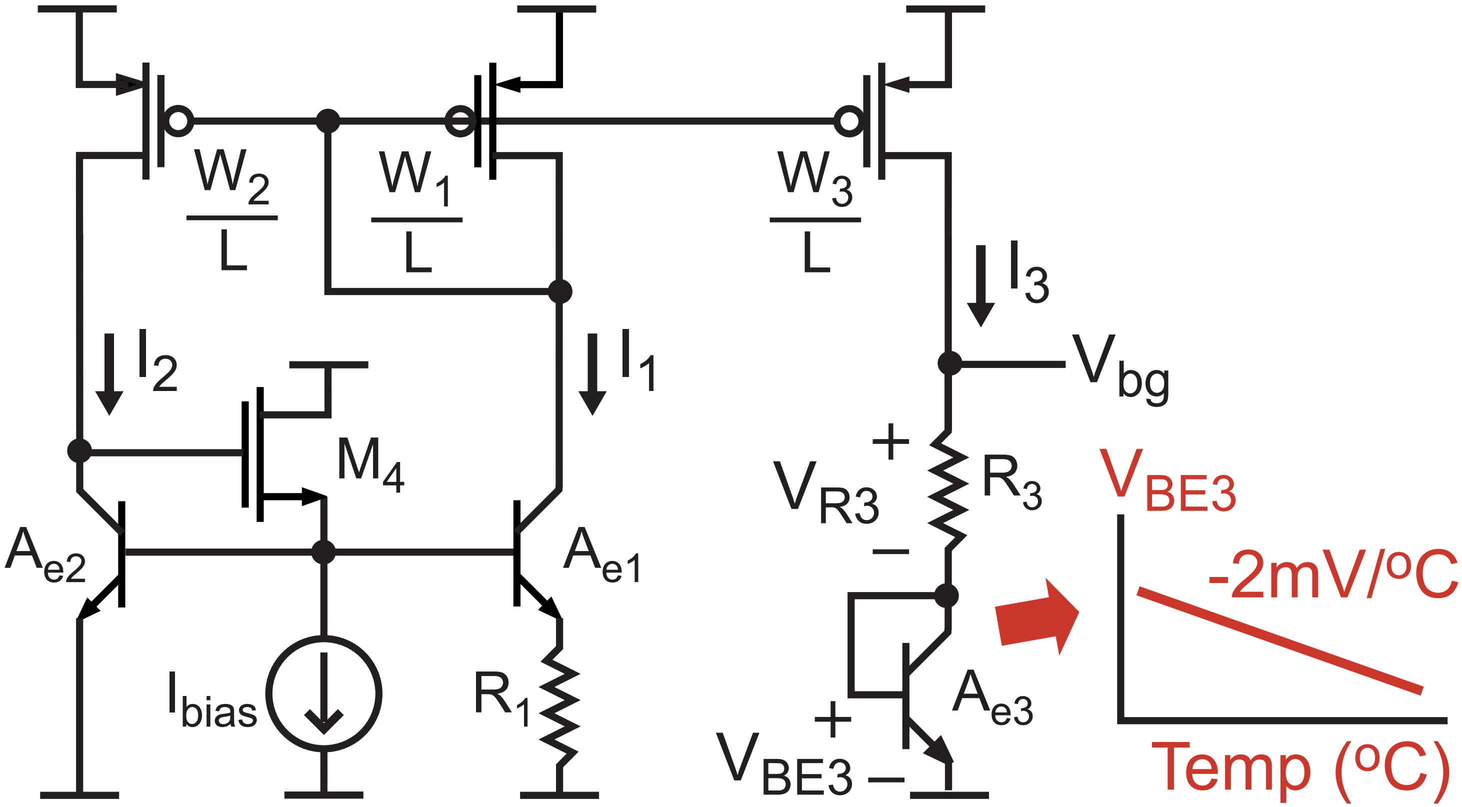
Consider Adding V_{BE} to the PTAT Voltage



$$V_{bg} = V_{R3} + V_{BE3} \approx \frac{W_3}{W_1}\frac{R_3}{R_1}\Delta V_{BE} + V_{BE3}$$

- **It turns out that this corresponds to a bandgap circuit**
  - **Proper design leads to stable V_o across temperature**

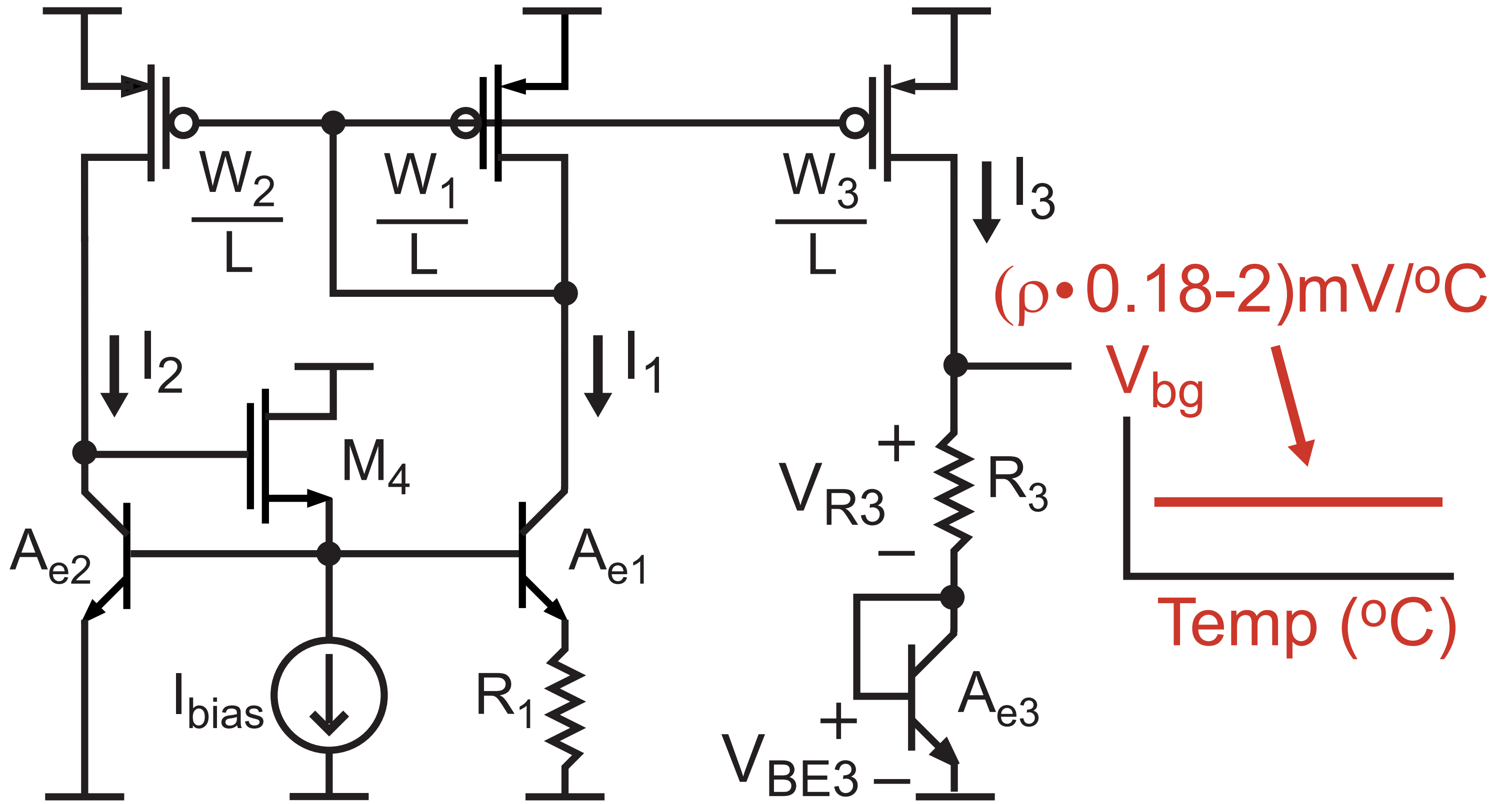
Temperature Sensitivity of V_{BE}



$$V_{bg} = V_{R3} + V_{BE3} \approx \frac{W_3}{W_1}\frac{R_3}{R_1}\Delta V_{BE} + V_{BE3}$$

- **V_{BE} has opposite temperature sensitivity as ΔV_{BE}**
  - **Recall that ΔV_{BE} is a PTAT voltage ($\approx$ +0.18mV/^{o}C)**

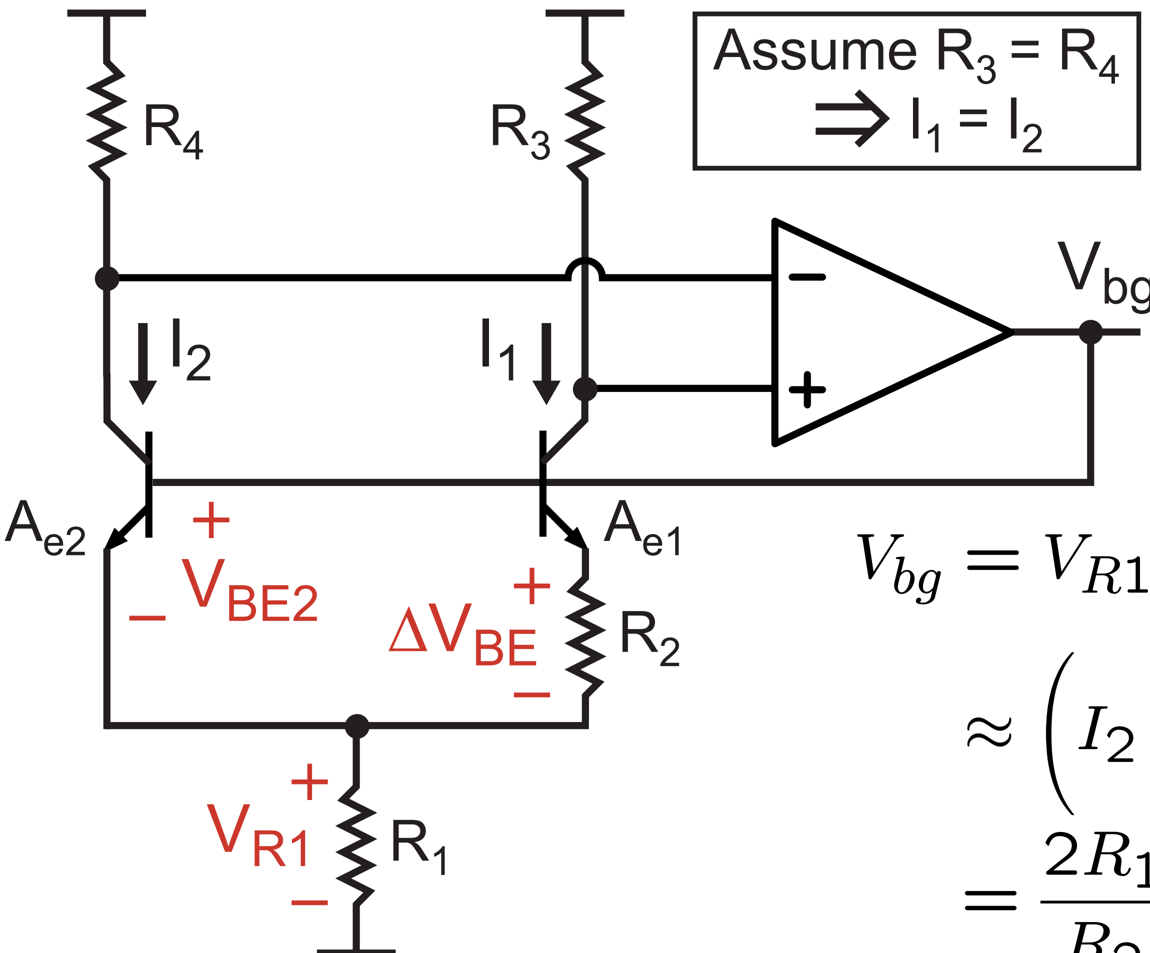
Bandgap Achieved Through Proper Scaling



$$V_{bg} = V_{R3} + V_{BE3} \approx \frac{W_3}{W_1}\frac{R_3}{R_1}\Delta V_{BE} + V_{BE3}$$

- **Set ratio as** $$\rho = \frac{W_3}{W_1}\frac{R_3}{R_1} = \frac{2mV/^\circ C}{0.18mV/^\circ C} = 11.11$$

The Brokaw Bandgap Circuit



Assume $R_3 = R_4$
$\Rightarrow I_1 = I_2$

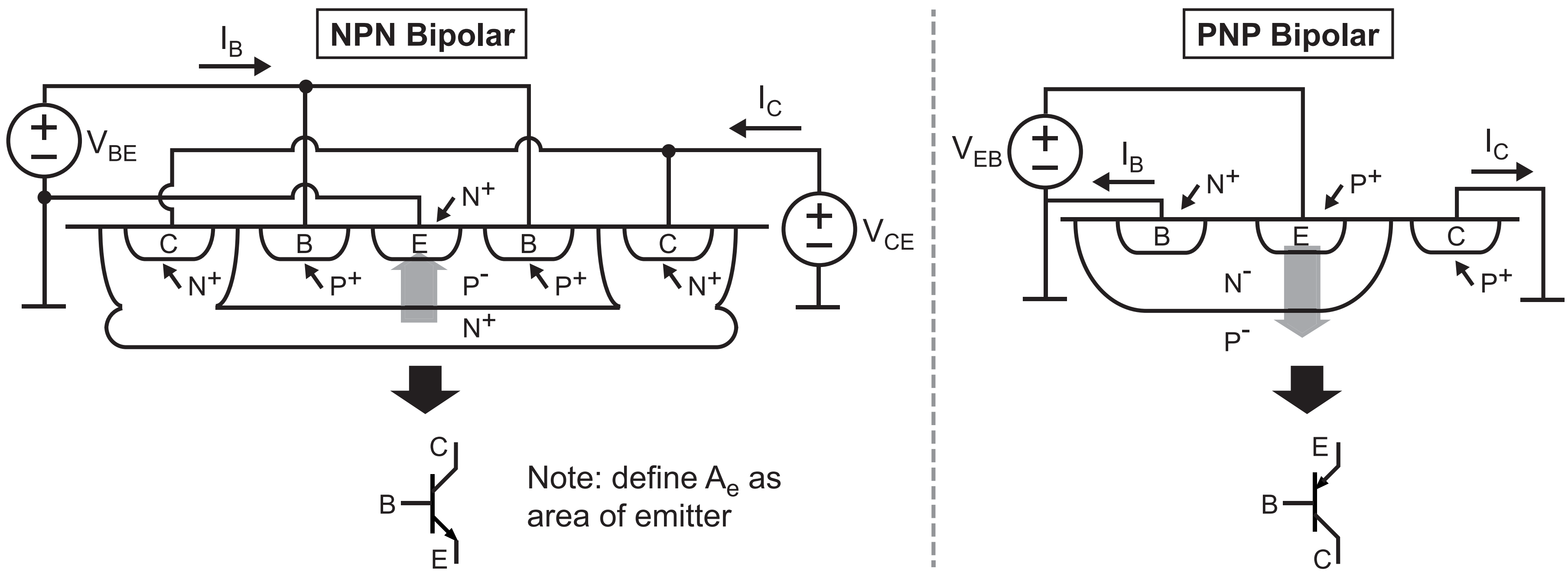
$$I_2 = I_1 \approx \frac{\Delta V_{BE}}{R_2}$$

$$\begin{aligned} V_{bg} &= V_{R1} + V_{BE2} \\ &\approx \left(I_2 + \frac{\Delta V_{BE}}{R_2}\right) R_1 + V_{BE2} \\ &= \frac{2R_1}{R_2}\Delta V_{BE} + V_{BE2} \end{aligned}$$

- **Assuming ΔV_{BE} varies at 0.18mV/ºC, set ratio as**

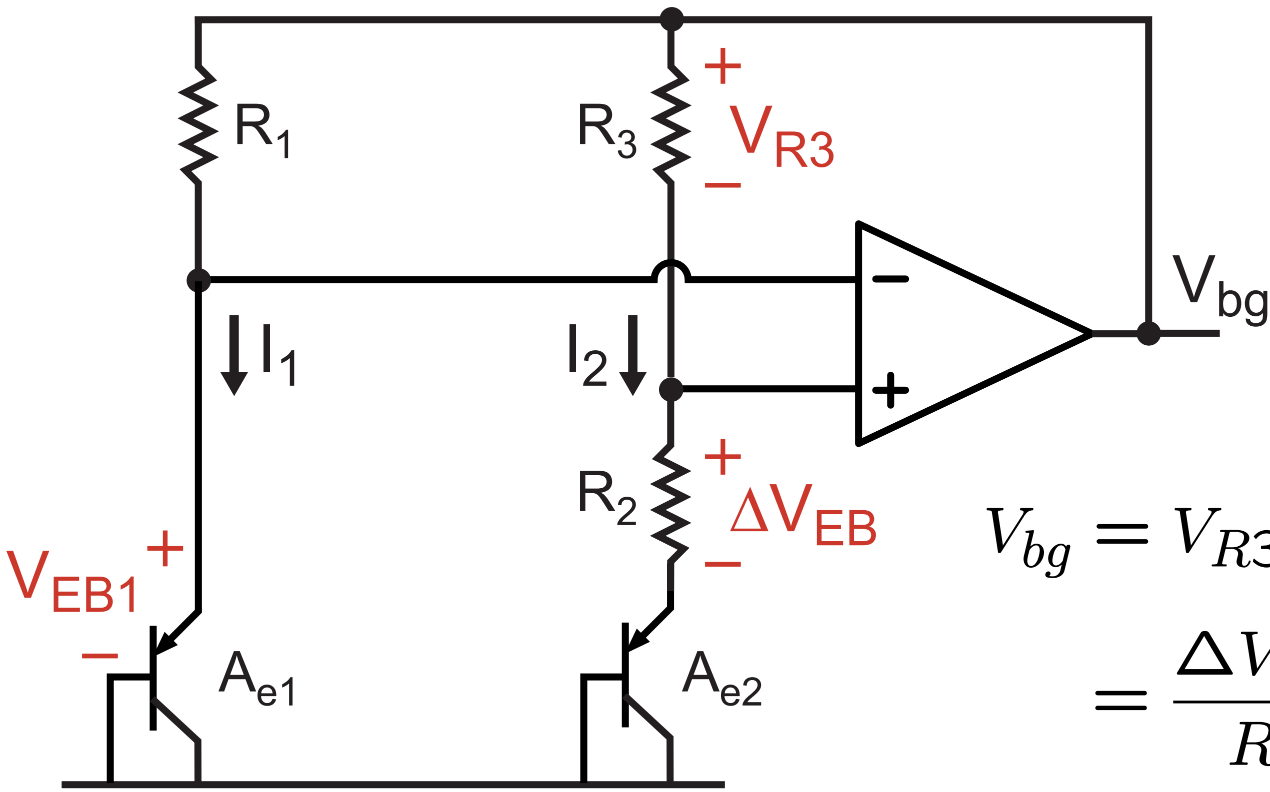
$$\frac{2R_1}{R_2} = \frac{2mV/^{\circ}C}{0.18mV/^{\circ}C} = 11.11$$

What if Deep NWELL Is Not Available?



- Deep NWELL allows an NPN device
- A PNP device is possible without Deep NWELL
  - A key constraint is that the collector must be grounded!

Grounded Collector PNP Bandgap Circuit

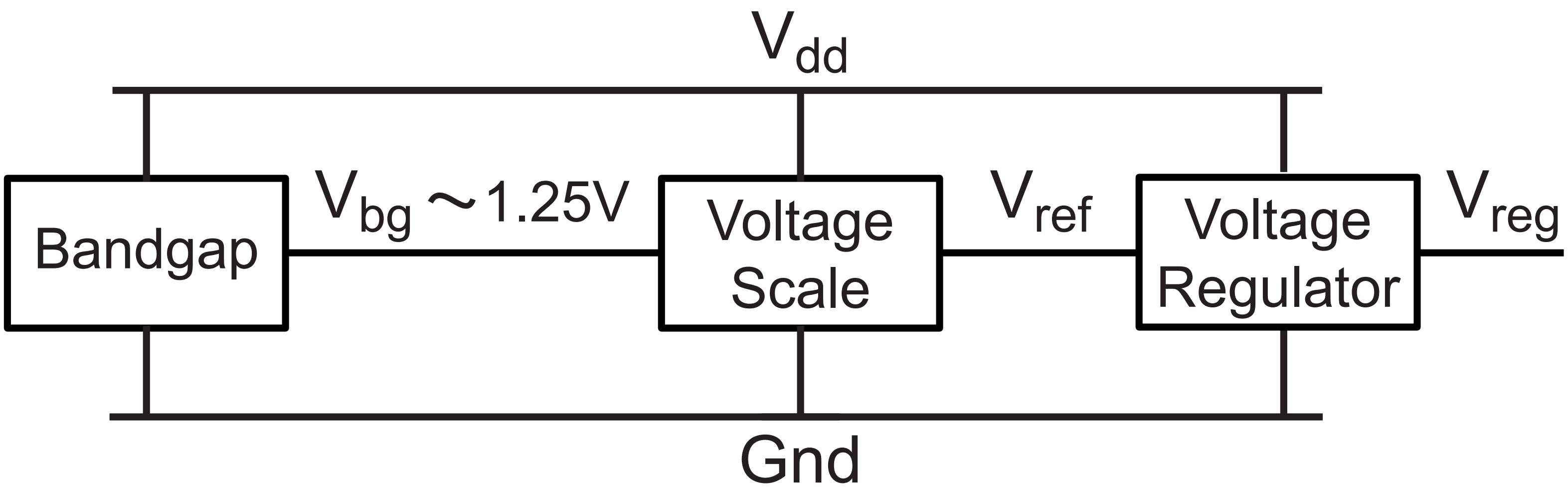


$$V_{bg} = V_{R3} + V_{EB1}$$
$$= \frac{\Delta V_{EB}}{R_2} R_3 + V_{EB1}$$
$$= \frac{R_3}{R_2} \Delta V_{EB} + V_{EB1}$$

- **Assuming ΔV_{EB} varies at 0.18mV/ºC, set ratio as**

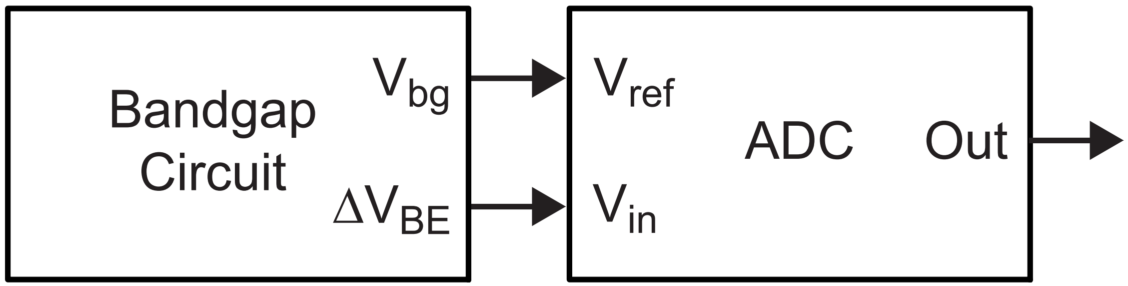
$$\frac{R_3}{R_2} = \frac{2mV/°C}{0.18mV/°C} = 11.11$$

Voltage Regulation Using a Bandgap Reference



- **Commonly used in modern integrated circuits**
  - **Rejection of power supply variation and noise**
  - **Variable voltage operation of circuits**

Temperature Sensing Using Bipolar Devices



- Recall that ΔV_{BE} is a linear function of temperature

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = \frac{kT}{q}\ln\left(\frac{I_2}{I_1}\cdot\frac{A_{e1}}{A_{e2}}\right)$$

- We can create an accurate temperature sensor by comparing ΔV_{BE} to a temperature stable bandgap reference voltage
  - Analog-to-digital converter is used to digitize the temperature signal

Summary

- CMOS processes offer parasitic bipolar devices
  - Deep NWELL option allows both NPN and PNP devices
- We can use the same analysis tools for both bipolar and CMOS devices
  - Hybrid π and Thevenin modeling techniques
- Bipolar devices have very useful properties
  - Exponential characteristic over a wide operating range
  - Higher g_m for a given current than CMOS devices
  - Lower 1/f noise and offset issues than CMOS devices
- Bipolar devices are very useful for certain circuits
  - Translinear circuits (for multiplication and division)
  - Bandgap voltage references
  - Temperature sensors