Analysis and Design of Analog Integrated Circuits
Lecture 8

Cascode Techniques

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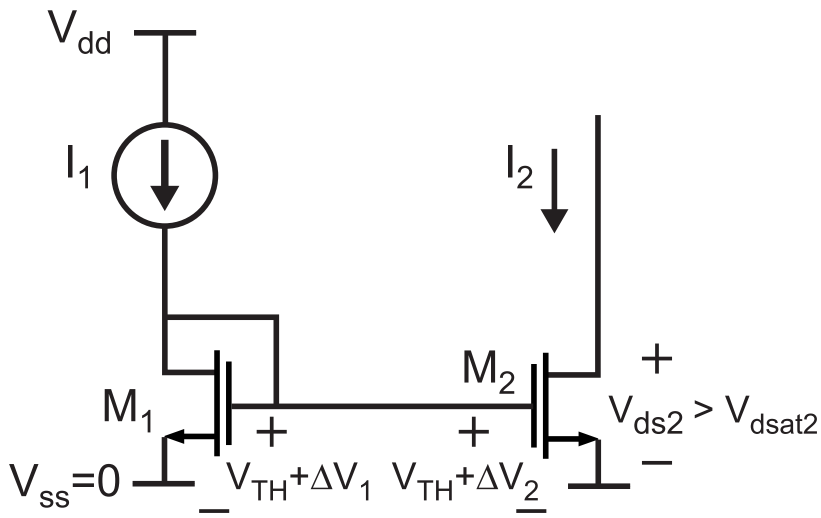
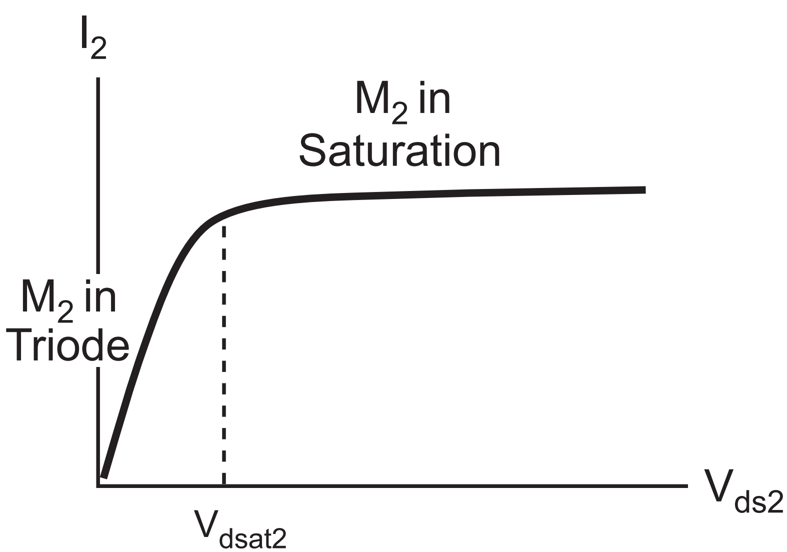
Review of Large Signal Analysis of Current Mirrors





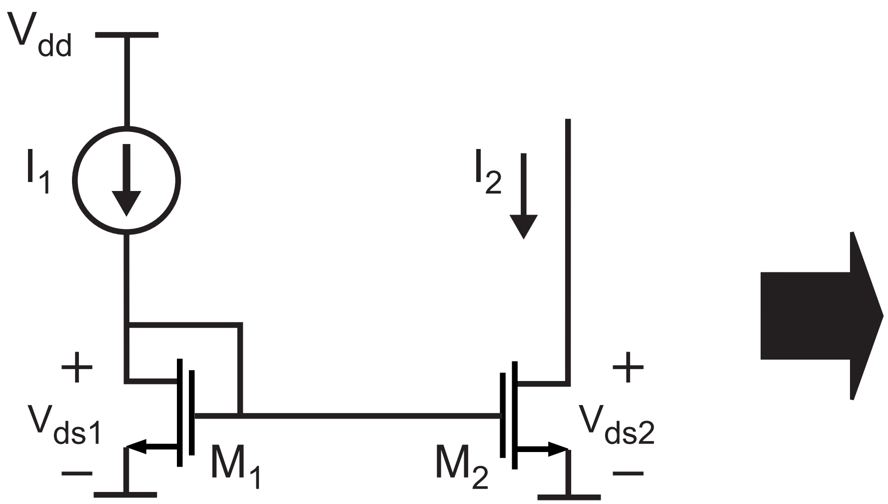
$$\frac{I_2}{I_1} = \frac{\frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2}\overbrace{(V_{GS2}-V_{TH})}^{\Delta V_2}{}^2(1+\lambda_2 V_{ds2})}{\frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1}\underbrace{(V_{GS1}-V_{TH})}_{\Delta V_1}{}^2(1+\lambda_1 V_{ds1})}$$

But, $V_{TH}+\Delta V_1 = V_{TH}+\Delta V_2$ ➡ $\Delta V_1 = \Delta V_2$

$$\Rightarrow \frac{I_2}{I_1} = \underbrace{\frac{W_2}{W_1}\frac{L_1}{L_2}}_{\text{Current setting based on geometry}}\underbrace{\frac{(1+\lambda_2 V_{ds2})}{(1+\lambda_1 V_{ds1})}}_{\text{Mismatch due to } V_{ds} \text{ difference}}$$

Note: for accurate ratio, set $L_1 = L_2$

The Issue of V_{ds} Mismatch in Current Mirrors

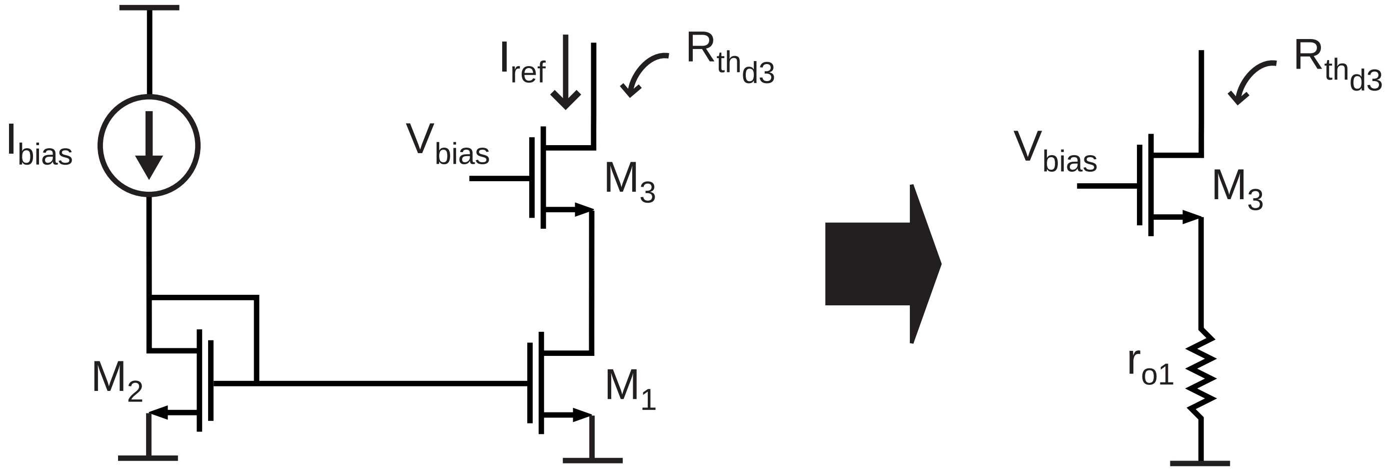


$$\frac{I_2}{I_1} = \underbrace{\frac{W_2}{W_1}}_{\text{Current setting based on geometry}} \underbrace{\frac{(1+\lambda_2 V_{ds2})}{(1+\lambda_1 V_{ds1})}}_{\text{Mismatch due to } V_{ds} \text{ difference}}$$

Note: we are assuming $L_1 = L_2$

- **Issue: Current I_2 can vary significantly as a function of the drain voltage of M_2**
  - **We often want a tightly controlled current set only by I_1 and transistor sizes**
- **How do we improve the current mirror matching performance?**

Cascoded Current Source

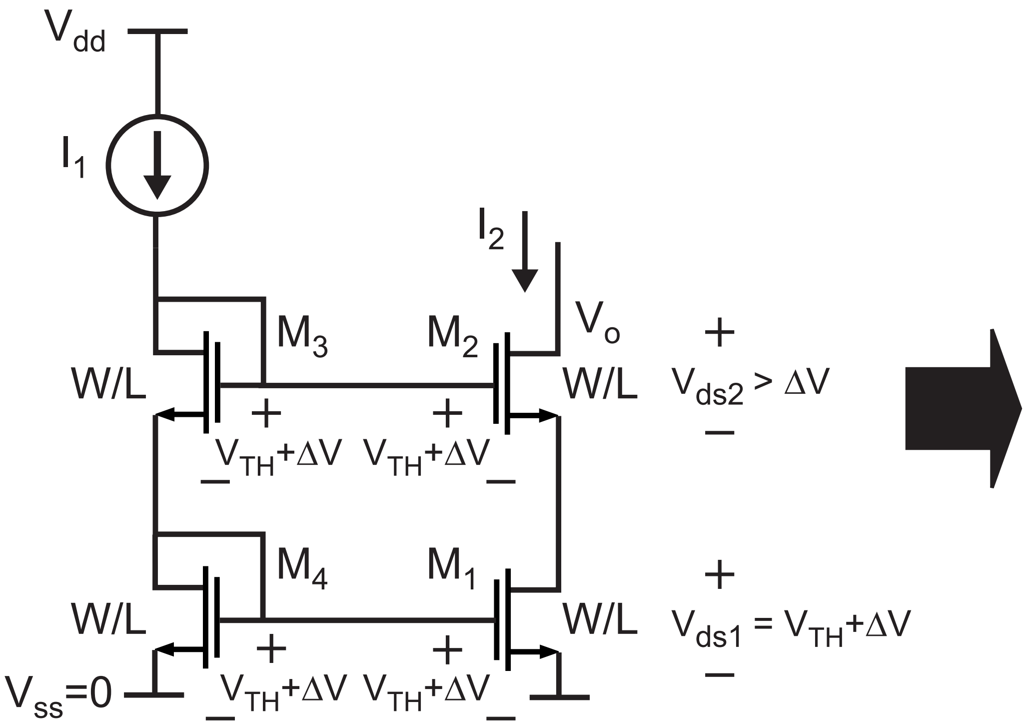


- **Offers increased output resistance**
  - **Reduces *small signal* dependence of output current on the output voltage of the current source**
  - **From Lecture 6, we derived:**

$$R_{th_{d3}} \approx r_{o3}(1+g_{m3}R_{th_{d1}}) = r_{o3}(1+g_{m3}r_{o1}) \approx (g_{m3}r_{o3})r_{o1}$$

    - Output resistance boosted by intrinsic gain of M_3, $g_{m3}r_{o3}$
- **But how do we reduce the influence of *large signal* V_{ds} mismatch between M_1 and M_2?**

Match V_{ds} of Current Mirror Devices With Proper Bias



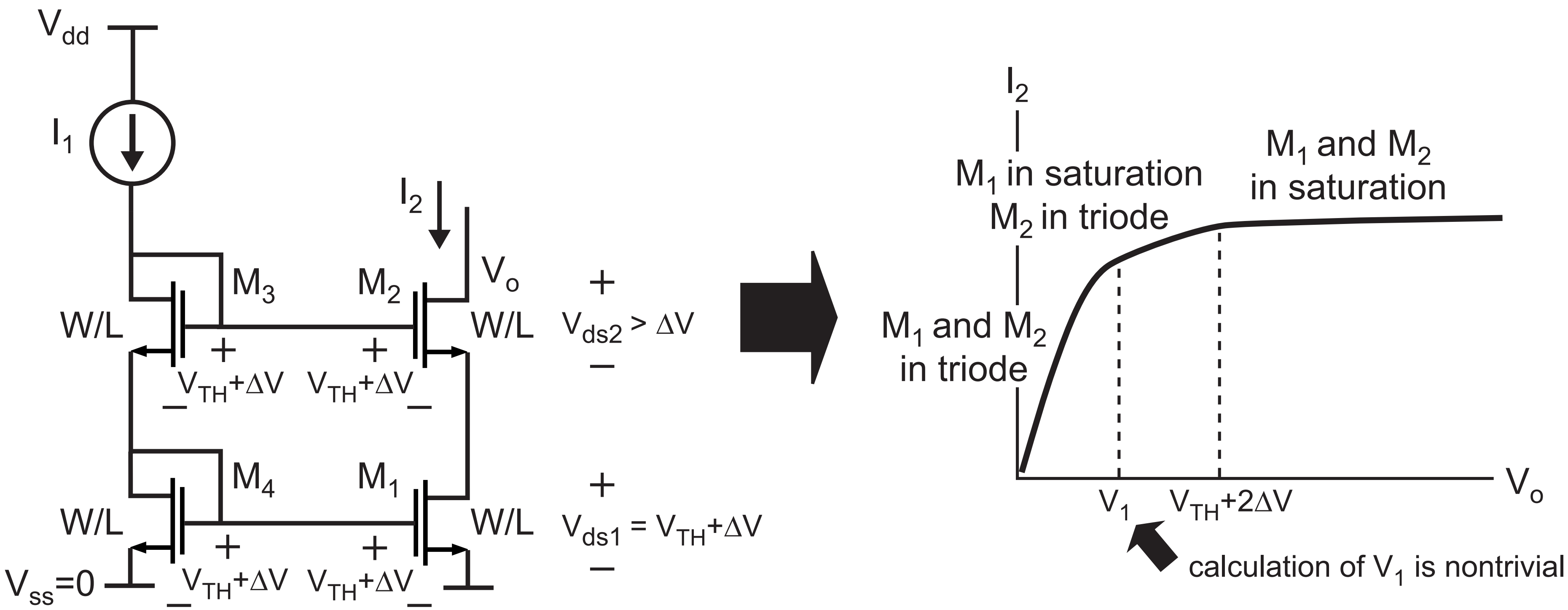
Recall: $\frac{I_2}{I_1} = \frac{W_1}{W_4}\frac{L_4}{L_1}\frac{(1+\lambda_1 V_{ds1})}{(1+\lambda_4 V_{ds4})}$

Current setting based on geometry | Mismatch due to V_{ds} difference

- **Key transistor for determining I_2 is M_1**
  - **Why is M_2 less important?**
- **Above biasing approach provides a much closer match between V_{ds1} and V_{ds4}**

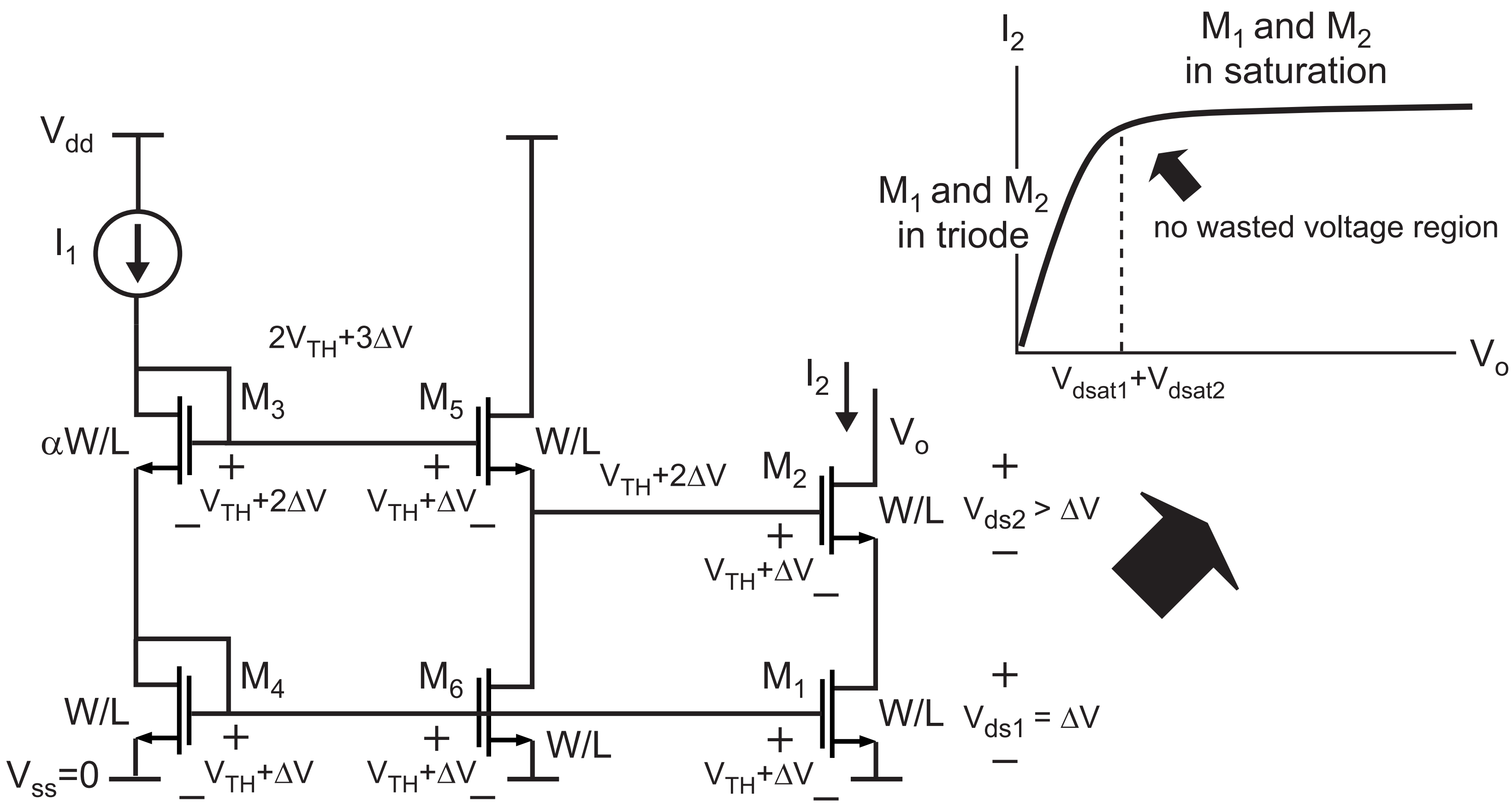
$$I_2 = \frac{W_1}{W_4}\frac{1+\lambda V_{ds1}}{1+\lambda V_{ds4}} I_1 \approx \frac{W_1}{W_4} I_1$$

The Drawback of Basic Cascode Bias Approach



- **Output voltage range is reduced**
  - **Now V_o must be > $V_{TH} + 2\Delta V$**
  - **What will happen to the output impedance of the current source if the output voltage is too low?**
  - **Can we improve the voltage range?**

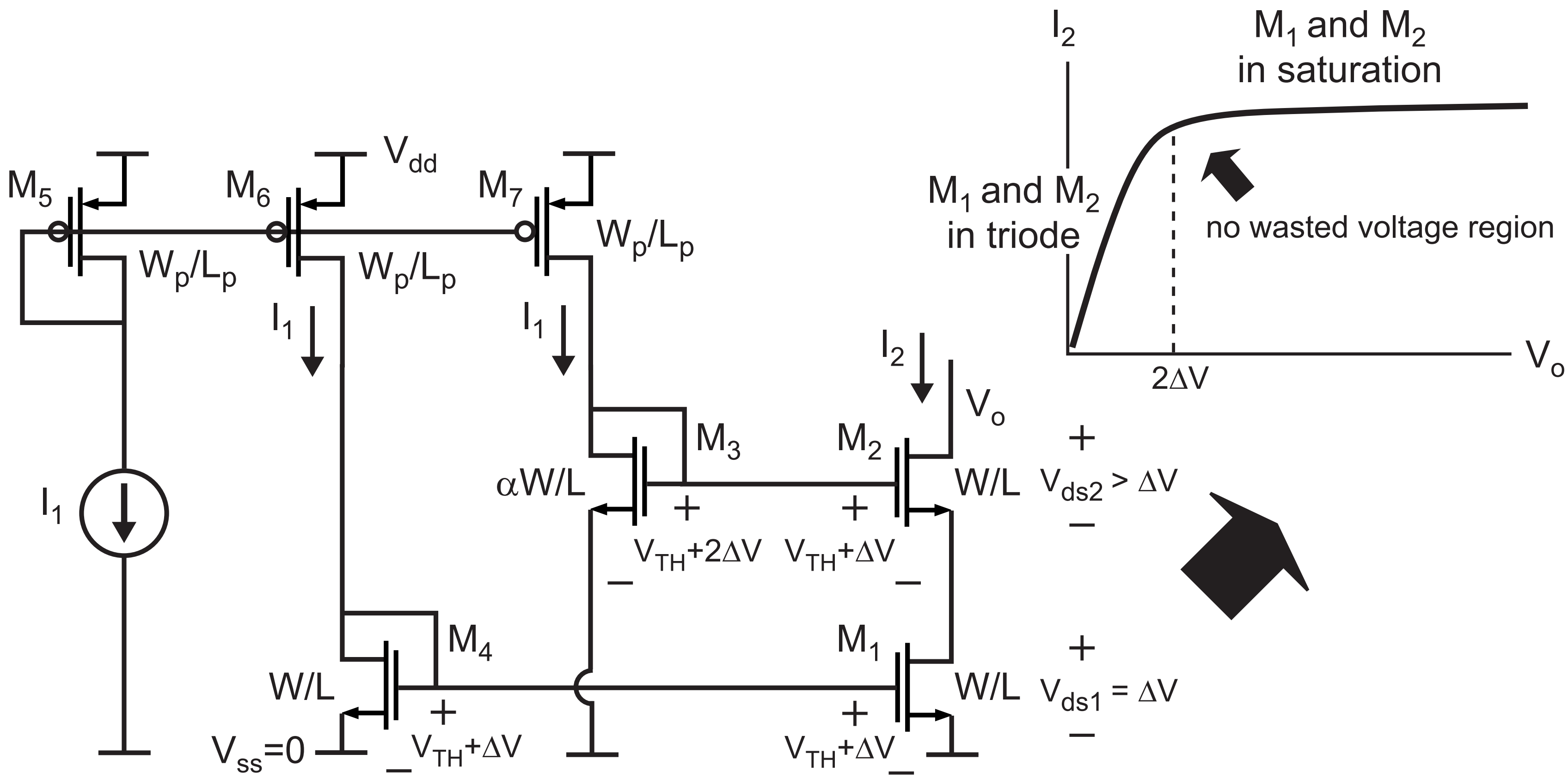
Improved Swing Cascode



- **Key idea: set size of M_3 such that $V_{ds1} = \Delta V$**
  - **Assuming strong inversion for M_1 and M_3:**

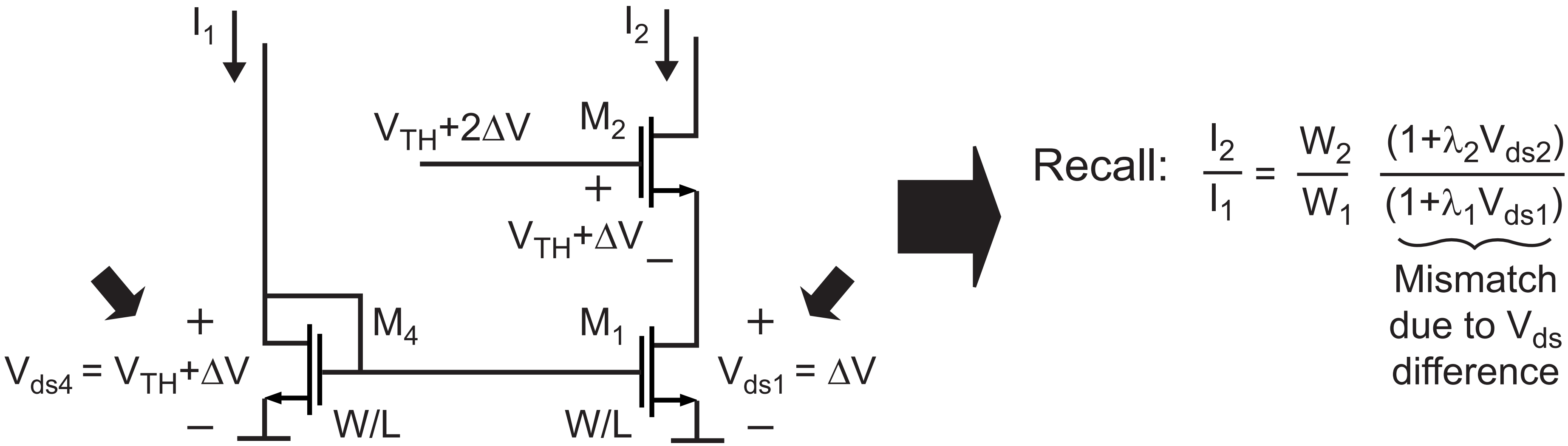
$$\Delta V = \sqrt{\frac{2 I_d L}{\mu_n C_{ox} W}} \Rightarrow \alpha = \frac{1}{4}$$

Alternative Implementation of Improved Swing Cascode



- **Set α as on previous slide**
- **Note: both implementations share a common problem**

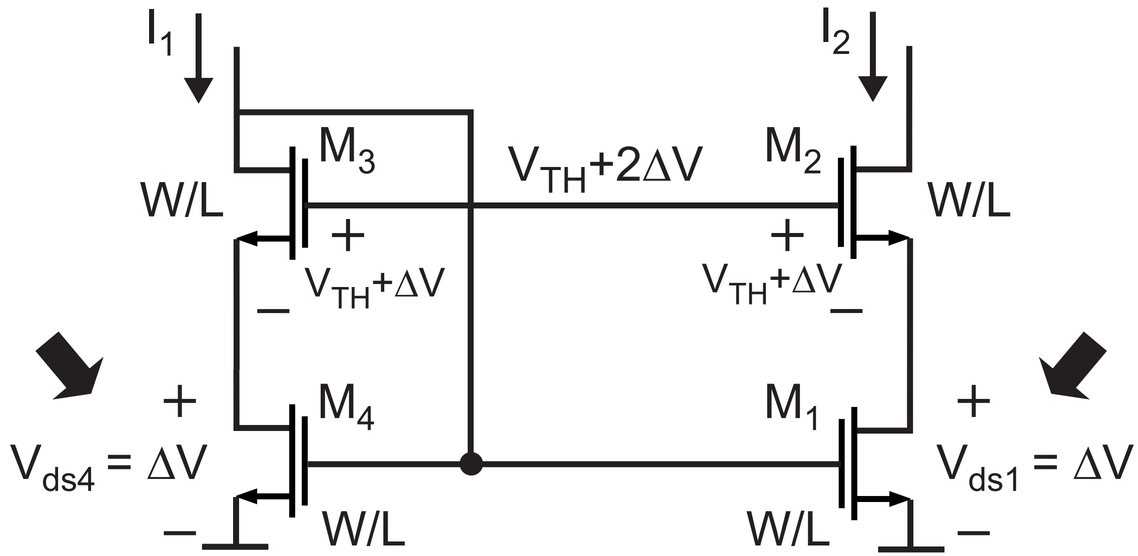
The Issue of Current Mismatch



- The improved swing approach causes a systematic mismatch between I_2 and I_1
  - Key issue: $V_{ds1} \neq V_{ds4}$

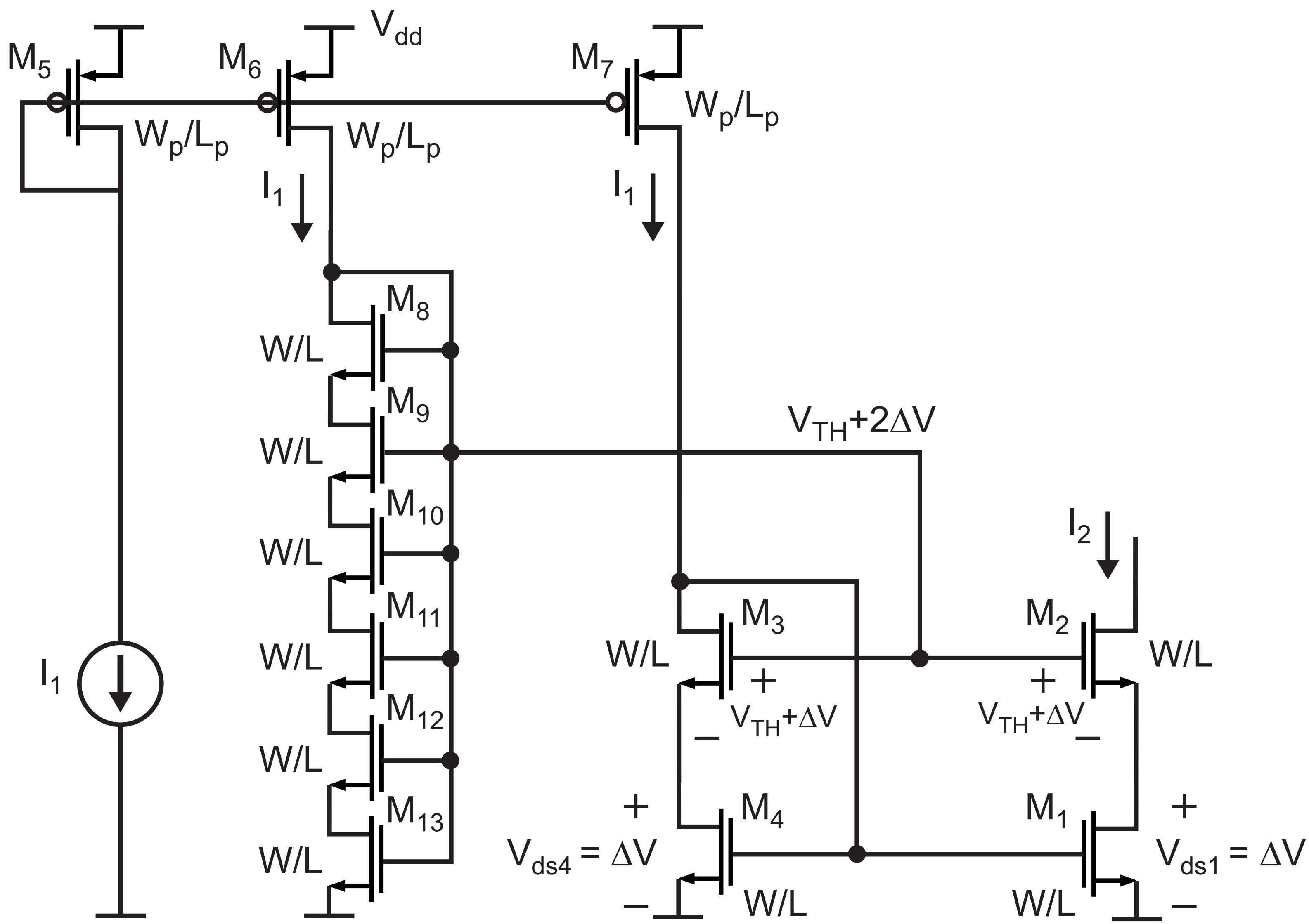
- Can we fix this problem?

Techniques to Reduce Current Mismatch



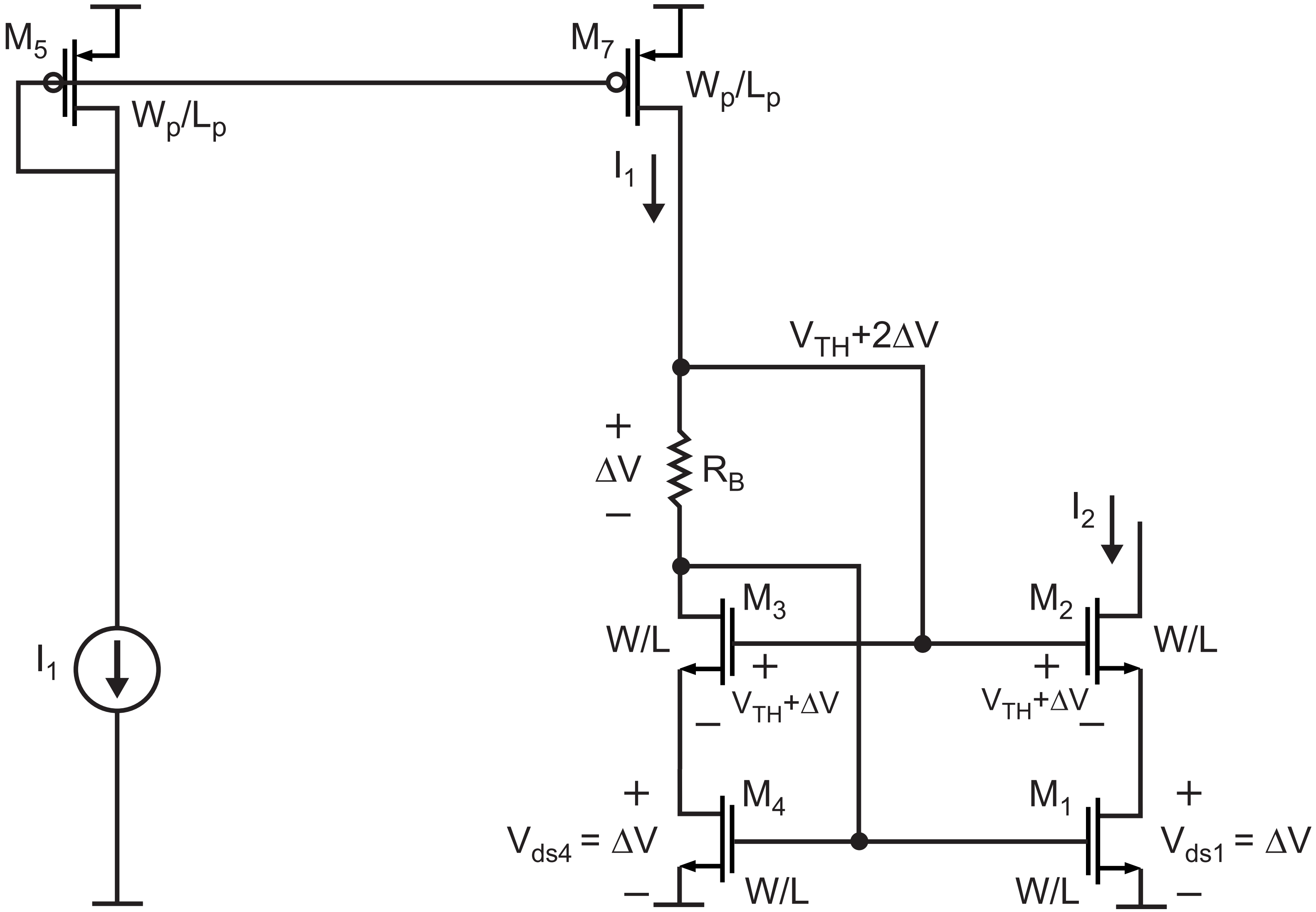
- **Systematic mismatch between I_1 and I_2 is greatly reduced by using the above circuit (now $V_{ds1} \approx V_{ds4}$)**
  - **Note that gate bias on M_2 and M_3 may be provided by previously discussed circuits**
- **Additional techniques for accurately matching I_1 and I_2**
  - **Set $L_1 = L_4 >> L_{min}$**
    - Note: set $L_2 = L_3 \approx L_{min}$ for lower area and capacitance
  - **Set $W_2/W_3 = I_2/I_1$ so that $\Delta V_2 = \Delta V_3$**

Another Common Cascode Bias Topology



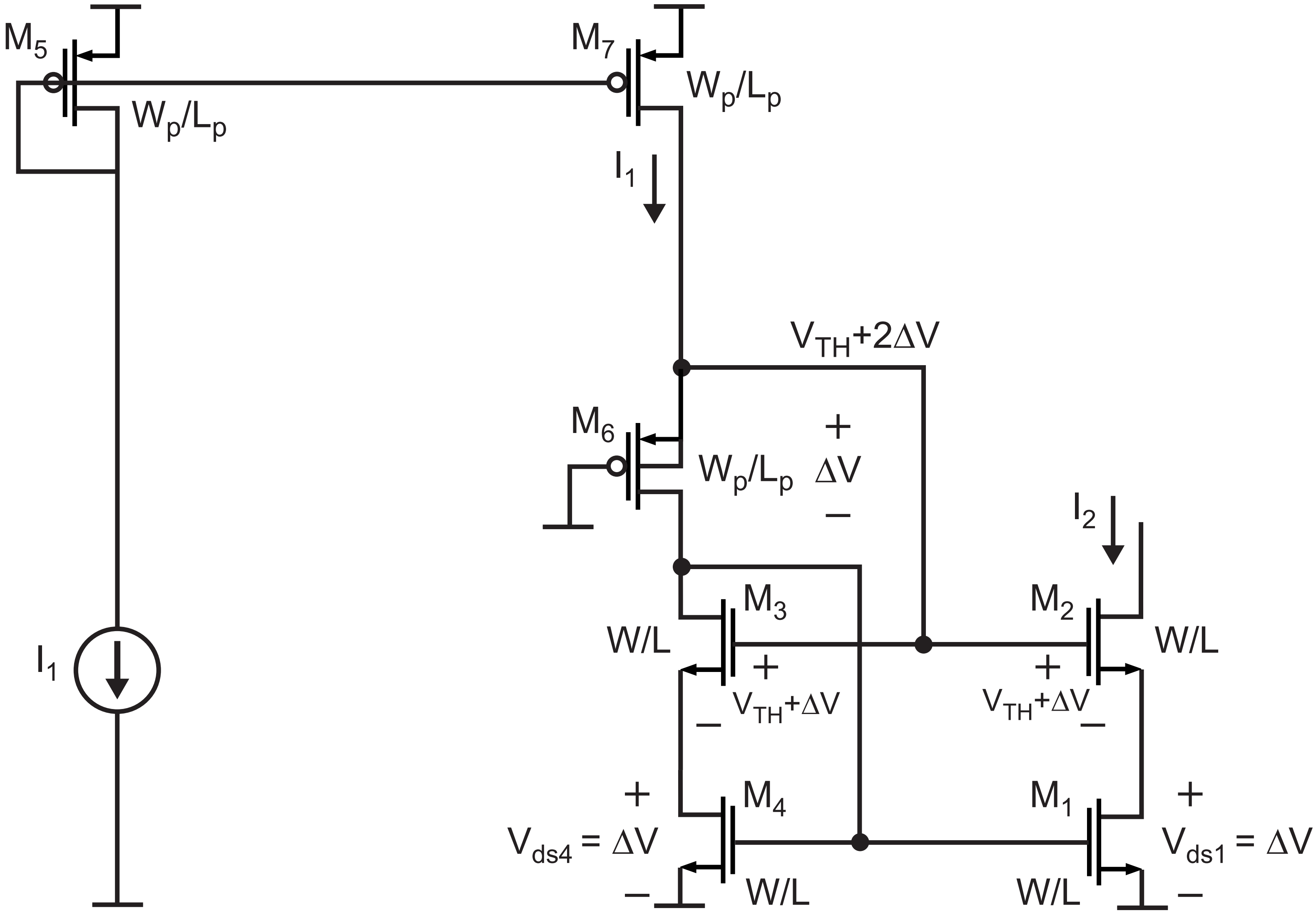
- **Key issue: needs two bias current branches**

Utilizing a Simple Resistor to Achieve One Bias Branch



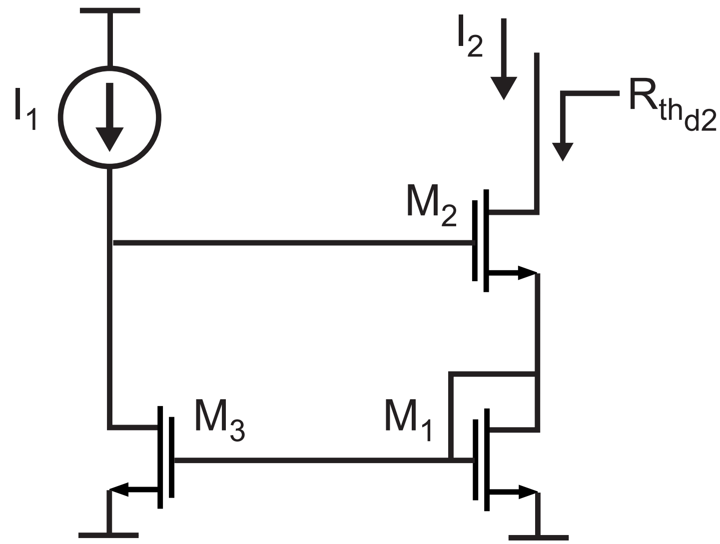
- **Issue: poly resistor is large and won't track NMOS devices across temperature and process variations**

Better Approach: Use PMOS Device In Triode Region



- **Much smaller, better tracking with NMOS devices than resistor**

Wilson Current Mirror

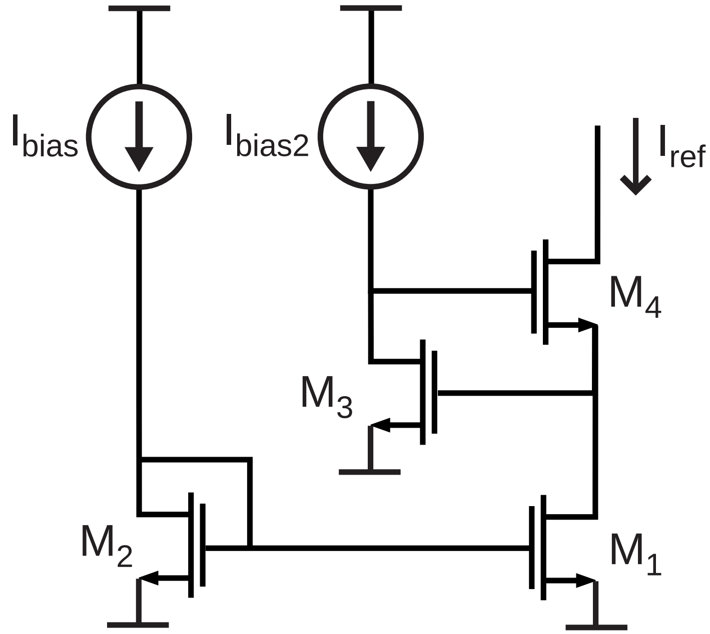


- **Relies on feedback in its operation**
- **Using Hybrid-π analysis**

$$R_{th_{d2}} \approx \frac{1}{g_{m1}}(g_{m2}r_{o2})(g_{m3}r_{o3})$$

  - **Output resistance comparable to cascode current source**
- **This circuit is rarely used these days**

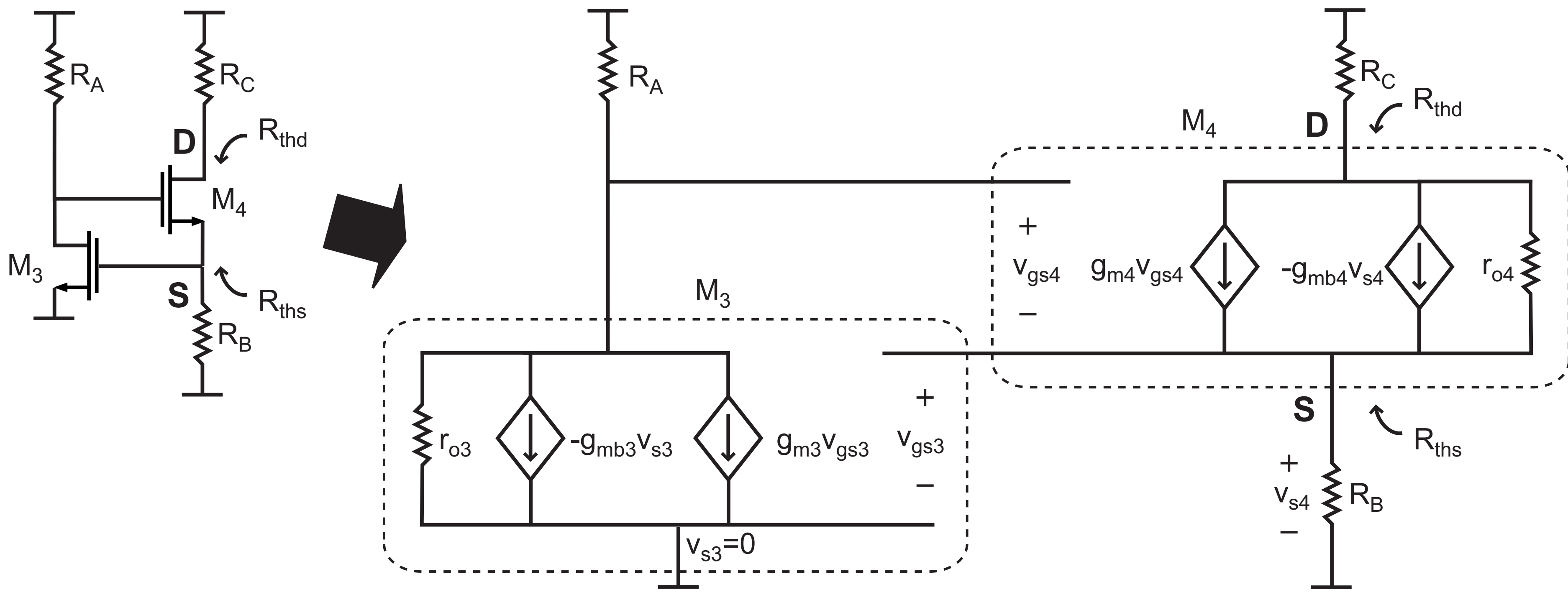
Enhanced Cascode Current Source



- **Offers output resistance comparable to double cascode current source**
- **As with Wilson mirror, analysis is tricky due to source/gate coupling**
  - **Using results shown in the following slide:**

$$R_{th_{d4}} \approx (g_{m4}r_{o4})(g_{m3}r_{o3})r_{o1}$$

Thevenin Resistances for CMOS Transistor Feedback Pair



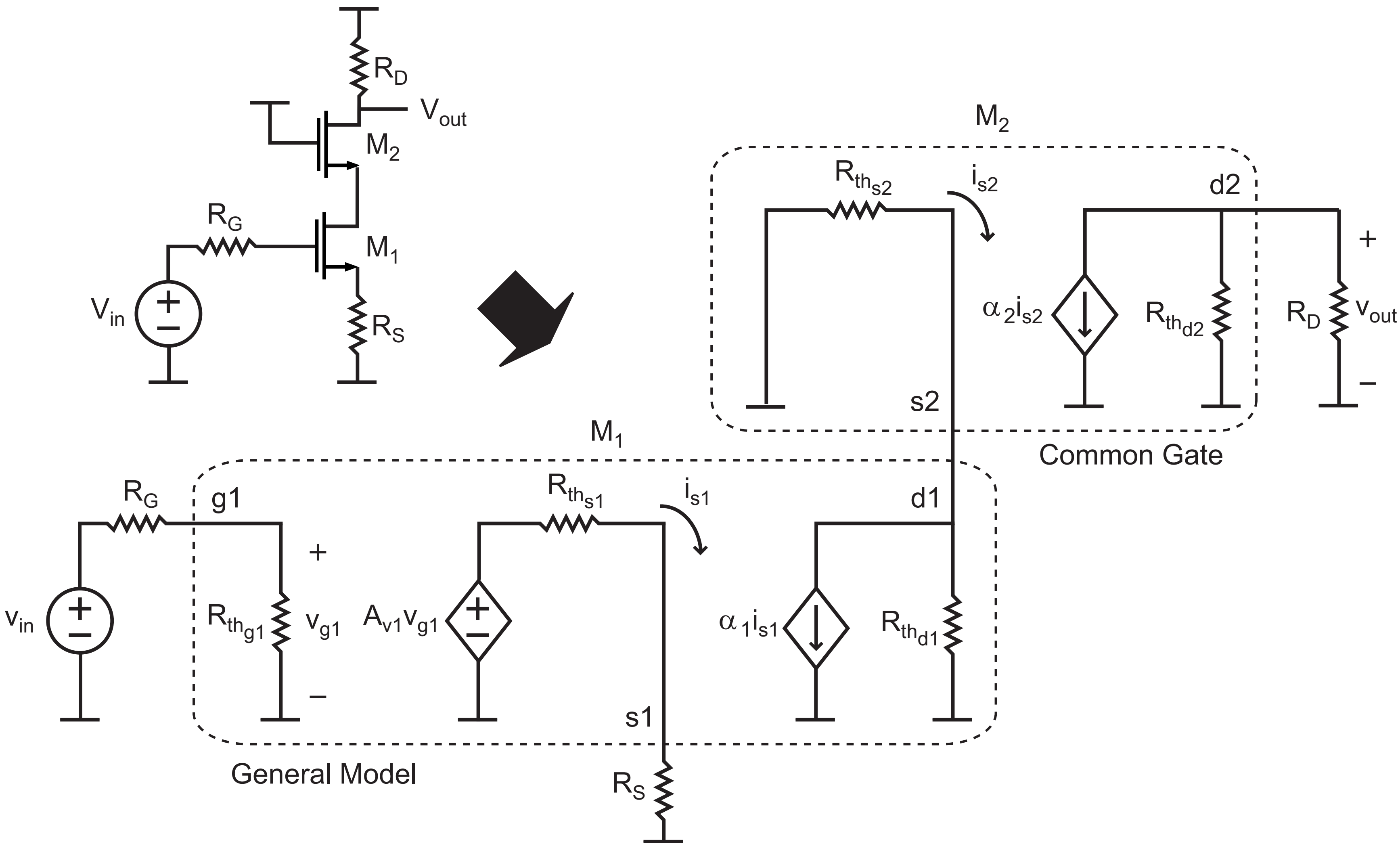
$$R_{th_d} = r_{o4}(1+(g_{m4}(1+g_{m3}(R_A||r_{o3}))+1/r_{o4}+g_{mb4})R_B$$

$$\approx (g_{m4}r_{o4})(g_{m3}(r_{o3}||R_A))R_B$$

$$R_{th_s} = \left(1+\frac{R_c}{r_{o4}}\right)\left(\frac{1}{g_{mb4}}||r_{o4}||\frac{1}{g_{m4}(1+g_{m3}(r_{o3}||R_A))}\right)$$

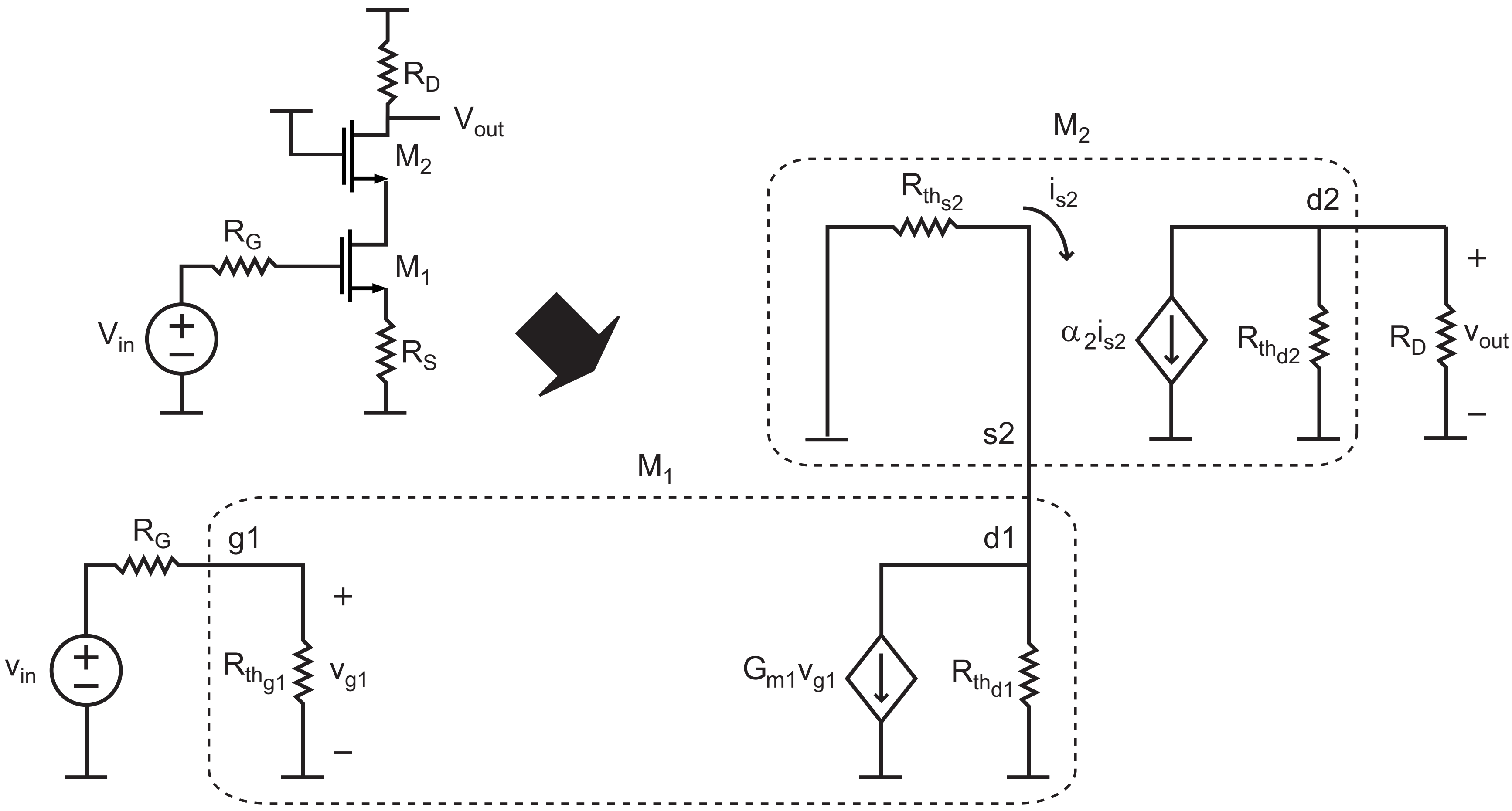
$$\approx \left(1+\frac{R_c}{r_{o4}}\right)\frac{1}{g_{m4}(g_{m3}(r_{o3}||R_A))}$$

Basic Cascode Amplifier



- **Allows improved frequency response (discussed later)**
- **Reduction to two-port will be done in several steps**

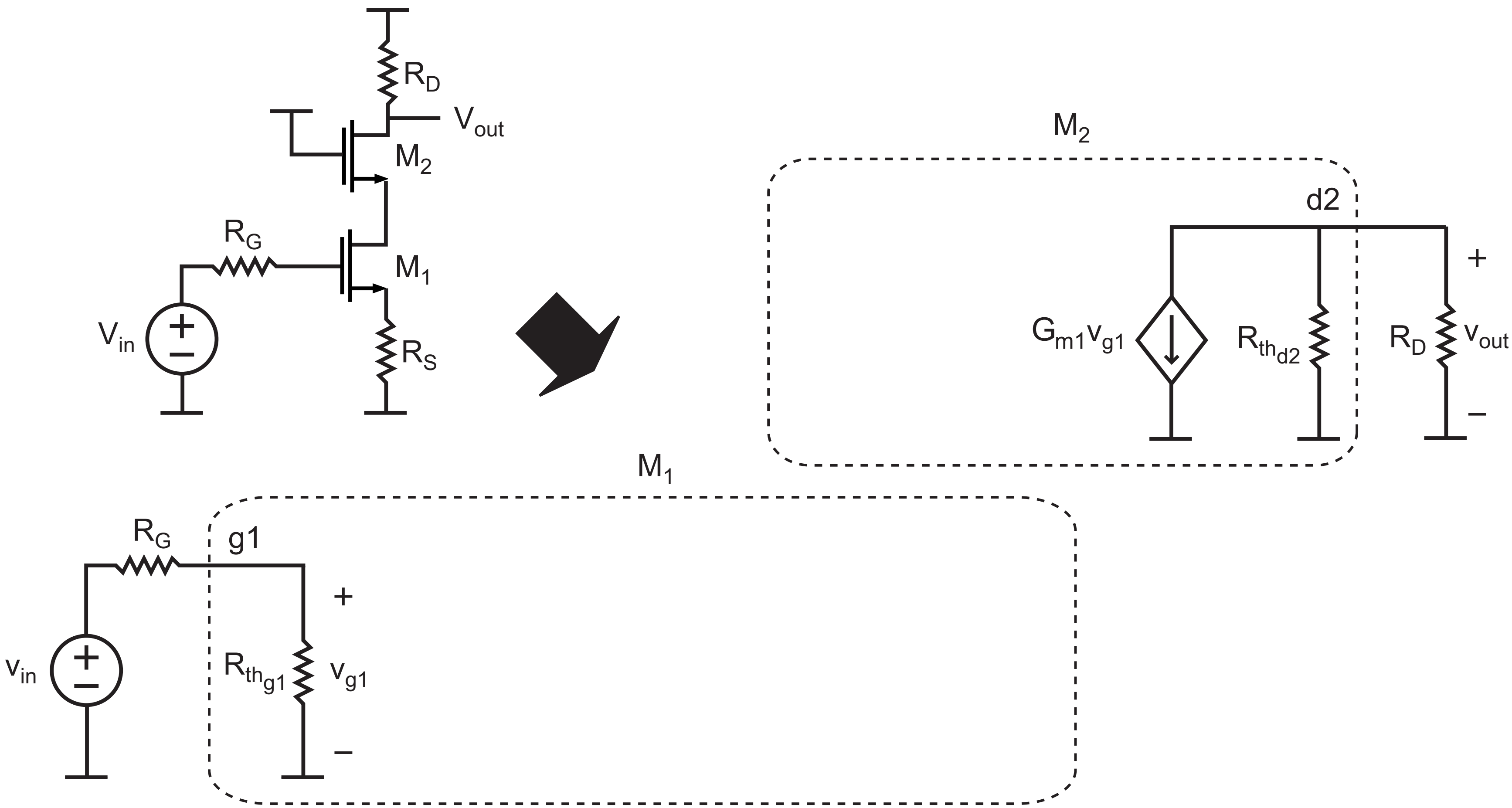
Eliminate Middle Sections



- **Calculation of G_{m1} same as for common source amp**
- **To reduce further, note that**

$$R_{th_{d1}} \gg R_{th_{s2}} \quad \Rightarrow \quad \alpha_2 i_{s2} = i_{s2} \approx G_{m1} v_{g1}$$

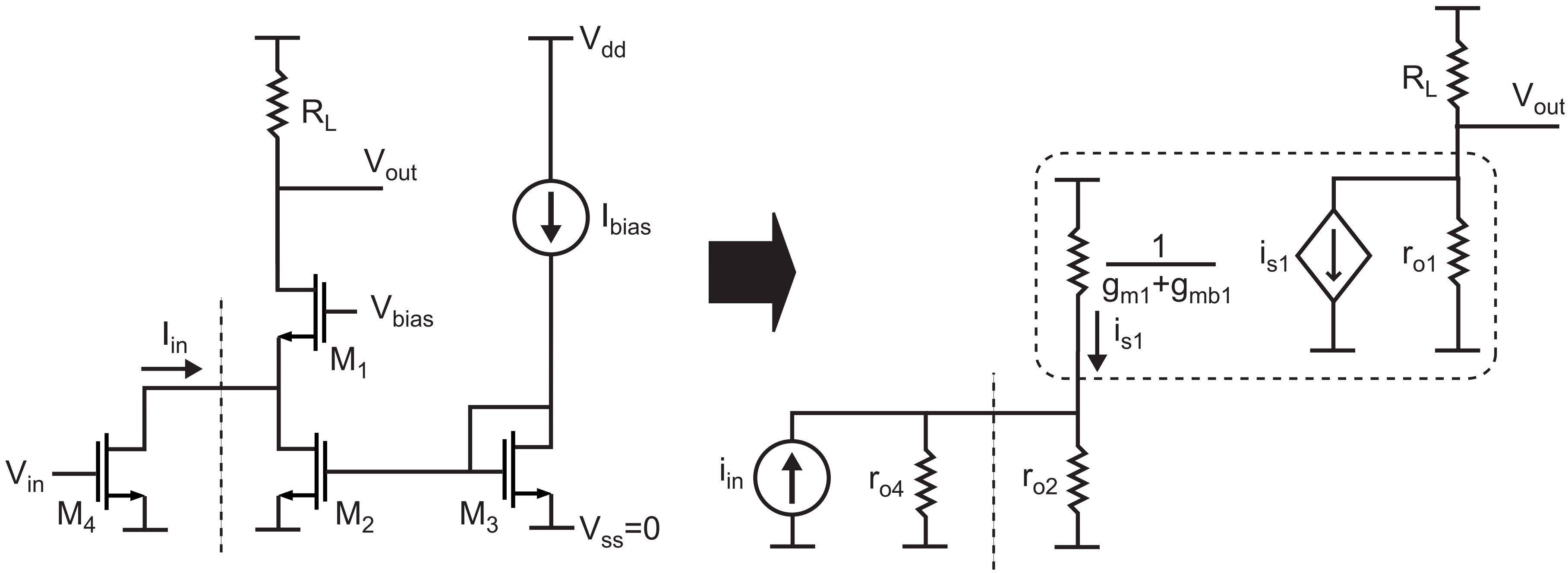
Resulting Two-Port Similar to Common Source Amp



- **Key difference: drain impedance much larger**

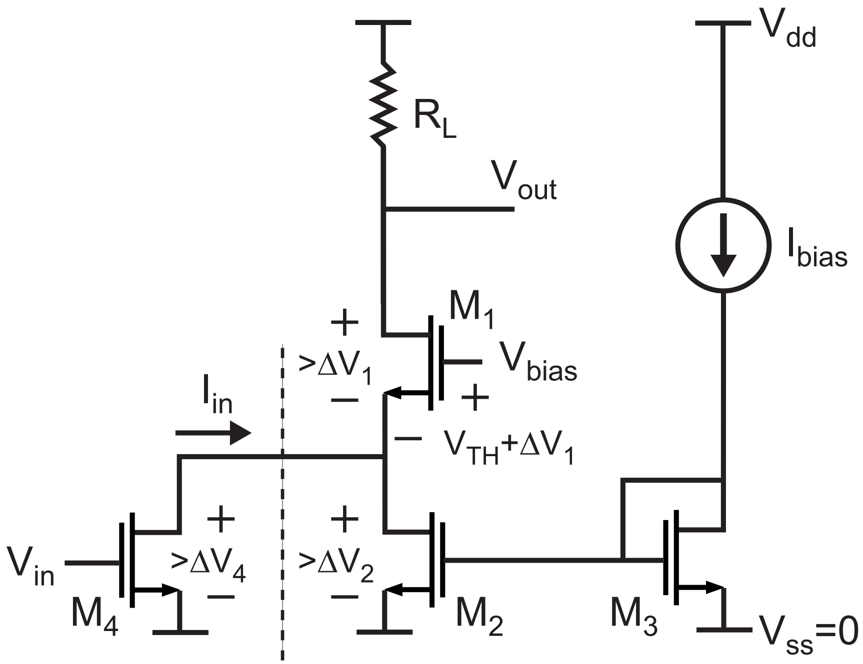
$$R_{th_{d2}} \approx r_{o2}(1+g_{m2}R_{th_{d1}}) \approx r_{o2}(1+g_{m2}r_{o1}(1+g_{m1}R_s))$$
$$\approx (g_{m2}r_{o2})(g_{m1}r_{o1})R_s$$

Slight Twist to Cascode Amplifier



- **What is the difference between this amplifier and basic cascode amplifier?**
- **What are the constraints in setting V_{bias}?**
- **What is the maximum output voltage swing?**

Constraints on V_{bias} and Output Range



- **To keep M_2 and M_4 in saturation**

$$V_{bias} - (V_{TH} + \Delta V_1) > \max(\Delta V_2, \Delta V_4)$$

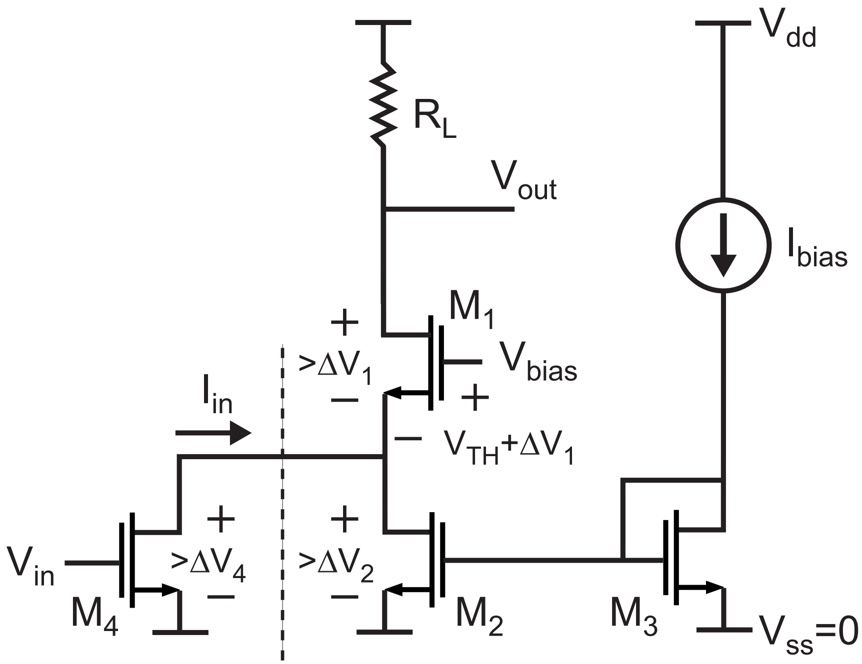
$$\Rightarrow V_{bias} > V_{TH} + \Delta V_1 + \max(\Delta V_2, \Delta V_4)$$

- **To keep M_1 in saturation**

$$V_{out} - (V_{bias} - (V_{TH} + \Delta V_1)) > \Delta V_1$$

$$\Rightarrow V_{out} > V_{bias} - V_{TH}$$

Calculation of Maximum Output Range



- **Minimum V_{bias} allows the maximum output range**

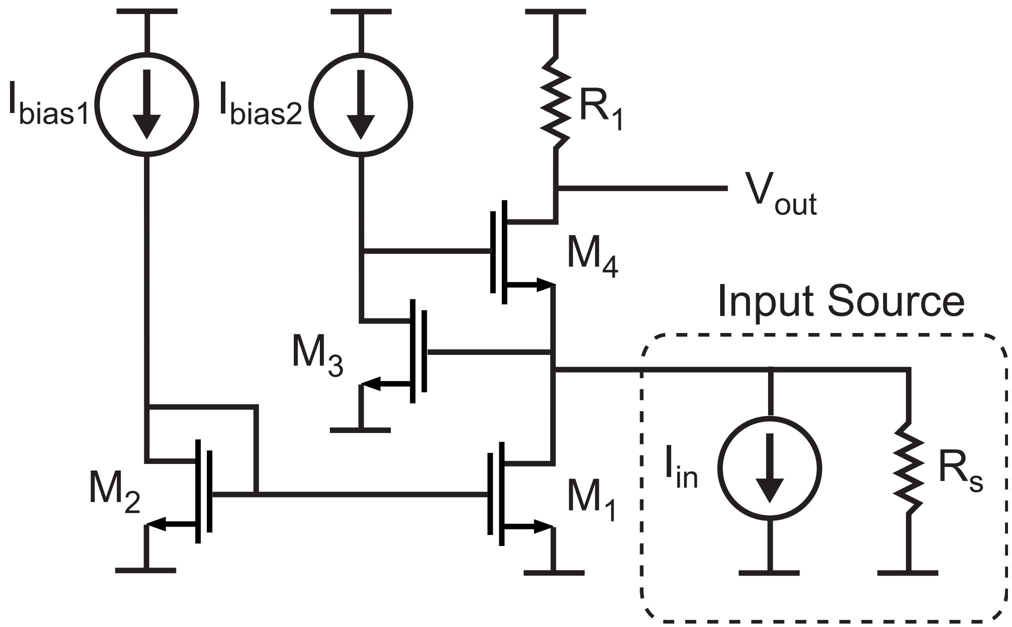
$$\Rightarrow V_{bias} = V_{TH} + \Delta V_1 + \max(\Delta V_2, \Delta V_4)$$

  - **Resulting output range**

$$V_{bias} - V_{TH} < V_{out} < V_{dd}$$

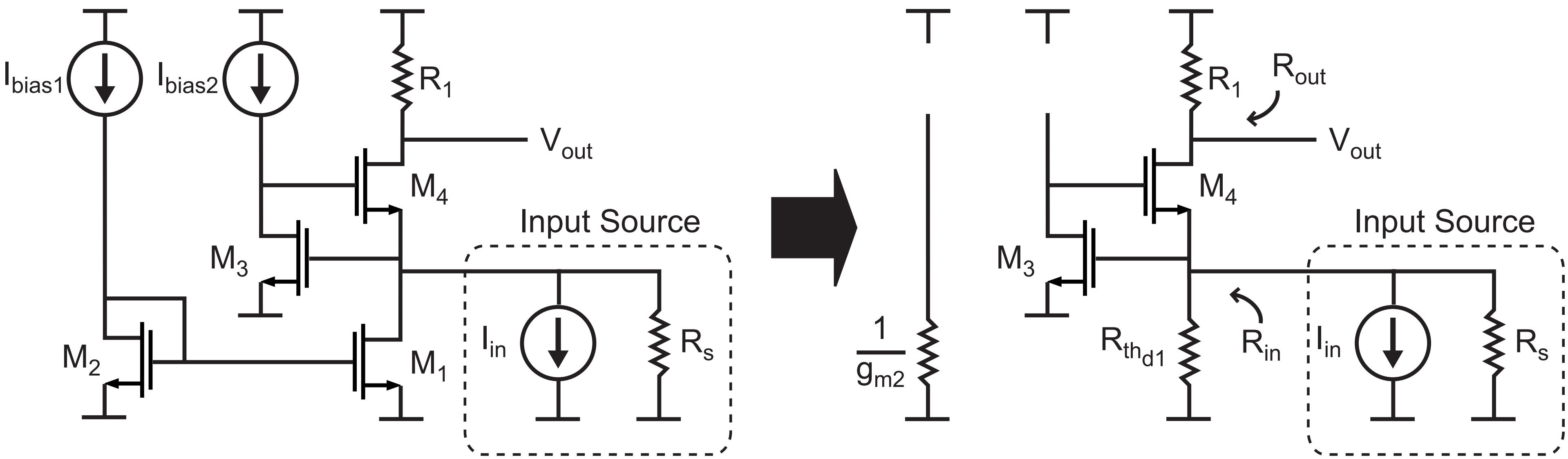
$$\Delta V_1 + \max(\Delta V_2, \Delta V_4) < V_{out} < V_{dd}$$

Variation on a Theme: Enhanced Cascode Amplifiers



- **We can turn the enhanced cascode current source into an amplifier**
  - **Inject a current input at the source of M_4**
- **Key aspects of small signal analysis can be done using Thevenin method**
  - **Simply leverage Thevenin resistance formulas shown on Slide 16**

Small-Signal Analysis of Enhanced Cascode Amp



- **From Thevenin resistance calculations on Slide 16:**
  - **Input impedance is quite low**

$$R_{in} \approx R_{th_{d1}} || \left(1 + \frac{R_1}{r_{o4}}\right) \frac{1}{g_{m4}(g_{m3}r_{o3})} \approx \frac{1}{g_{m4}(g_{m3}r_{o3})}$$

  - **Output impedance is probably determined by R_1**

$$R_{out} \approx R_1 || (g_{m4}r_{o4})(g_{m3}r_{o3})(R_{th_{d1}} || R_s) \approx R_1$$

- **This amplifier is useful for extracting a current signal while keeping the source voltage nearly constant**