High Speed Communication Circuits and Systems
Lecture 14
High Speed Frequency Dividers

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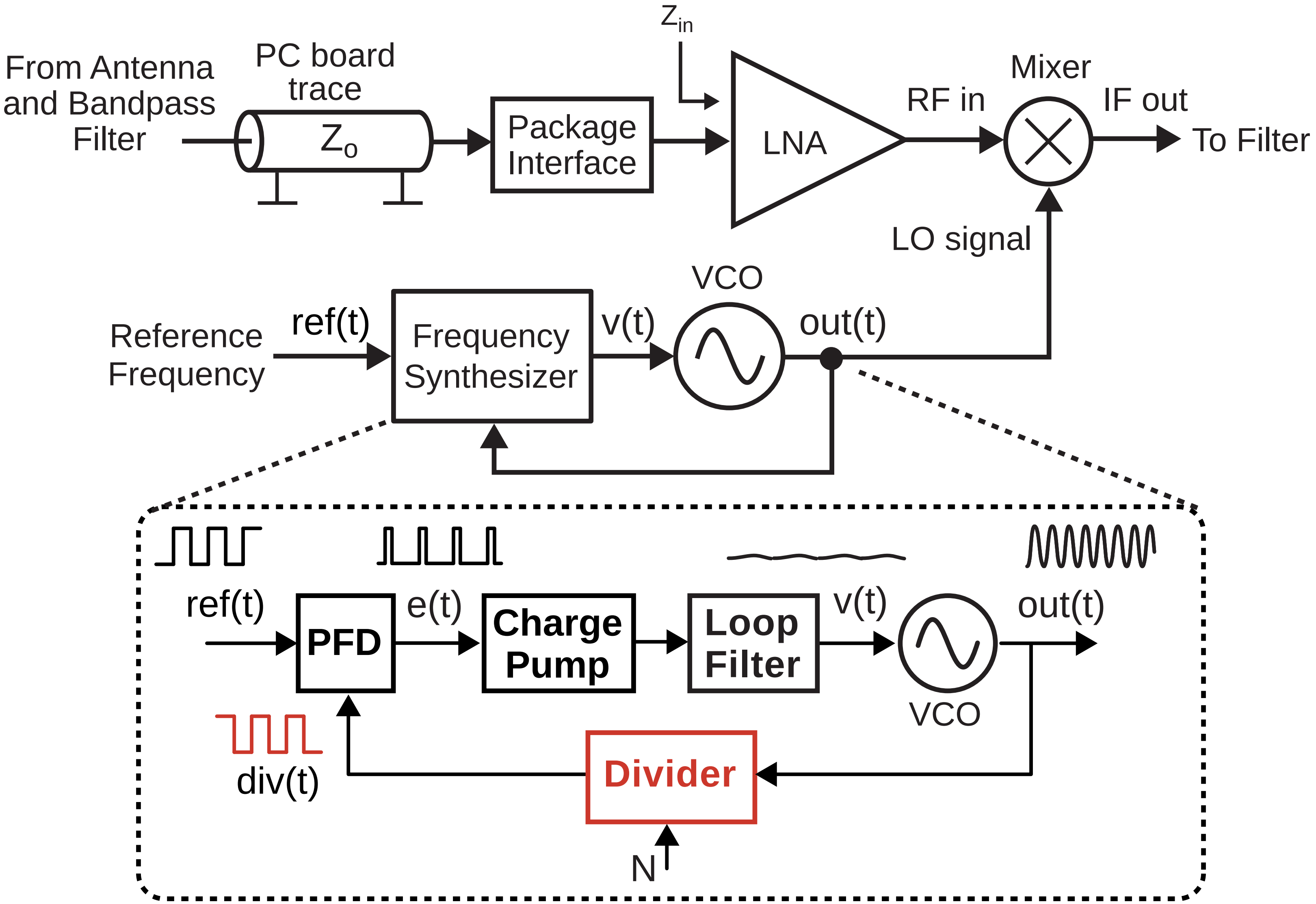
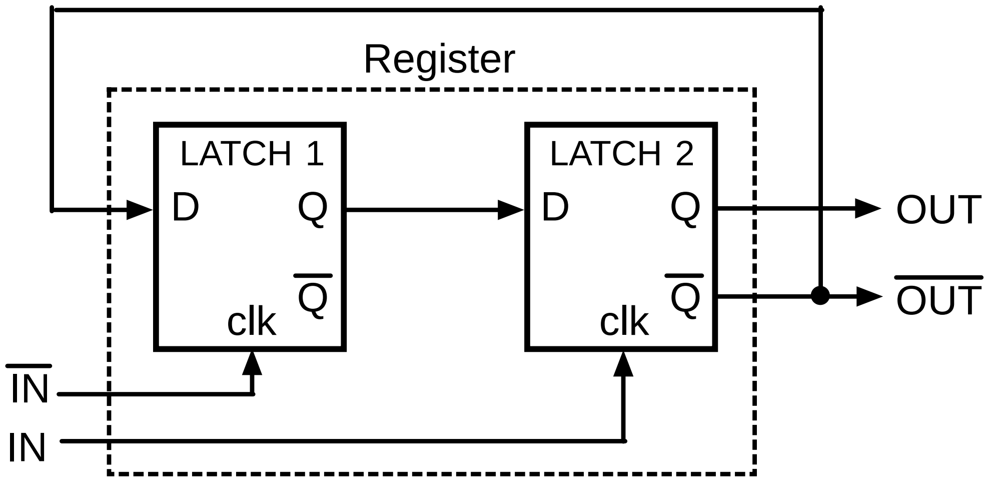
March 19, 2004

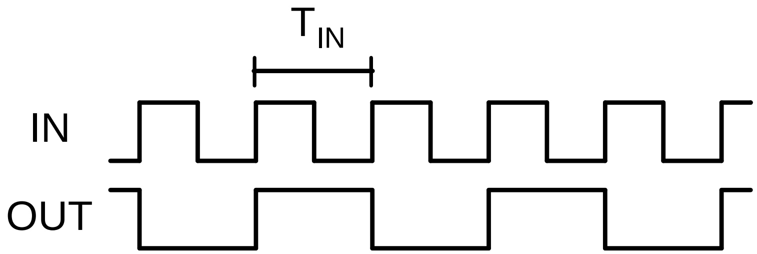
High Speed Frequency Dividers in Wireless Systems



- **Design Issues: high speed, low power**

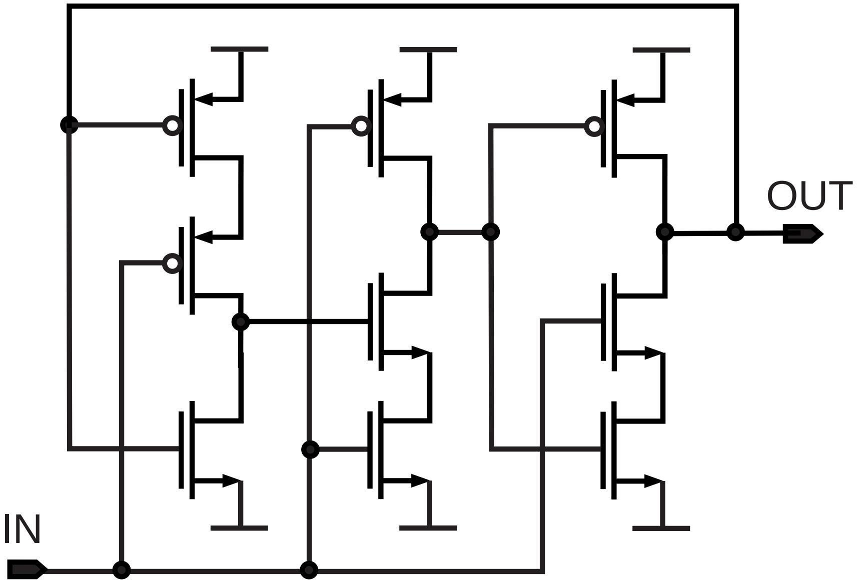
Divide-by-2 Circuit (Johnson Counter)

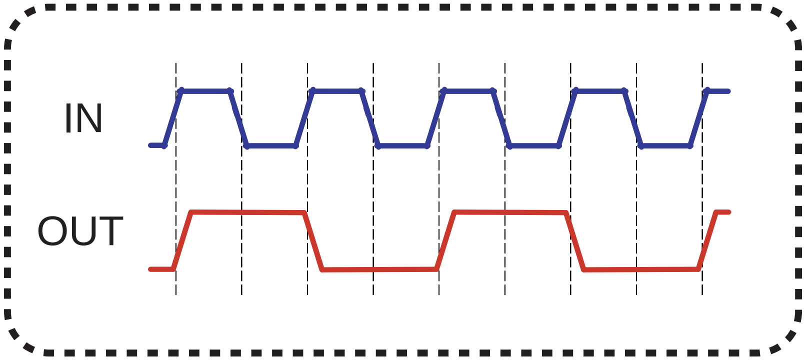




- **Achieves frequency division by clocking two latches (i.e., a register) in negative feedback**
- **Latches may be implemented in various ways according to speed/power requirements**

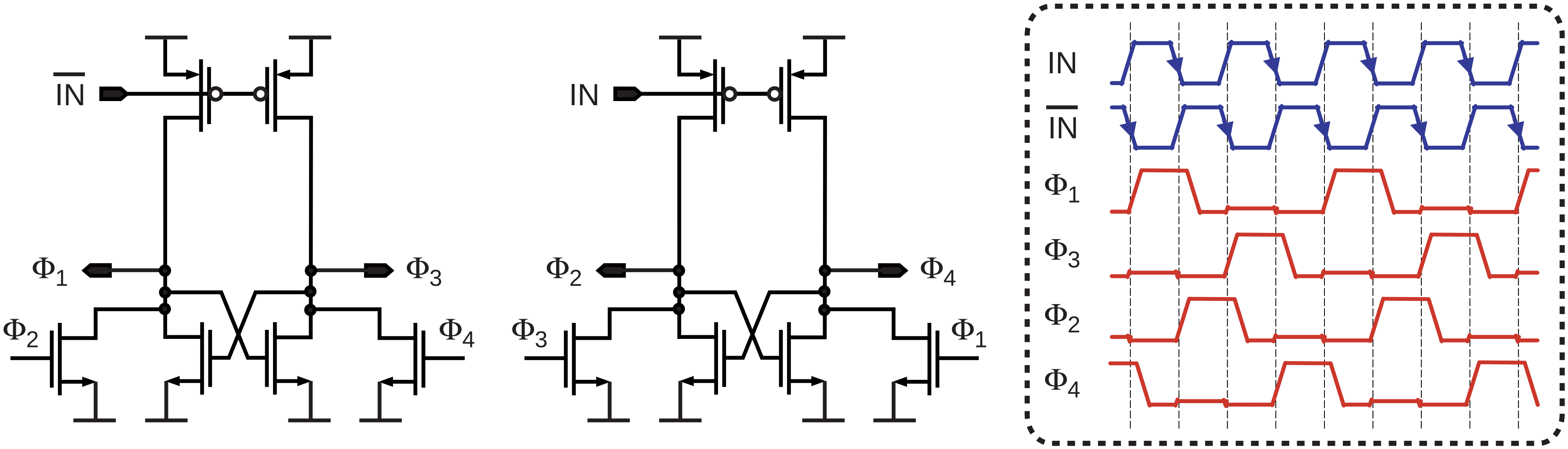
Divide-by-2 Using a TSPC register





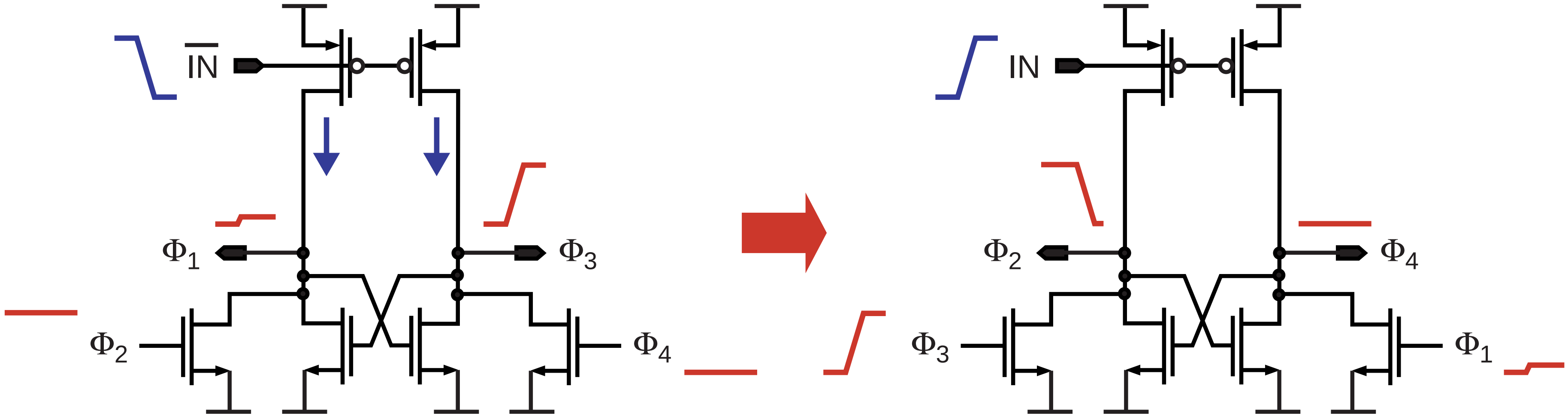
- **Advantages**
  - **Reasonably fast, compact size**
  - **No static power dissipation, differential clock not required**
- **Disadvantages**
  - **Slowed down by stacked PMOS, signals goes through three gates per cycle**
  - **Requires full swing input clock signal**

Divide-by-2 Using Razavi's Topology



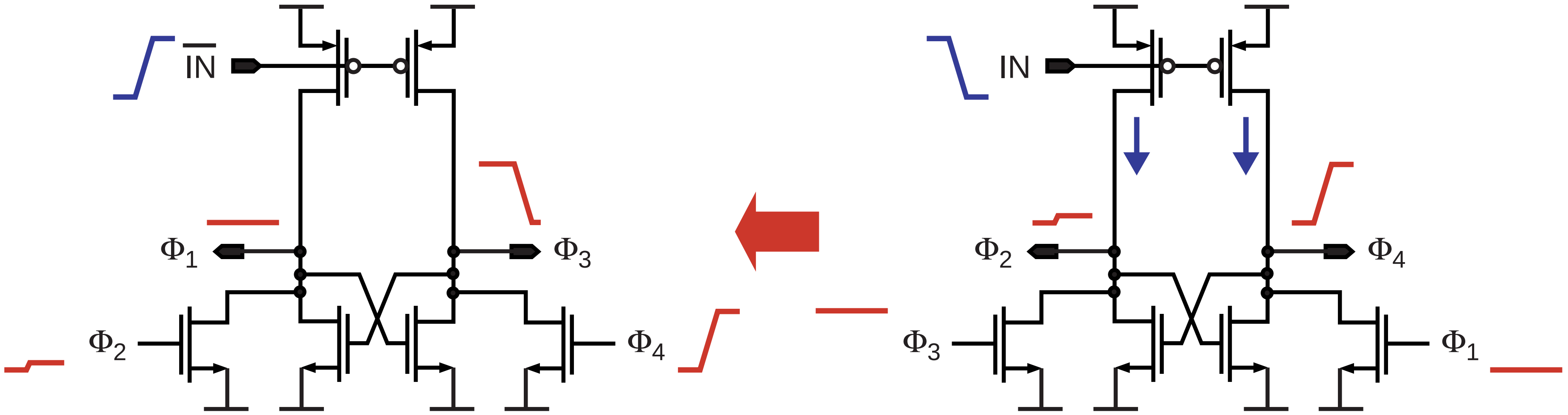
- **Faster topology than TSPC approach**
- **See B. Rezavi et. al., "Design of High Speed, Low Power Frequency Dividers and Phase-Locked Loops in Deep Submicron CMOS", JSSC, Feb 1995, pp 101-109**

Explanation of Razavi Divider Operation (Part 1)



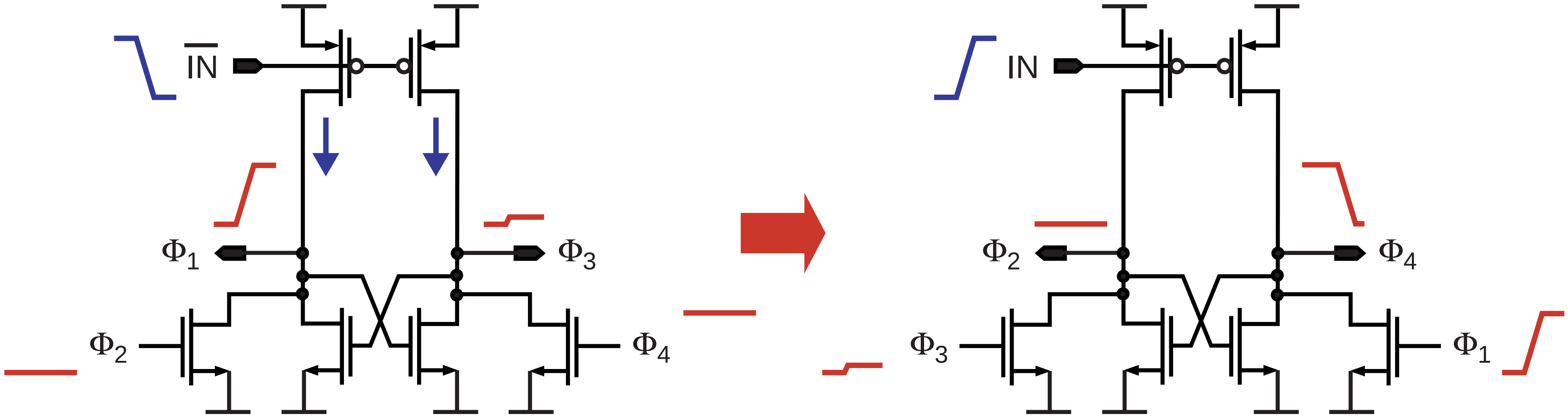
- **Left latch:**
  - **Clock drives current from PMOS devices of a given latch onto the NMOS cross-coupled pair**
  - **Latch output voltage rises asymmetrically according to voltage setting on gates of outside NMOS devices**
- **Right latch:**
  - **Outside NMOS devices discharge the latch output voltage as the left latch output voltage rises**

Explanation of Razavi Divider Operation (Part 2)



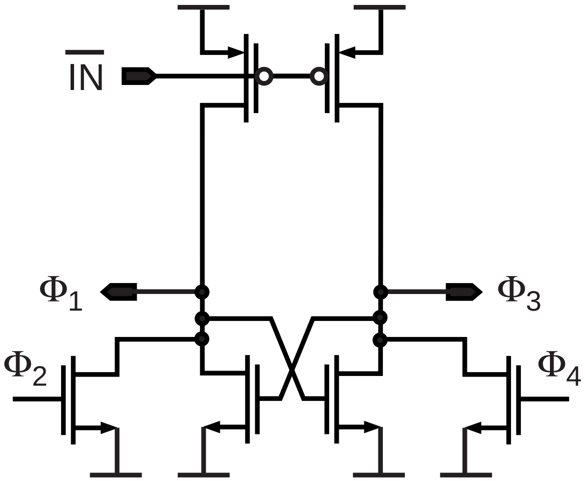
- **Right latch:**
  - **Clock drives current from PMOS devices of a given latch onto the NMOS cross-coupled pair**
  - **Latch output voltage rises asymmetrically according to voltage setting on gates of outside NMOS devices**
- **Left latch:**
  - **Outside NMOS devices discharge the latch output voltage as the left latch output voltage rises**

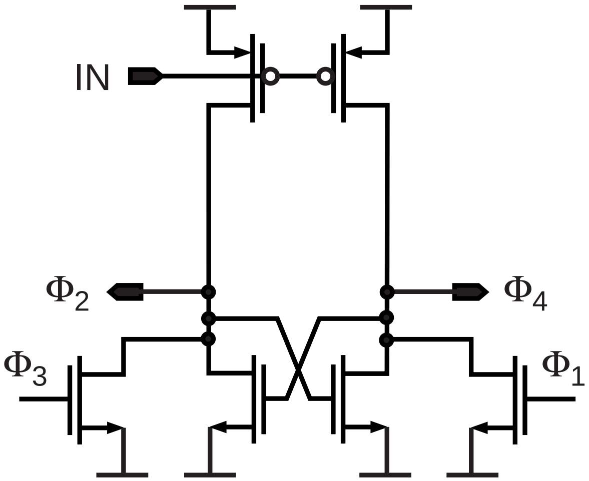
Explanation of Razavi Divider Operation (Part 3)

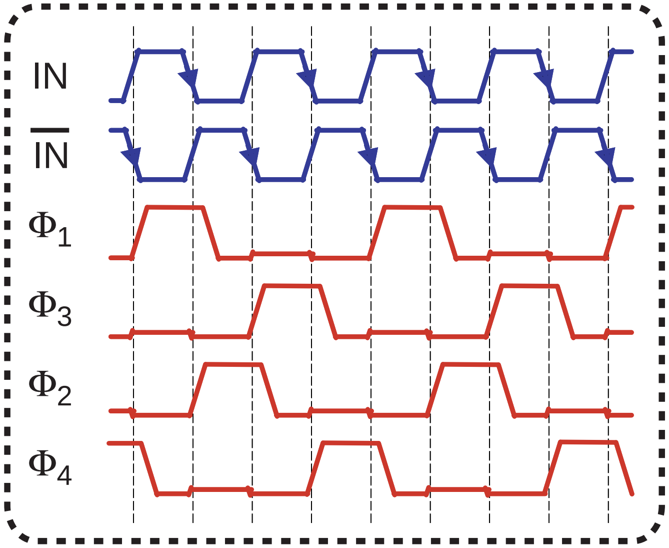


- **Process starts over again with current being driven into left latch**
  - **Voltage polarity at the output of the latch has now flipped**

Advantages and Disadvantages of Razavi Topology

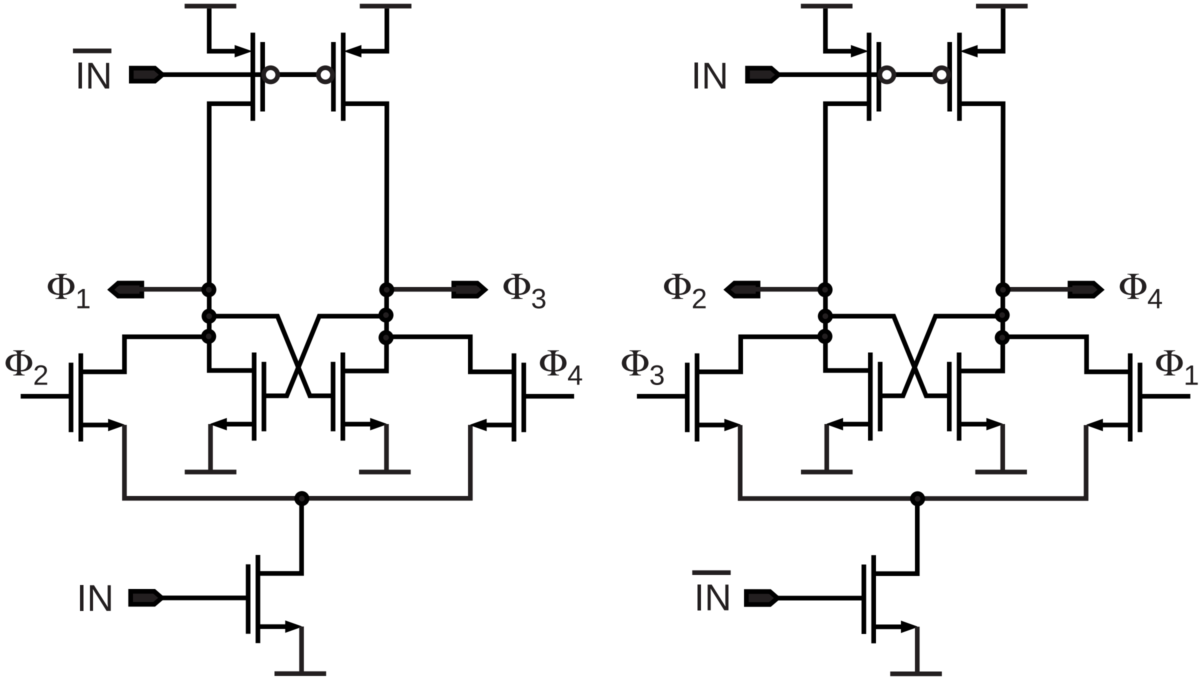


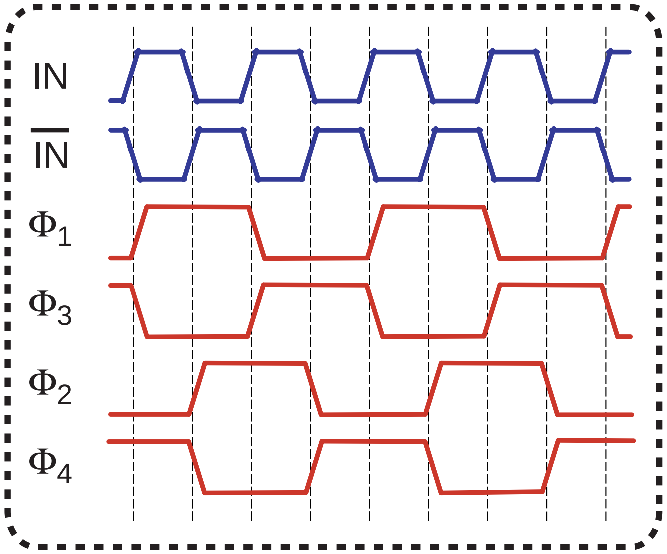




- **Advantages**
  - **Fast – no stacked PMOS, signal goes through only two gates per cycle**
- **Disadvantages**
  - **Static power**
  - **Full swing, differential input clock signal required**
- **Note: quarter period duty cycle can be turned into fifty percent duty cycle with OR gates after the divider**
  - **See my thesis at http://www-mtl.mit.edu/~perrott**

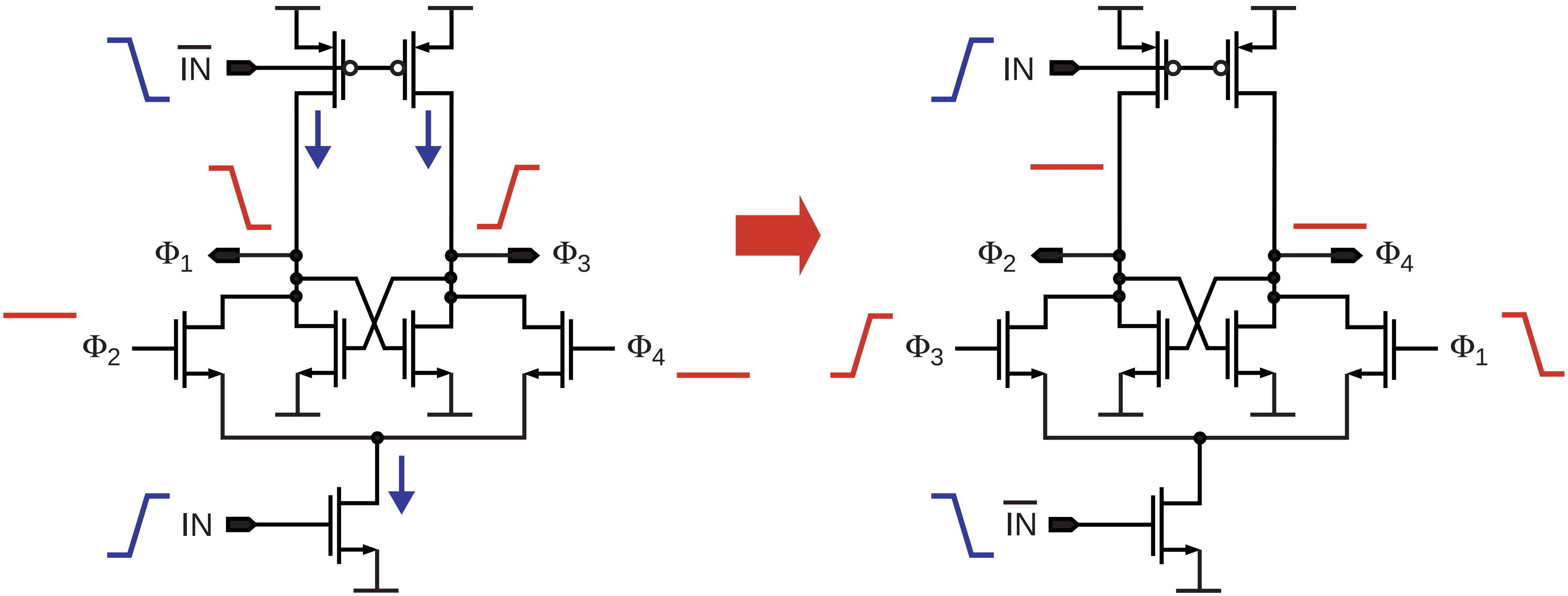
Divide-by-2 Using Wang Topology





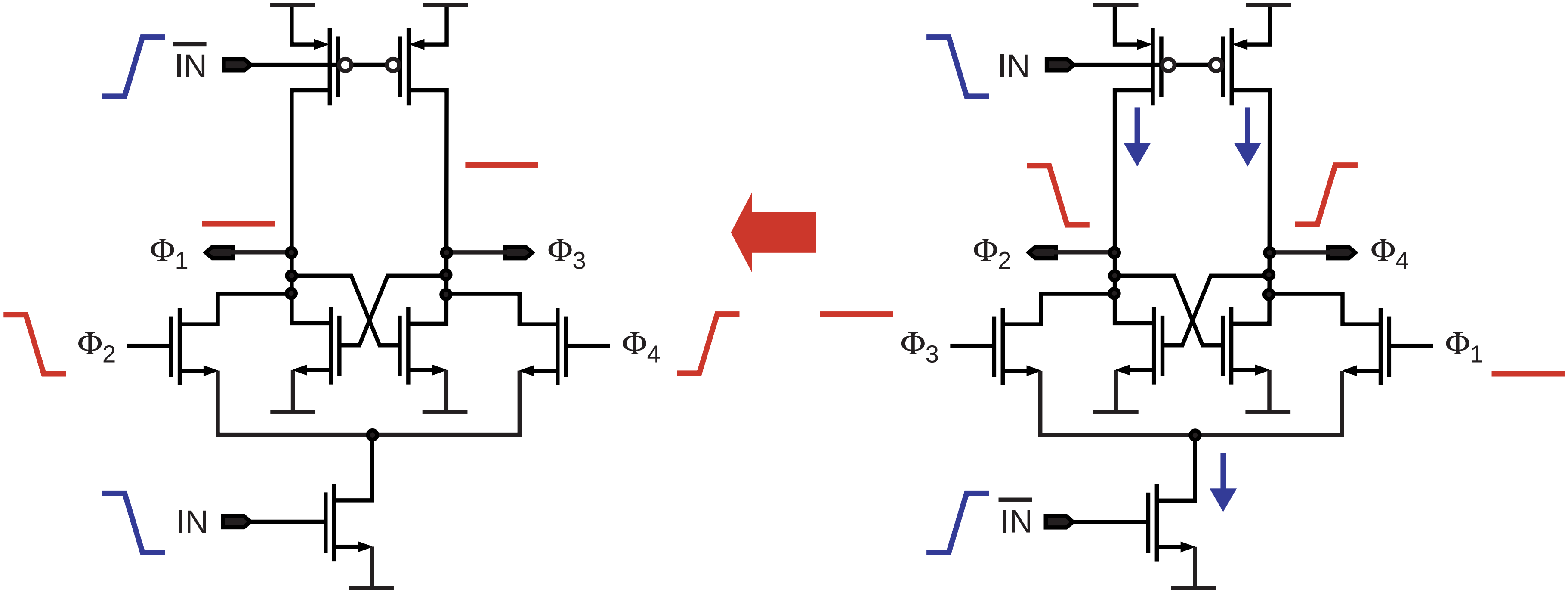
- **Claims to be faster than Razavi topology**
  - **Chief difference is addition of NMOS clock devices and different scaling of upper PMOS devices**
- **See HongMo Wang, “A 1.8 V 3 mW 16.8 GHz Frequency Divider in 0.25μm CMOS”, ISSCC 2000, pp 196-197**

Explanation of Wang Topology Operation (Part 1)



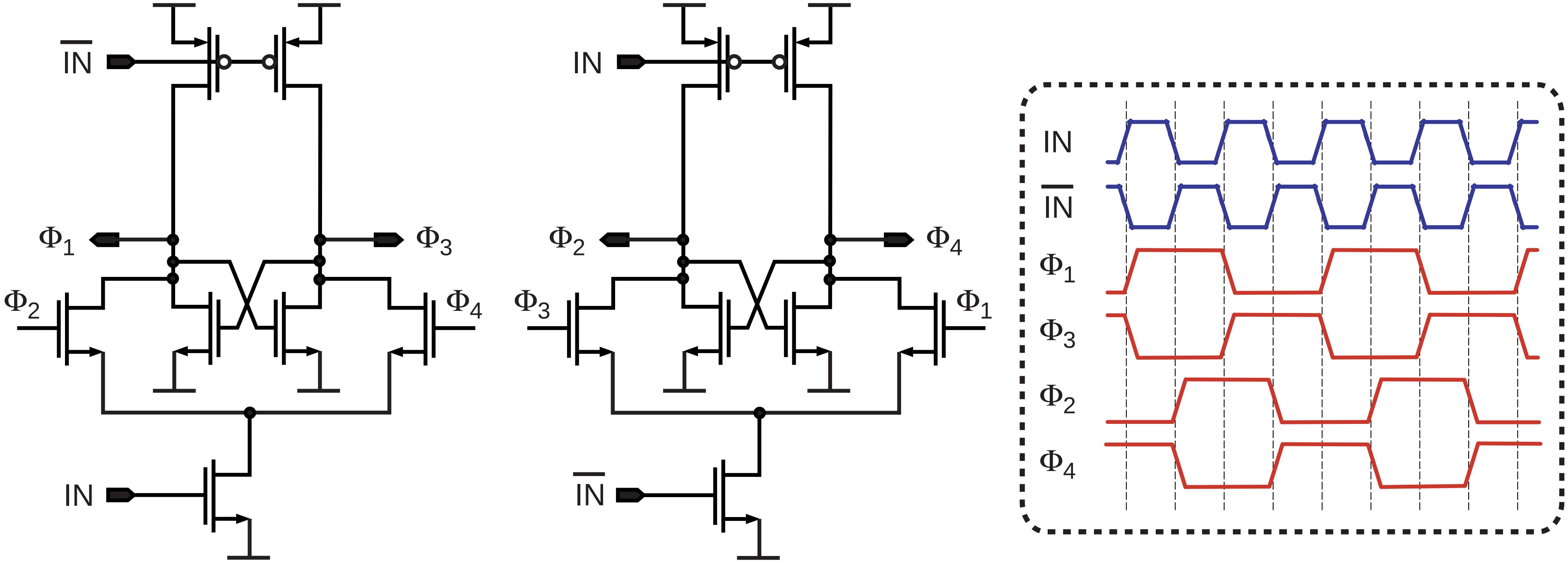
- **Left latch**
  - **Current driven into latch and output voltage responds similar to Razavi architecture**
- **Right latch**
  - **Different than Razavi architecture in that latch output voltage is *not* discharged due to presence of extra NMOS**

Explanation of Wang Topology Operation (Part 2)



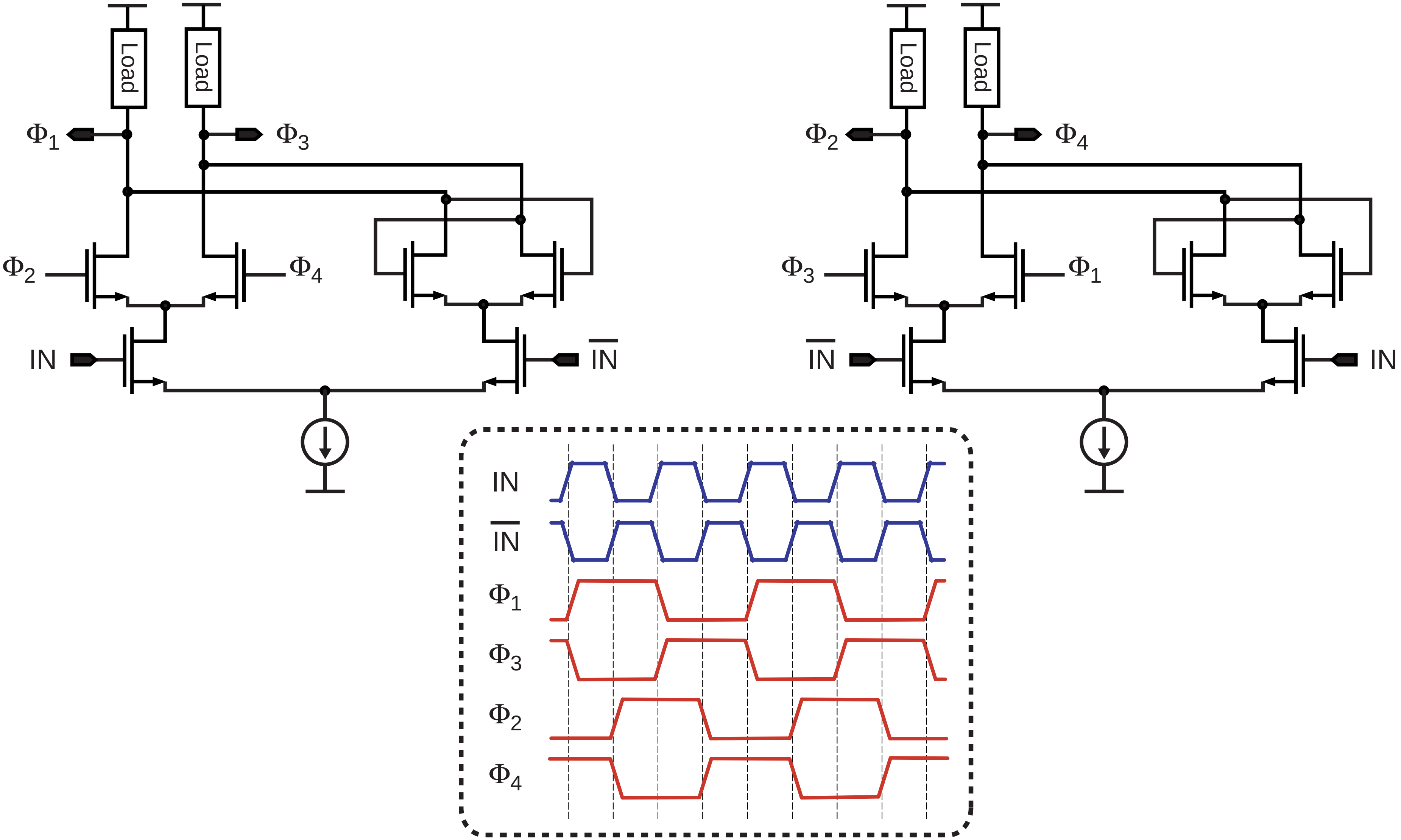
- **Same process repeats on the right side**
  - **The left side maintains its voltages due to presence of NMOS device**

Advantages and Disadvantages of Wang Topology



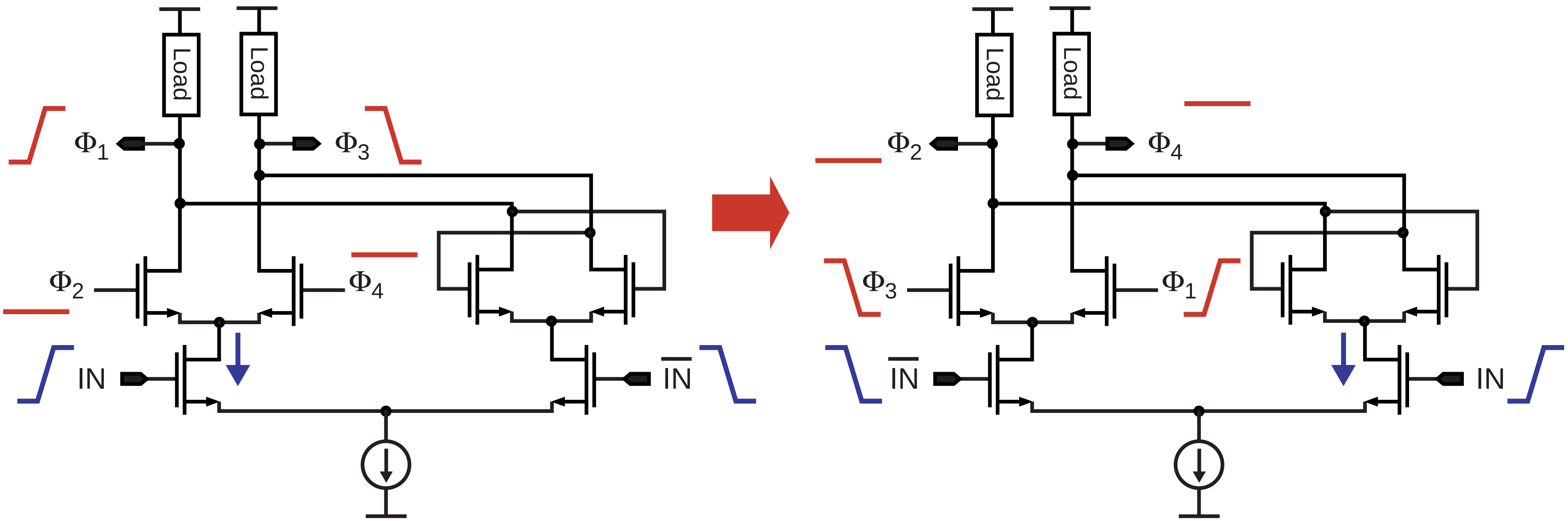
- **Advantages**
  - **Fast – no stacked PMOS, signal goes through only two gates per cycle**
- **Disadvantages**
  - **Static power**
  - **Full swing, differential input clock signal required**

Divide-by-2 Using SCL Latches



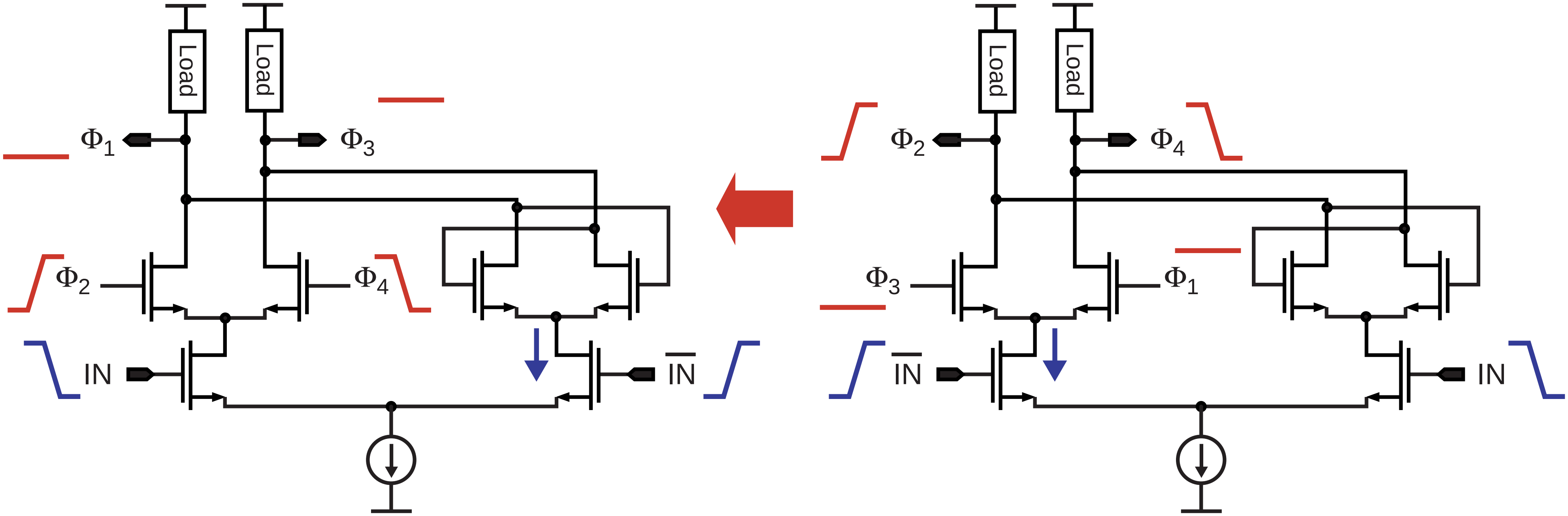
- **Fastest structure uses resistors for load**

Explanation of SCL Topology Operation (Part 1)



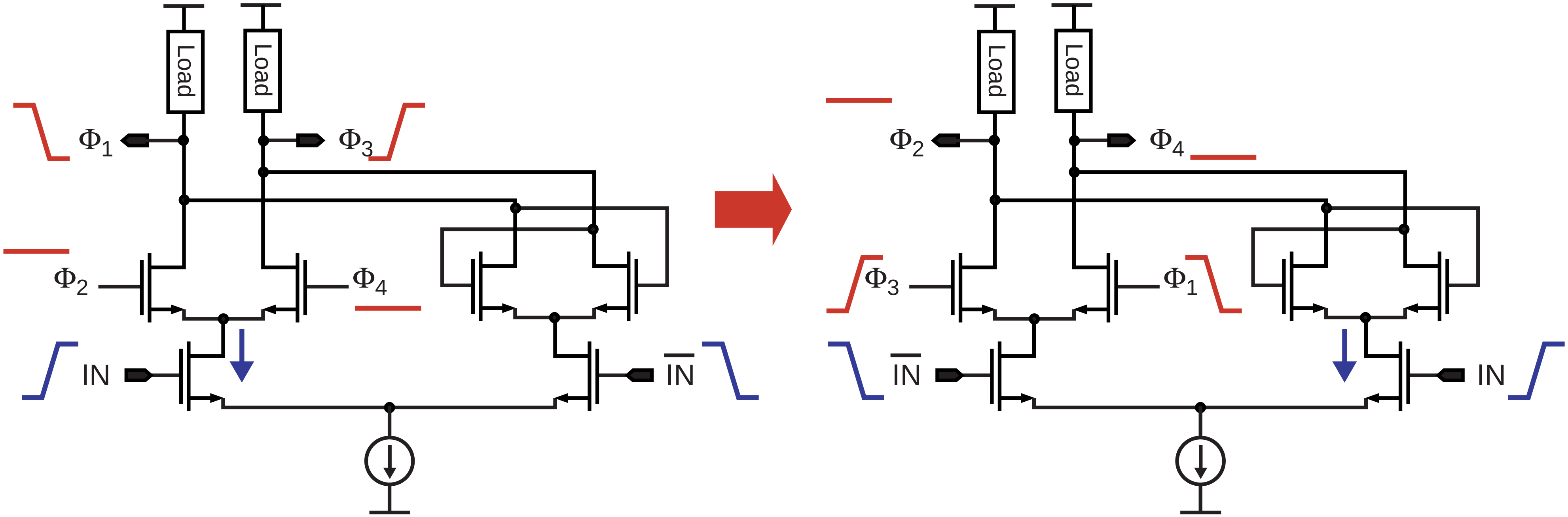
- **Left latch**
  - **Current directed into differential amp portion of latch**
    - Latch output follows input from right latch
- **Right latch**
  - **Current directed into cross-coupled pair portion of latch**
    - Latch output is held

Explanation of SCL Topology Operation (Part 2)



- **Left latch**
  - **Current is directed into cross-coupled pair**
    - Latch output voltage retained
- **Right latch**
  - **Current is directed into differential amp**
    - Latch output voltage follows input from left latch

Explanation of SCL Topology Operation (Part 3)



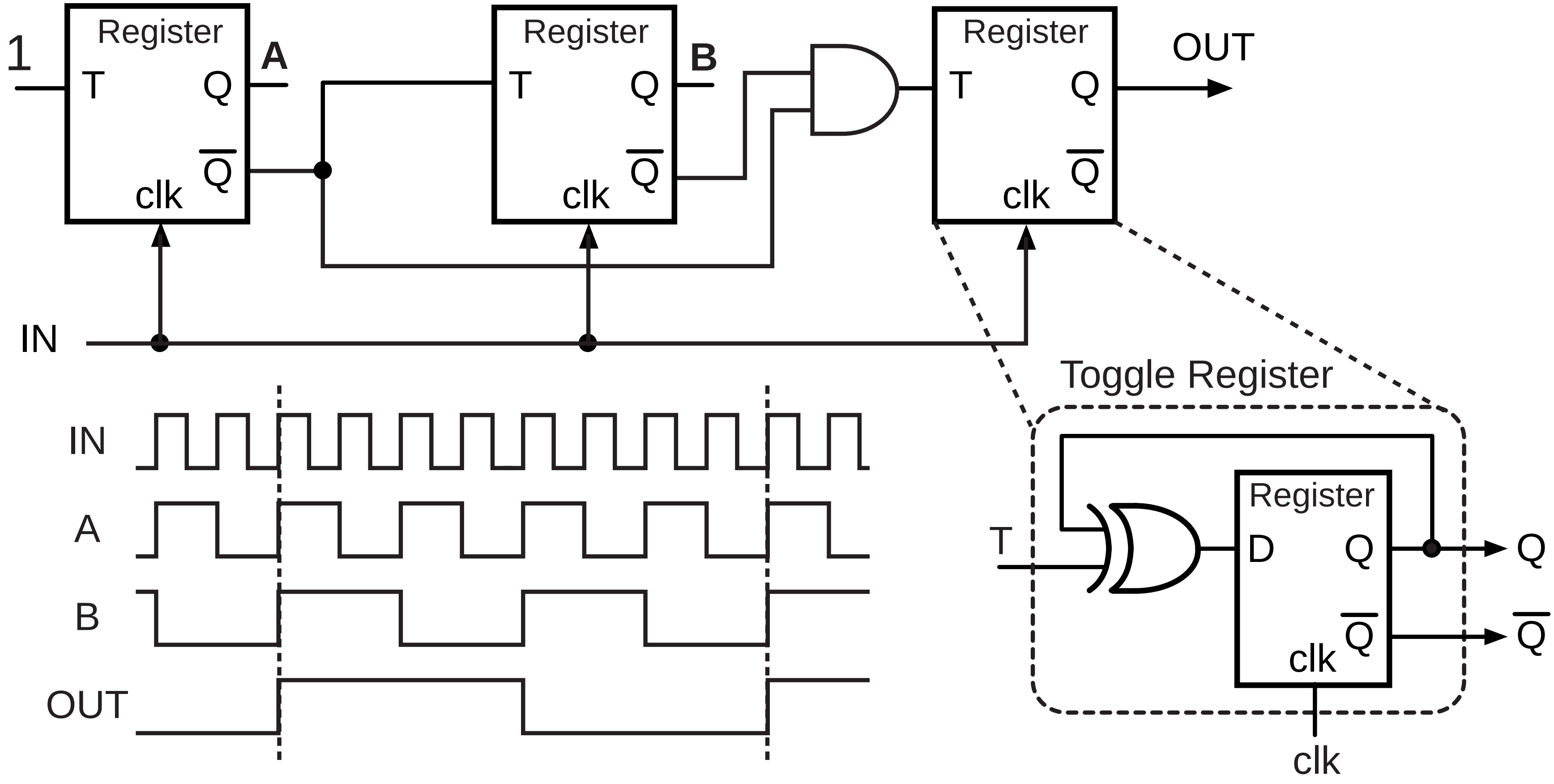
- Same process repeats on left side
  - Voltage polarity is now flipped

Advantages and Disadvantages of SCL Topology

- **Advantages**
  - **Very fast – no PMOS at all, signal goes through only two gates per cycle**
  - **Smaller input swing for input clock than previous approaches**
    - Much easier to satisfy at high frequencies
- **Disadvantages**
  - **Static power**
  - **Differential signals required**
  - **Large area compared to previous approaches**
  - **Biasing sources required**

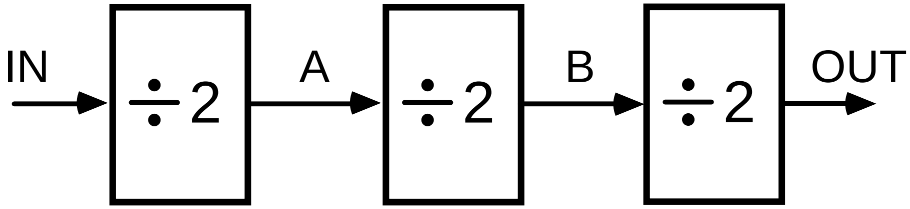
- **Note: additional speedup can be obtained by adding using inductor peaking as described for amplifiers in Lecture 6**

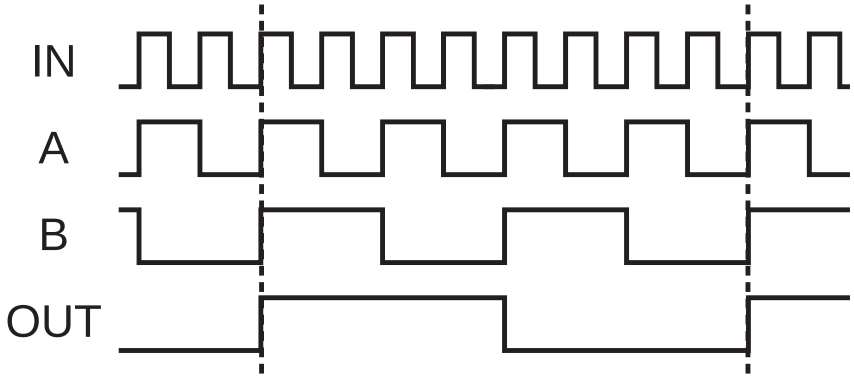
Creating Higher Divide Values (Synchronous Approach)



- **Cascades toggle registers and logic to perform division**
  - **Advantage: low jitter (explained shortly)**
  - **Problems: high power (all registers run at high frequency), high loading on clock (IN signal drives *all* registers)**

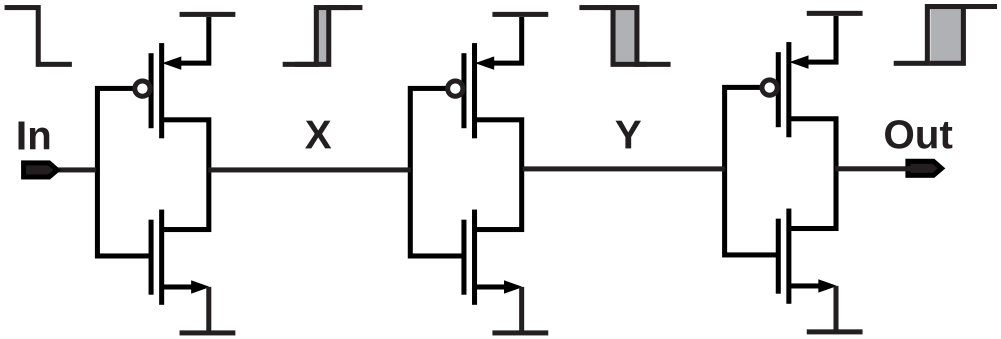
Creating Higher Divide Values (Asynchronous Approach)





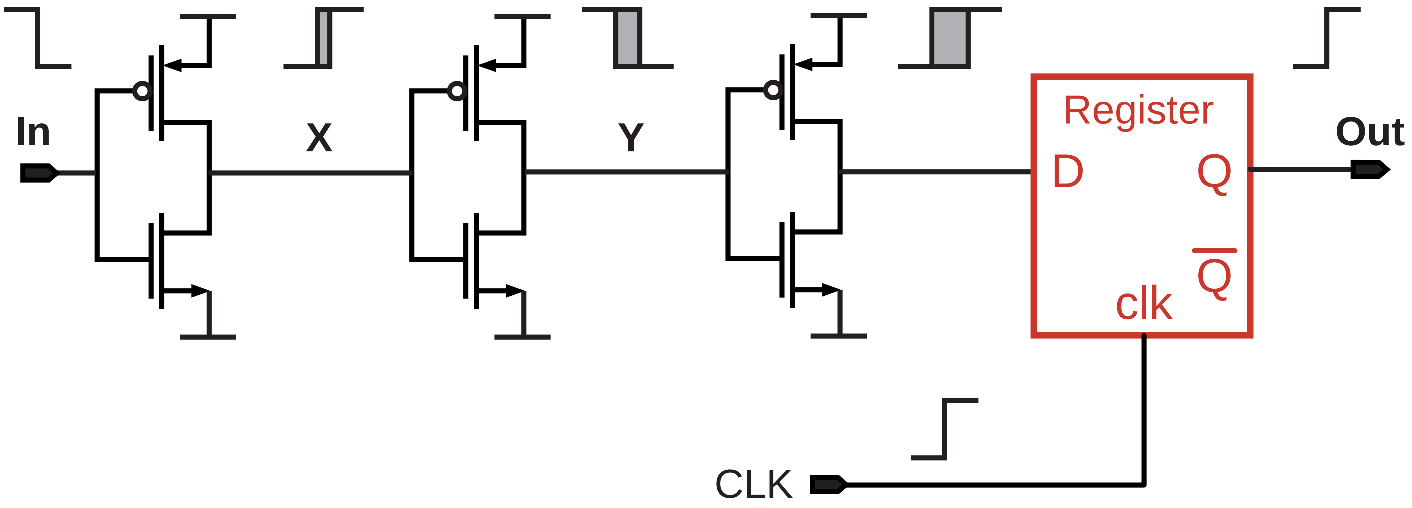
- **Higher division achieved by simply cascading divide-by-2 stages**
- **Advantages over synchronous approach**
  - **Lower power: each stage runs at a lower frequency, allowing power to be correspondingly reduced**
  - **Less loading of input: IN signal only drives first stage**
- **Disadvantage: jitter is larger**

Jitter in Asynchronous Designs



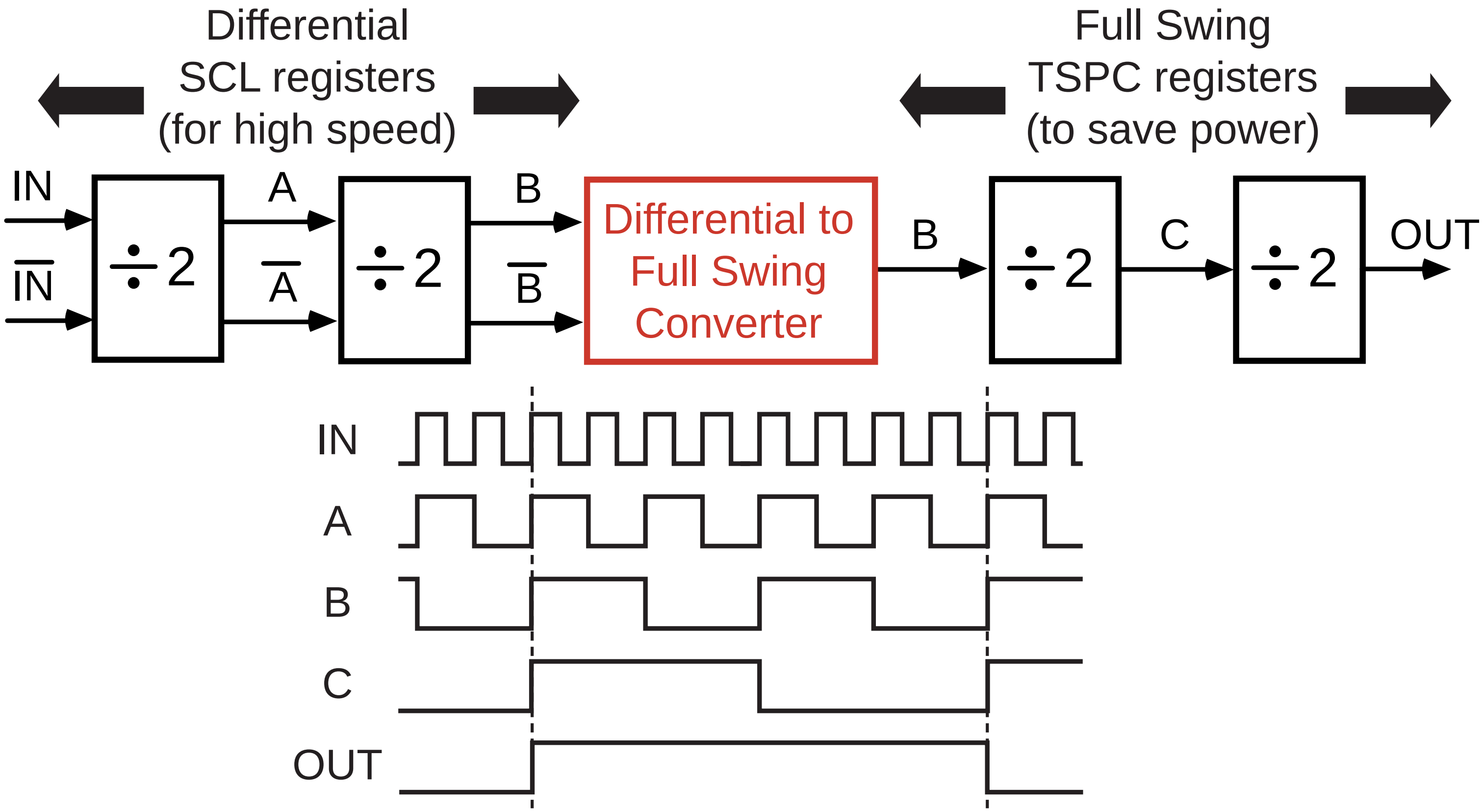
- Each logic stage adds jitter to its output
  - Jitter accumulates as it passes through more and more gates

Jitter in Synchronous Designs



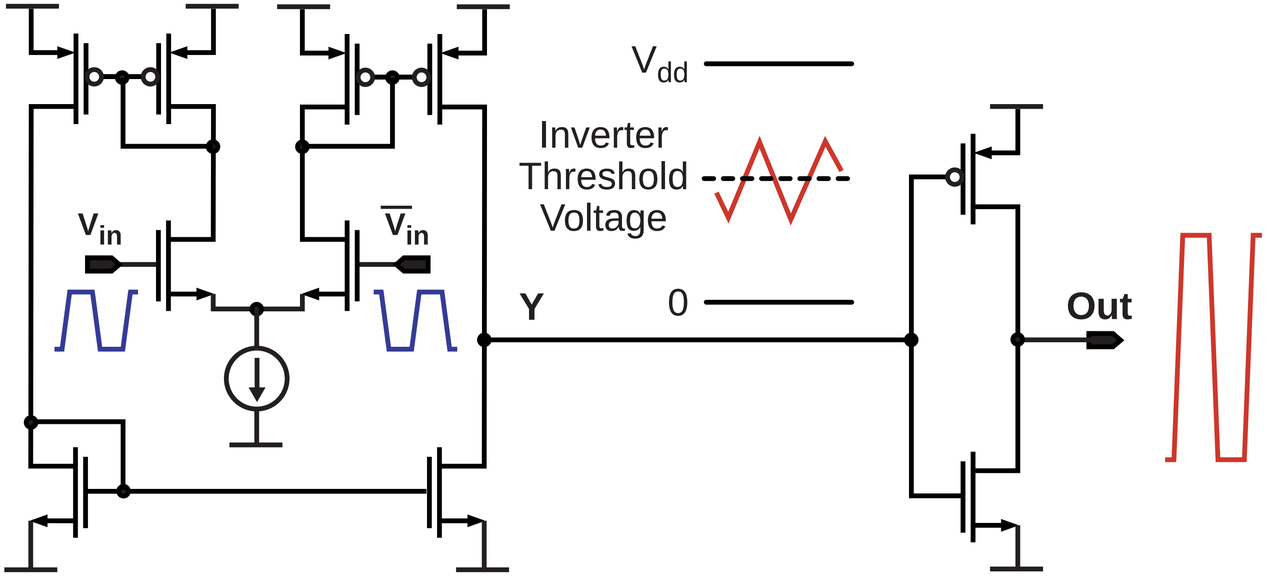
- **Transition time of register output is set by the clock, not the incoming data input**
  - **Synchronous circuits have jitter performance corresponding to their clock**
  - **Jitter does not accumulate as signal travels through synchronous stages**

High Speed, Low Power Asynchronous Dividers



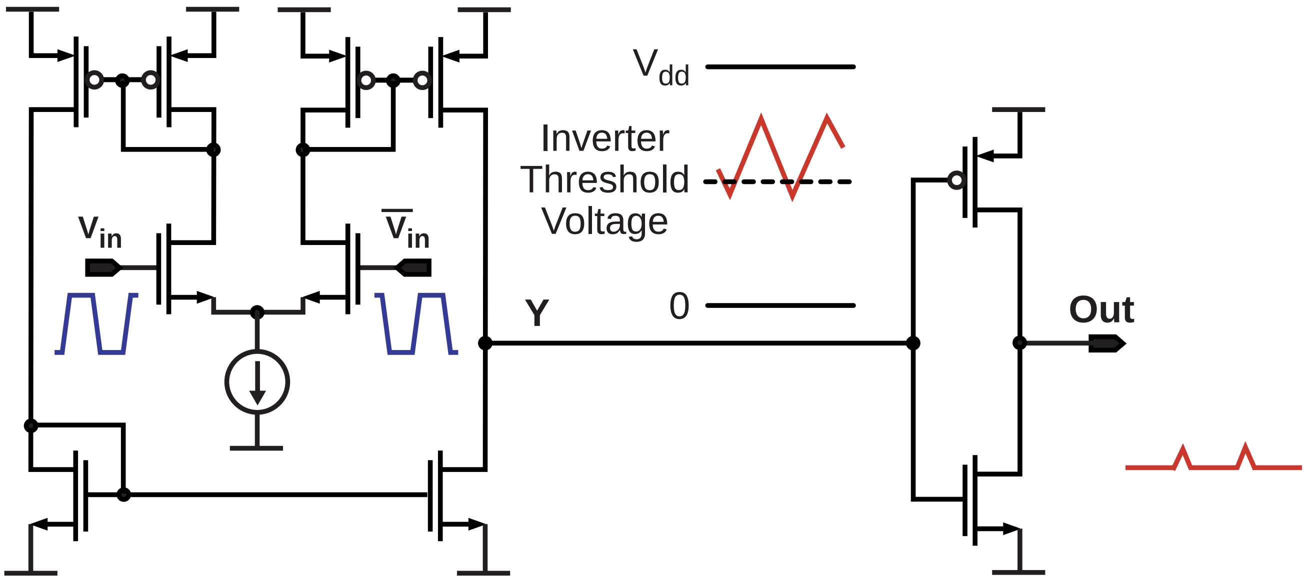
- **Highest speed achieved with differential SCL registers**
  - **Static power consumption not an issue for high speed sections, but wasteful in low speed sections**
- **Lower power achieved by using full swing logic for low speed sections**

Differential to Full Swing Converter



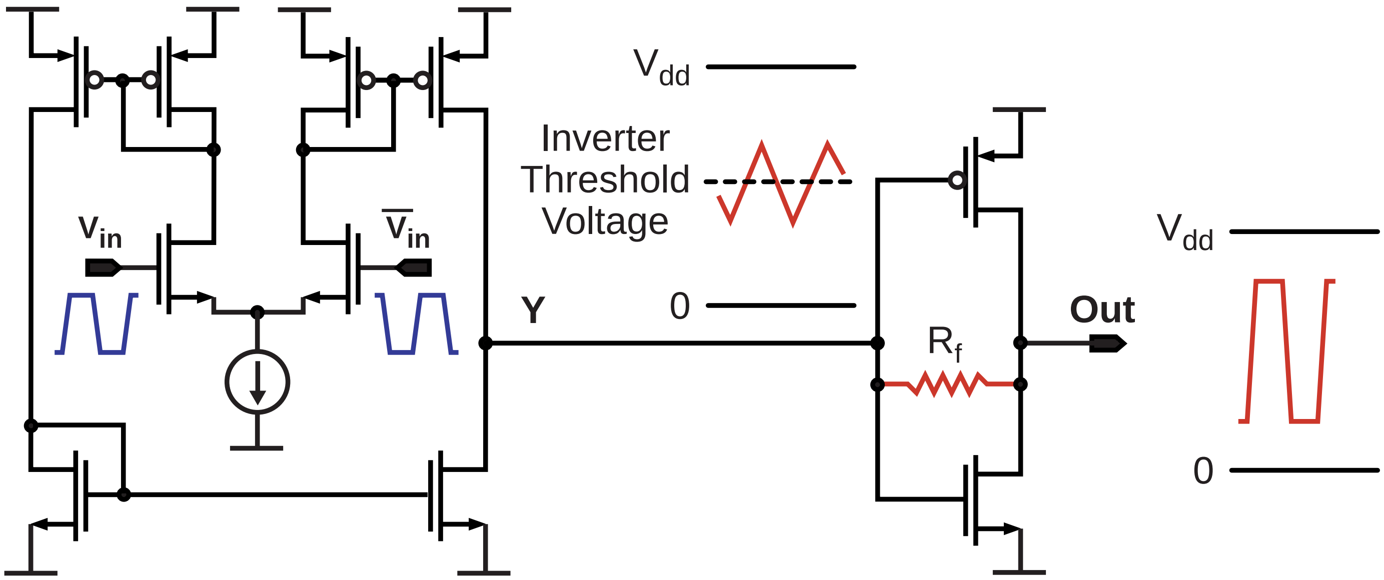
- **Use an opamp style circuit to translate differential input voltage to a single-ended output**
- **Use an inverter to amplify the single-ended output to full swing level**

Issue: Architecture Very Sensitive to DC Offset



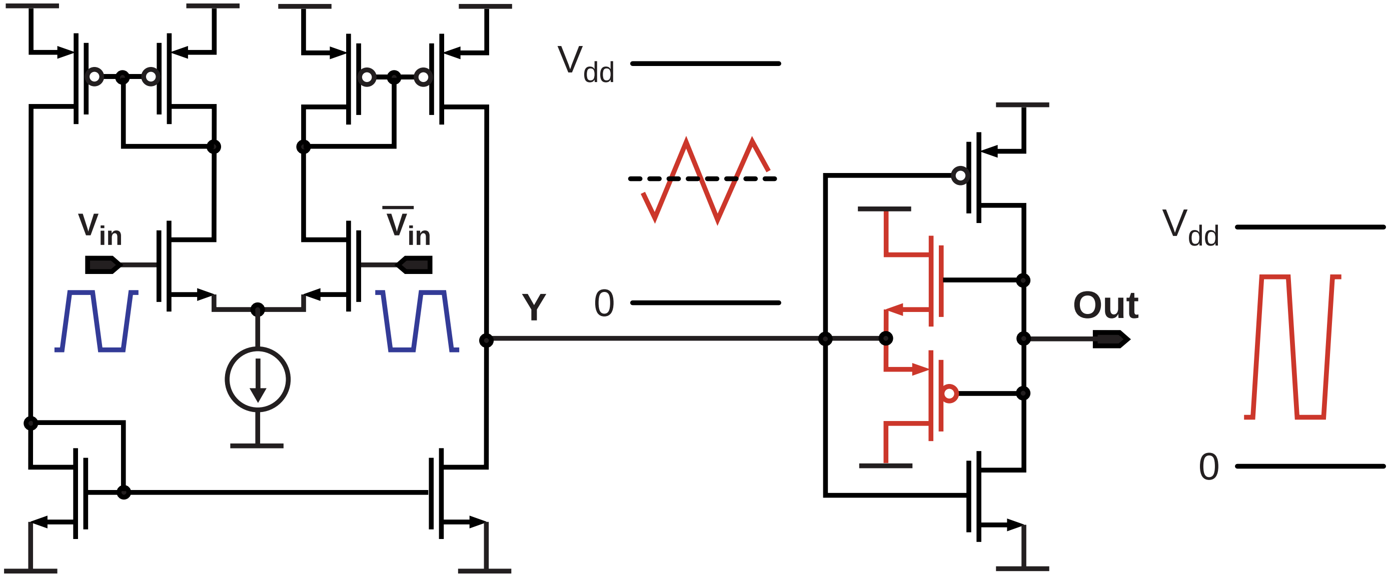
- **Opamp style circuit has very high DC gain from V_{in} to node Y**
- **DC offset will cause signal to rise above or fall below inverter threshold**
  - **Output signal rails rather than pulsing**

Use Resistor Feedback to Reduce DC Gain



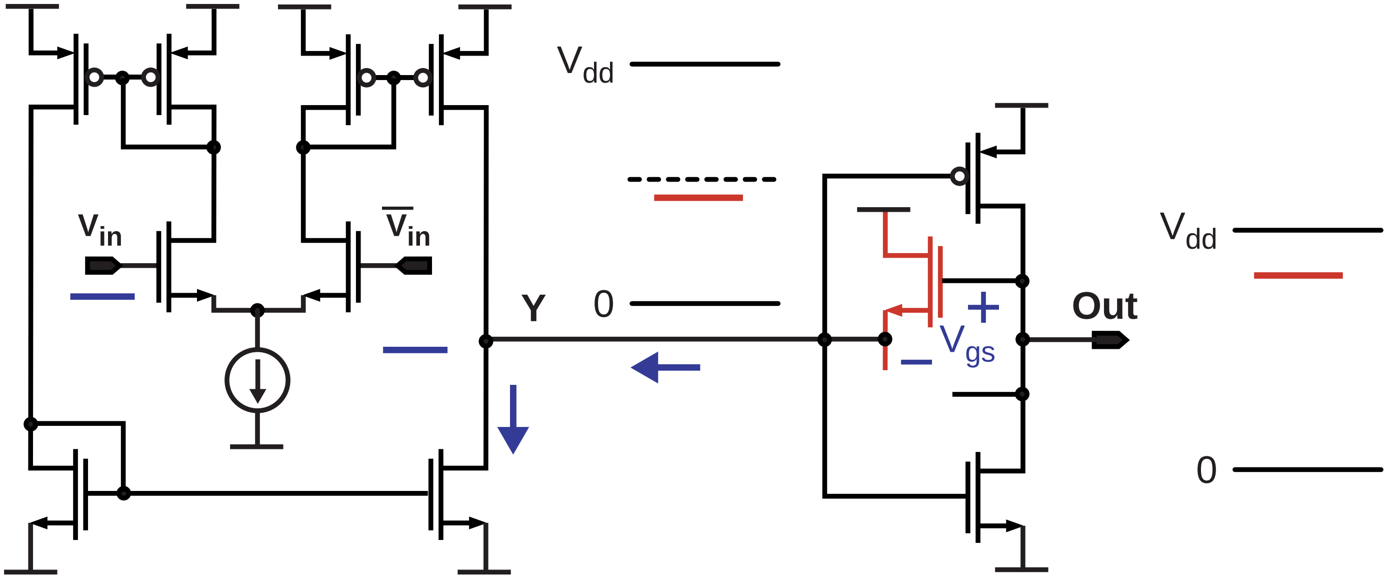
- Idea: create transresistance amplifier rather than voltage amplifier out of inverter by using feedback resistor
  - Presents a low impedance to node Y
  - Current from opamp style circuit is shunted through resistor
  - DC offset at input shifts output waveform slightly, but not node Y (to first order)
- Circuit is robust against DC offset!

Alternate Implementation of Inverter Feedback



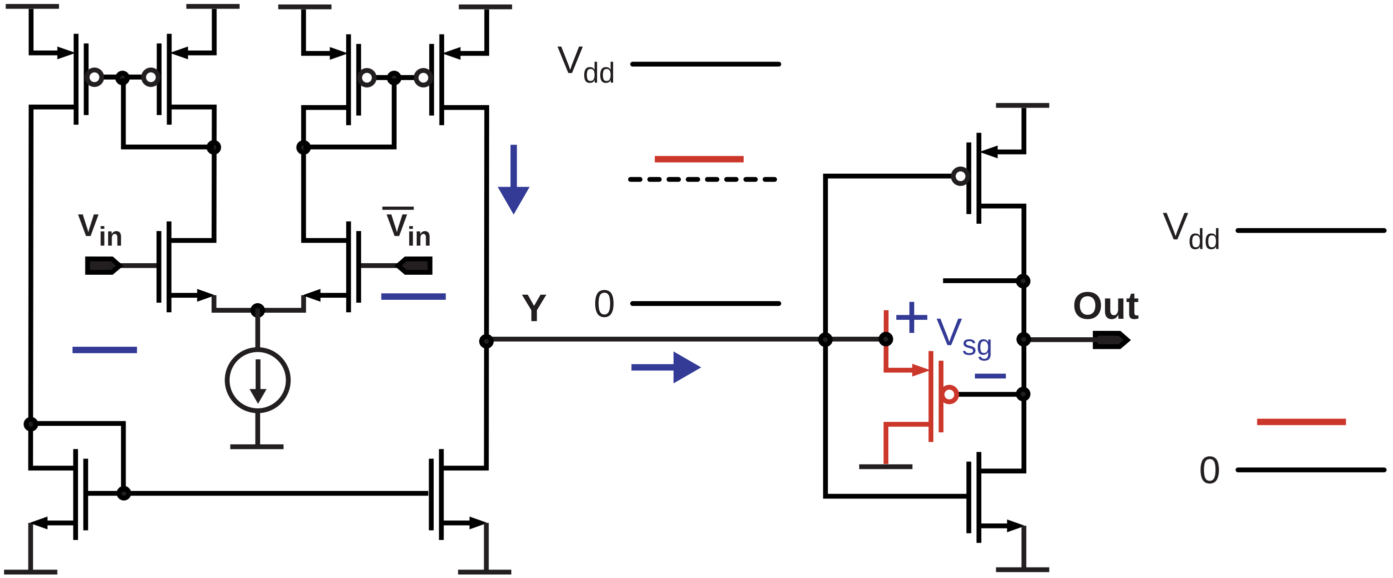
- Nonlinear feedback using MOS devices can be used in place of resistor
  - Smaller area than resistor implementation
- Analysis done by examining impact of feedback when output is high or low

Impact of Nonlinear Feedback When Output is High



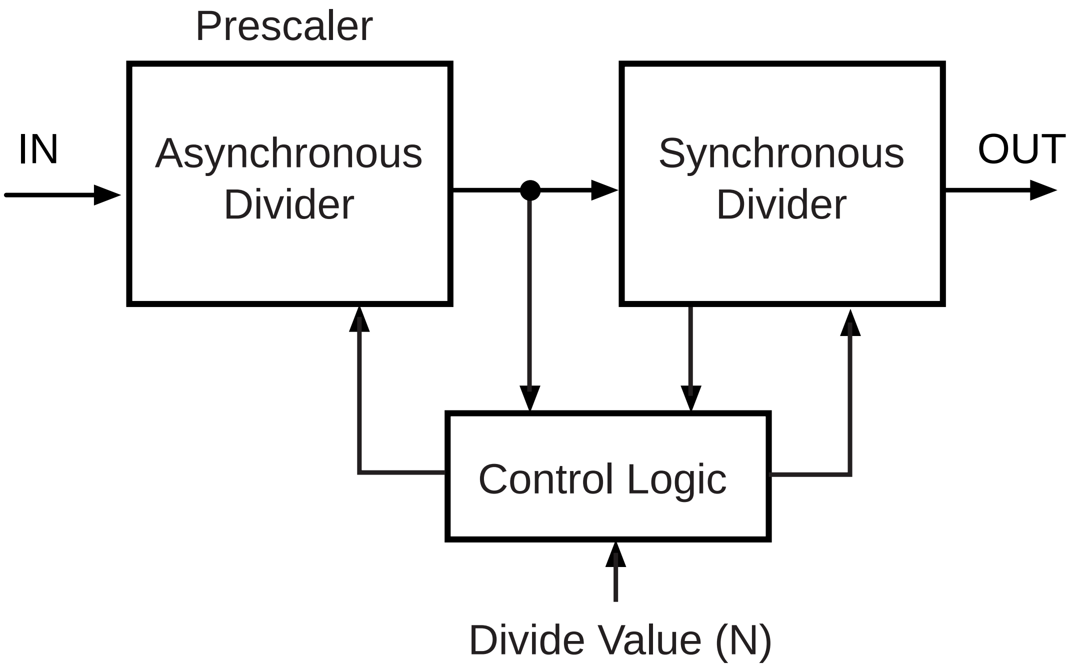
- **Corresponds to case where current flows into node Y**
  - **NMOS device acts like source follower**
  - **PMOS device is shut off**
- **Output is approximately set to V_{gs} of NMOS feedback device away from inverter threshold voltage**
  - **Inverter input is set to a value that yields that output voltage**
    - High DC gain of inverter insures it is close to inverter threshold

Impact of Nonlinear Feedback When Output is Low



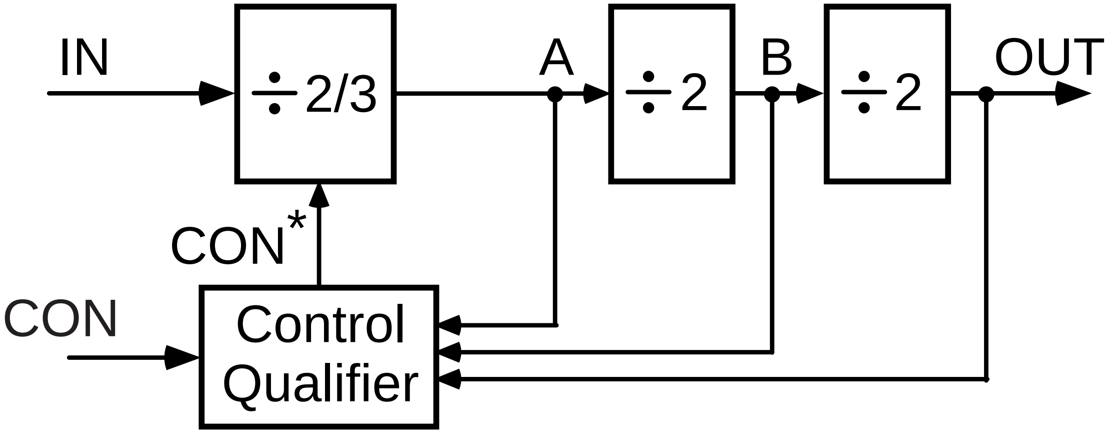
- Corresponds to case where current flows out of node Y
    - NMOS device is shut off
    - PMOS device acts like source follower
- Output is approximately set to Vgs of PMOS feedback device away from inverter threshold voltage
    - Inverter input is set to a value that yields that output voltage
        - High DC gain of inverter insures it is close to inverter threshold

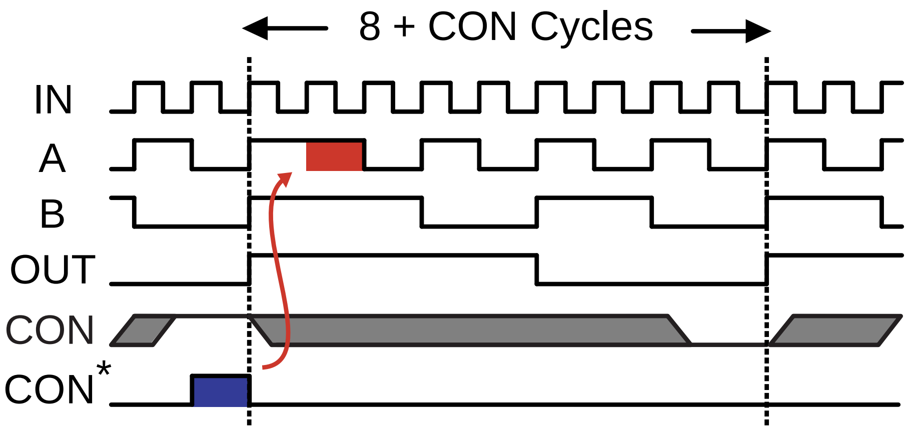
Variable Frequency Division



- **Classical design partitions variable divider into two sections**
  - **Asynchronous section (called a prescaler) is fast**
    - Often supports a limited range of divide values
  - **Synchronous section has no jitter accumulation and a wide range of divide values**
  - **Control logic coordinates sections to produce a wide range of divide values**

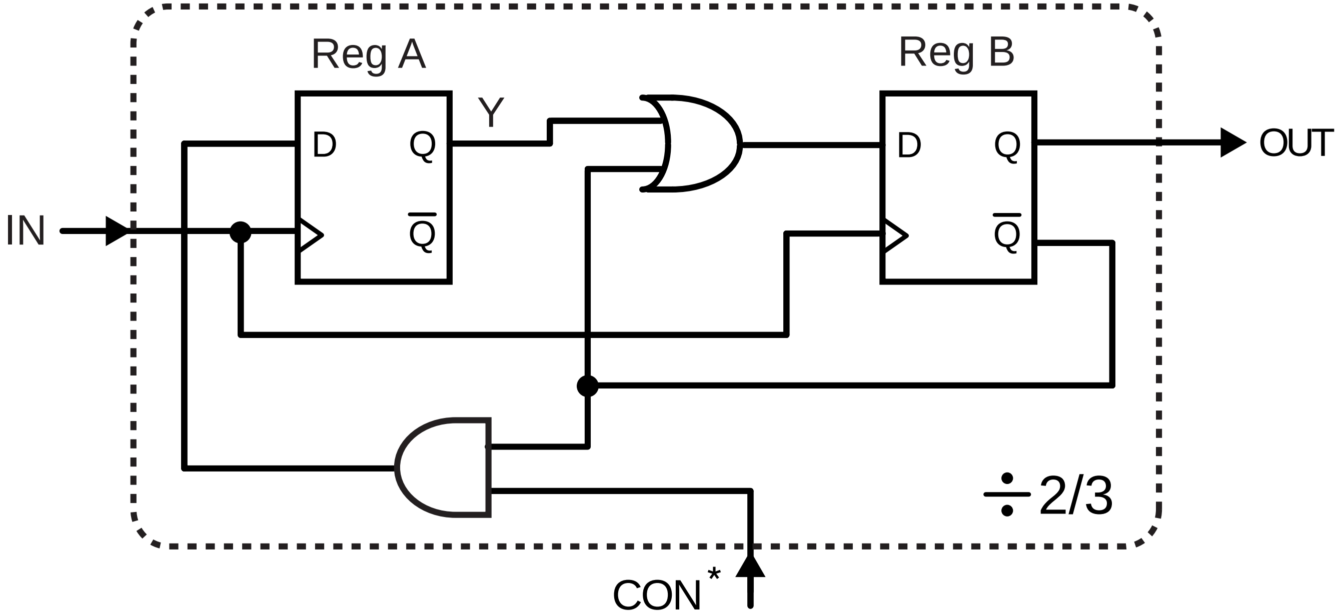
Dual Modulus Prescalers





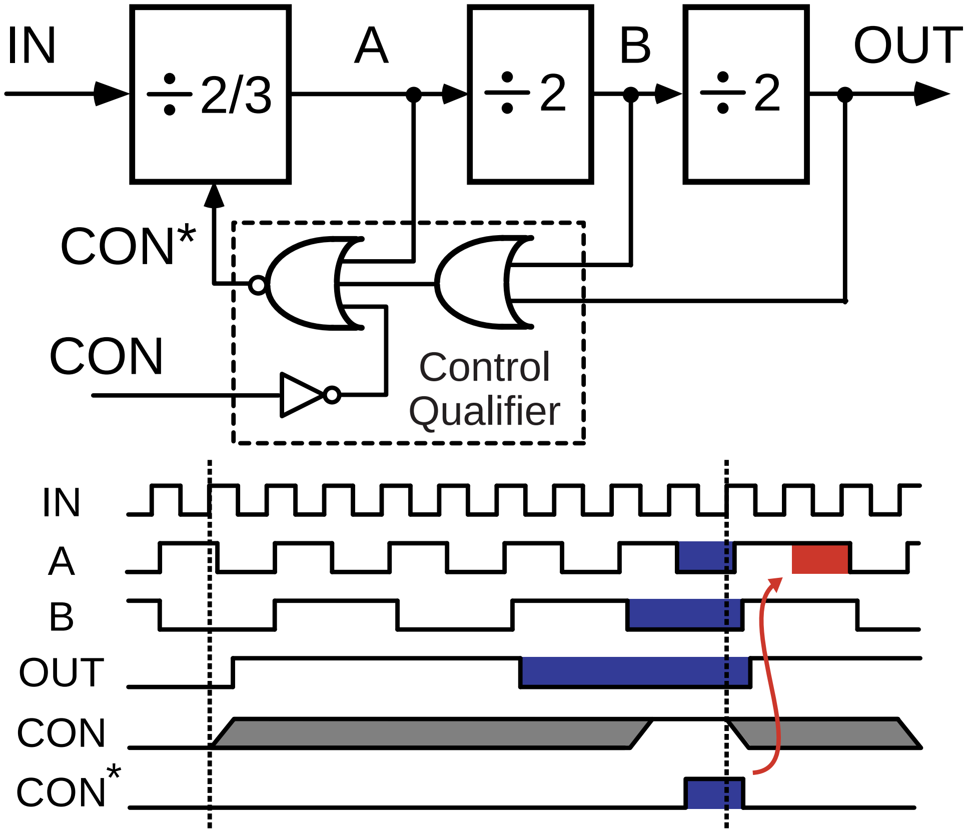
- **Dual modulus design supports two divide values**
  - **In this case, divide-by-8 or 9 according to CON signal**
- **One cycle resolution achieved with front-end “2/3” divider**

Divide-by-2/3 Design (Classical Approach)



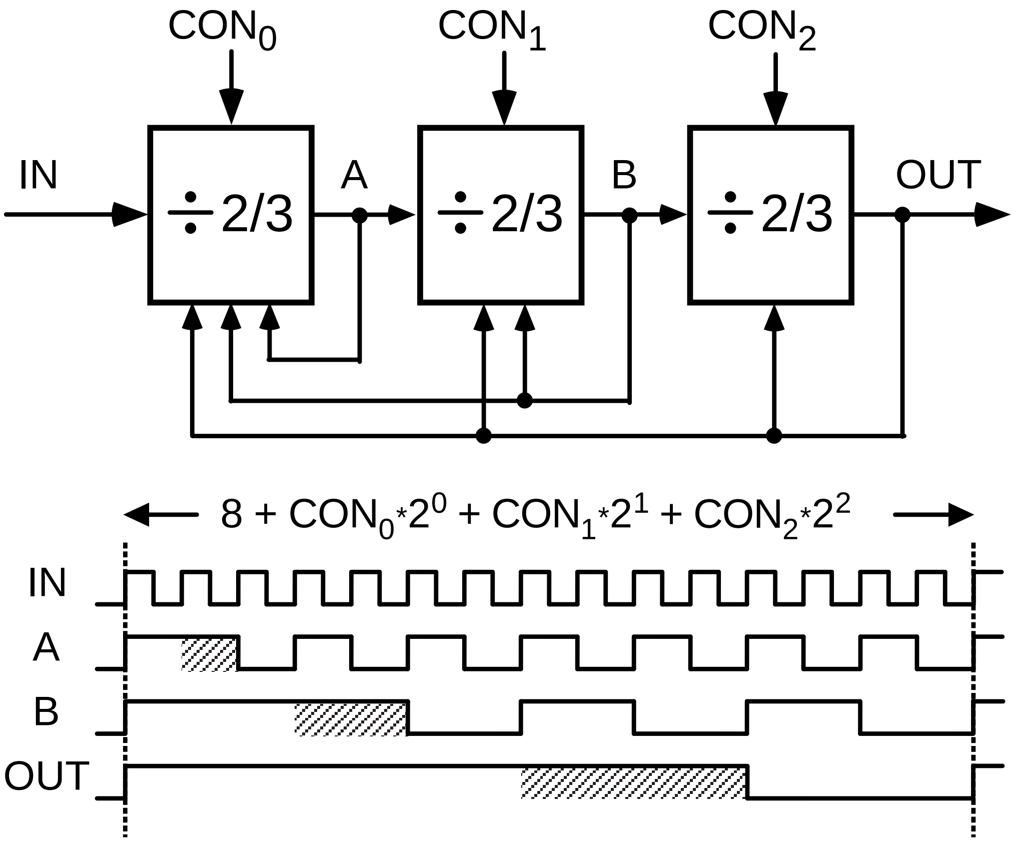
- **Normal mode of operation: CON* = 0 ⇒ Y = 0**
  - **Register B acts as divide-by-2 circuit**
- **Divide-by-3 operation: CON* = 1 ⇒ Y = 1**
  - **Reg B remains high for an extra cycle**
    - Causes Y to be set back to 0 ⇒ Reg B toggles again
    - CON* must be set back to 0 before Reg B toggles to prevent extra pulses from being swallowed

Control Qualifier Design (Classical Approach)



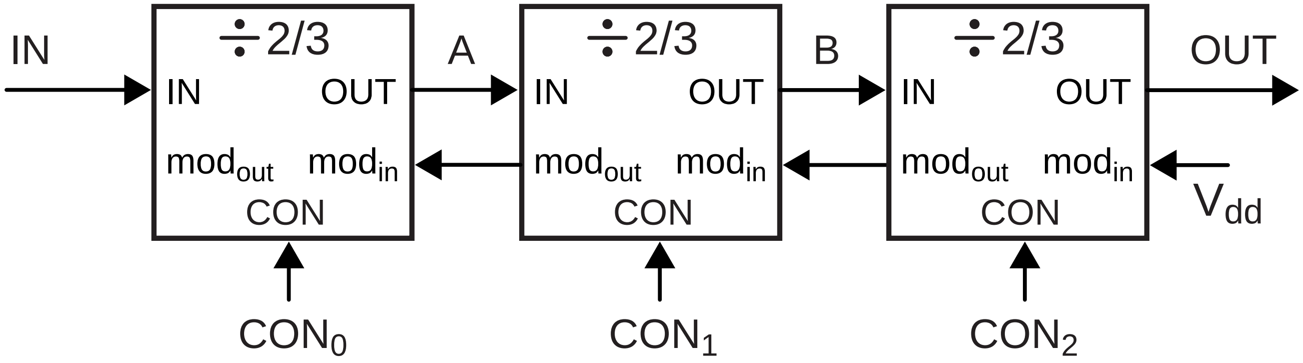
- **Must align CON signal to first "2/3" divider stage**
  - **CON signal is based on logic clocked by divider output**
    - There will be skew between "2/3" divider timing and CON
- **Classical approach cleverly utilizes outputs from each section to "gate" the CON signal to "2/3" divider**

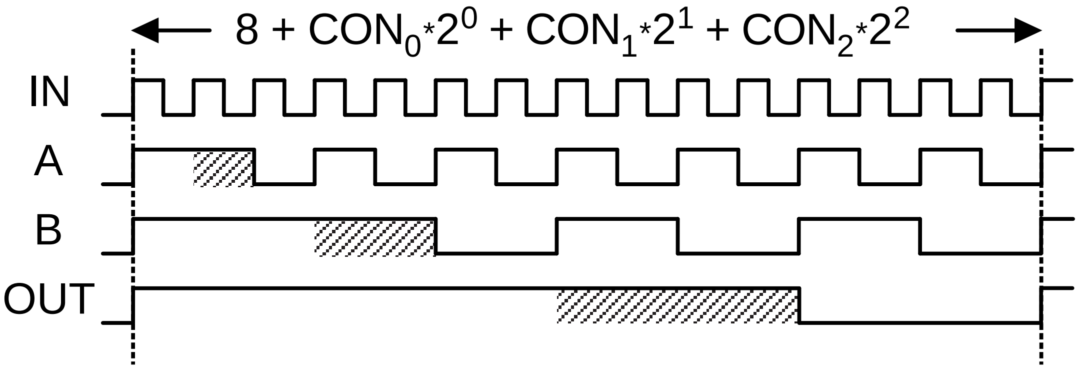
Multi-Modulus Prescalers



- **Cascaded 2/3 sections achieves a range of 2^n to 2^{n+1}-1**
  - **Above example is 8/ ··· /15 divider**
- **Asynchronous design allows high speed and low power operation to be achieved**
  - **Only negative is jitter accumulation**

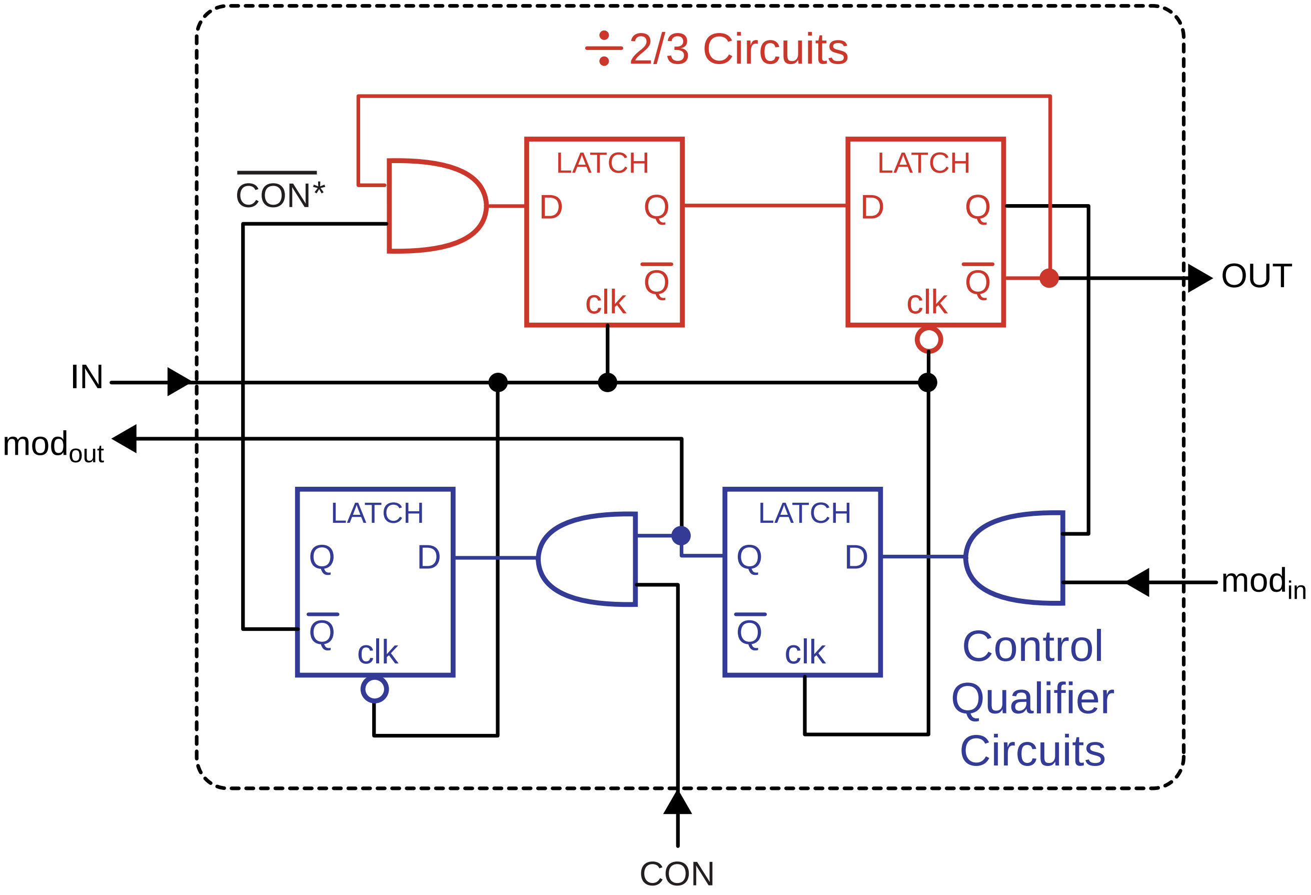
A More Modular Design





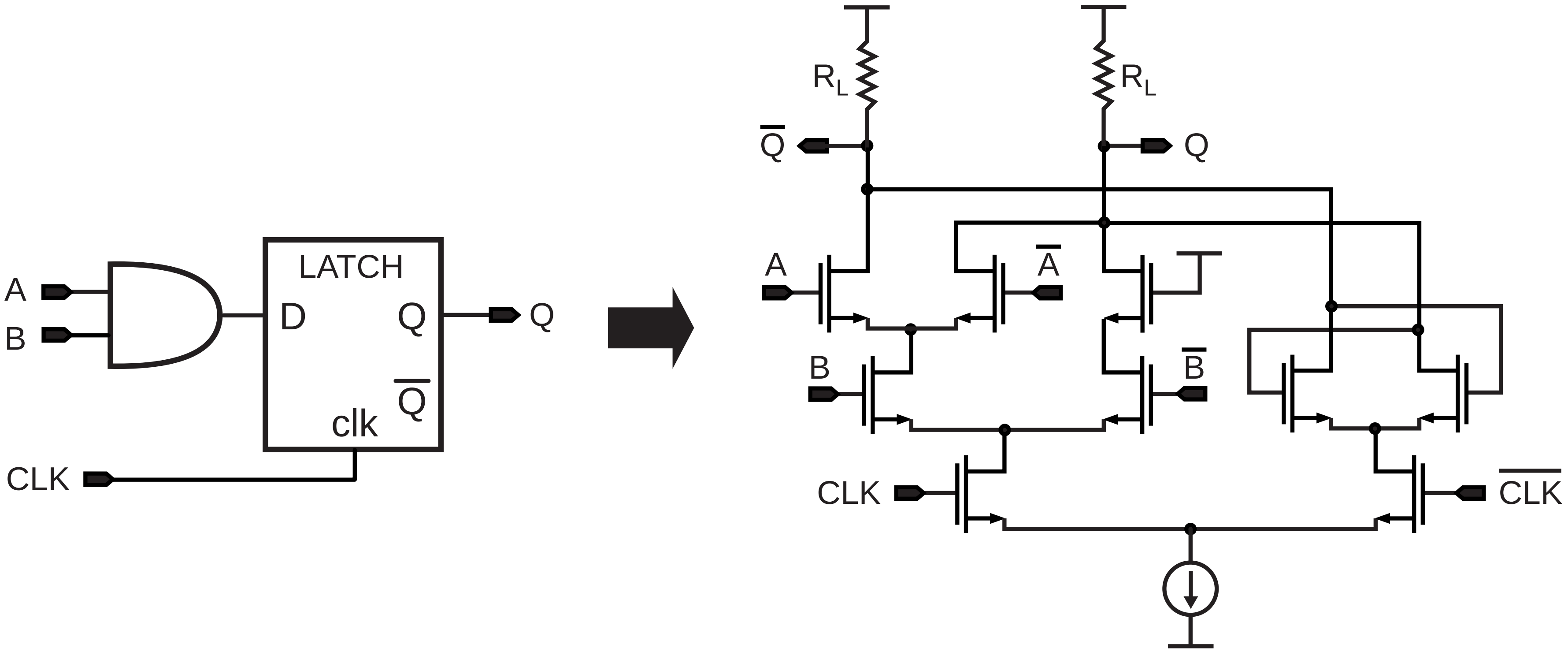
- **Perform control qualification by synchronizing within each stage before passing to previous one**
  - **Compare to previous slide in which all outputs required for qualification of first 2/3 stage**
- **See Vaucher et. al., "A Family of Low-Power Truly Modular Programmable Dividers …", JSSC, July 2000**

Implementation of 2/3 Sections in Modular Approach



- **Approach has similar complexity to classical design**
  - **Consists of two registers with accompanying logic gates**
- **Cleverly utilizes “gating” register to pass synchronized control qualifying signal to the previous stage**

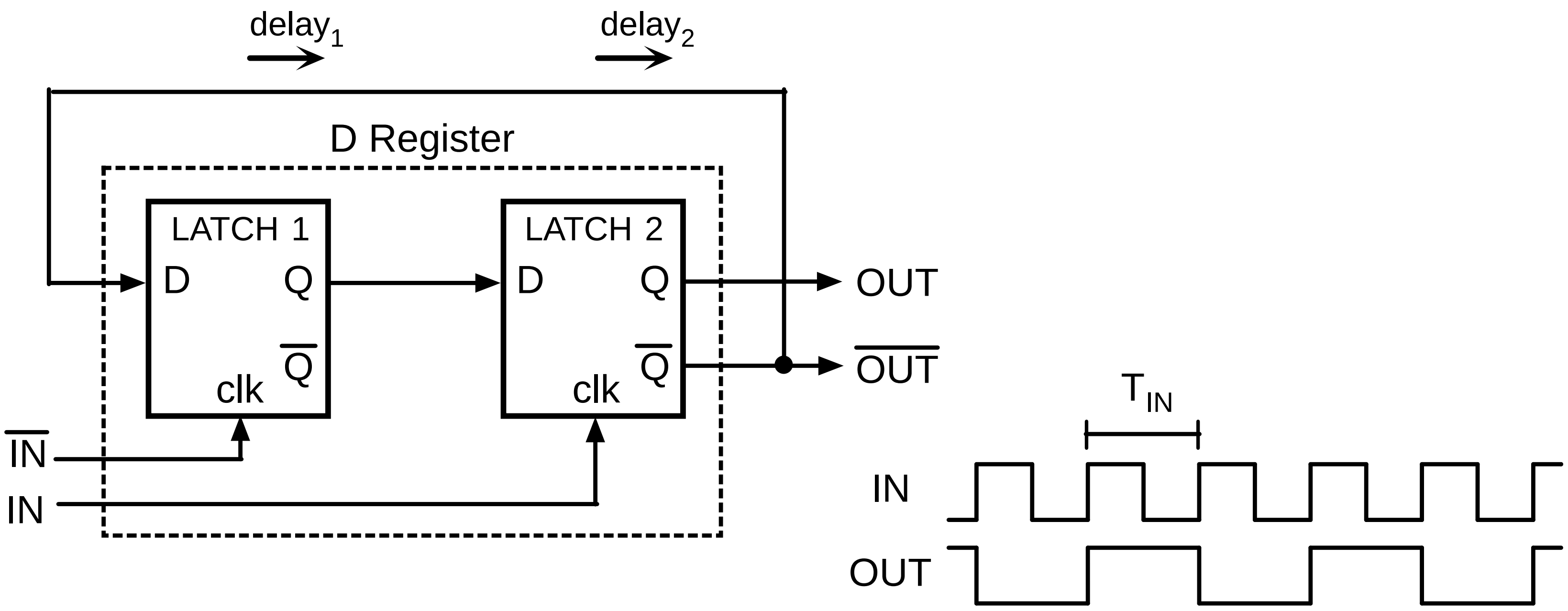
Implementation of Latch and And Gate in 2/3 Section



- **Combine AND gate and latch for faster speed and lower power dissipation**
- **Note that all primitives in 2/3 Section on previous slide consist of this combination or just a straight latch**

Can We Go Even Faster?

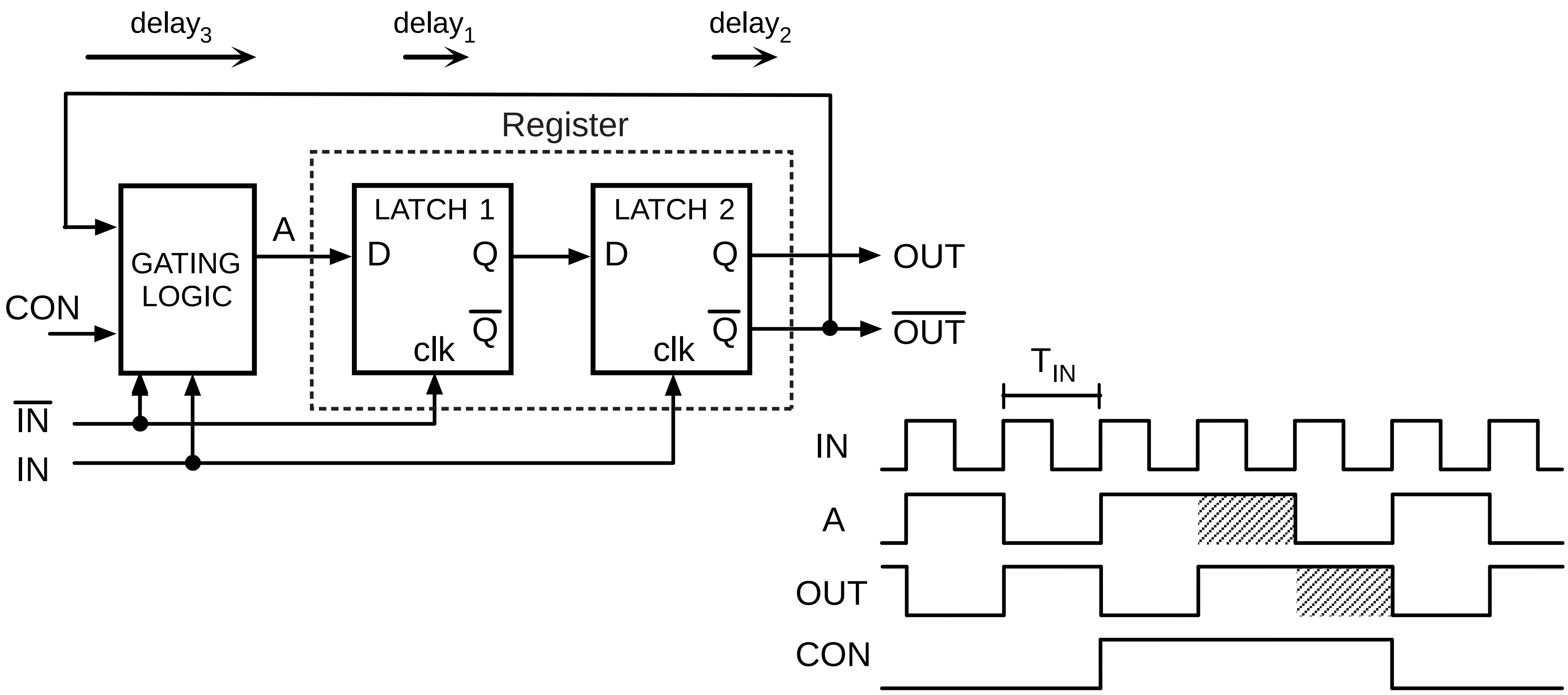
Speed Limitations of Divide-by-2 Circuit



- **Maximum speed limited only by propagation delay (delay$_1$, delay$_2$) of latches and setup time of latches (T_s)**

$$\frac{T_{IN}}{2} > delay_1 + T_s, \quad \frac{T_{IN}}{2} > delay_2 + T_s$$

Speed Limitations of Gated Divide-by-2/3 Circuit

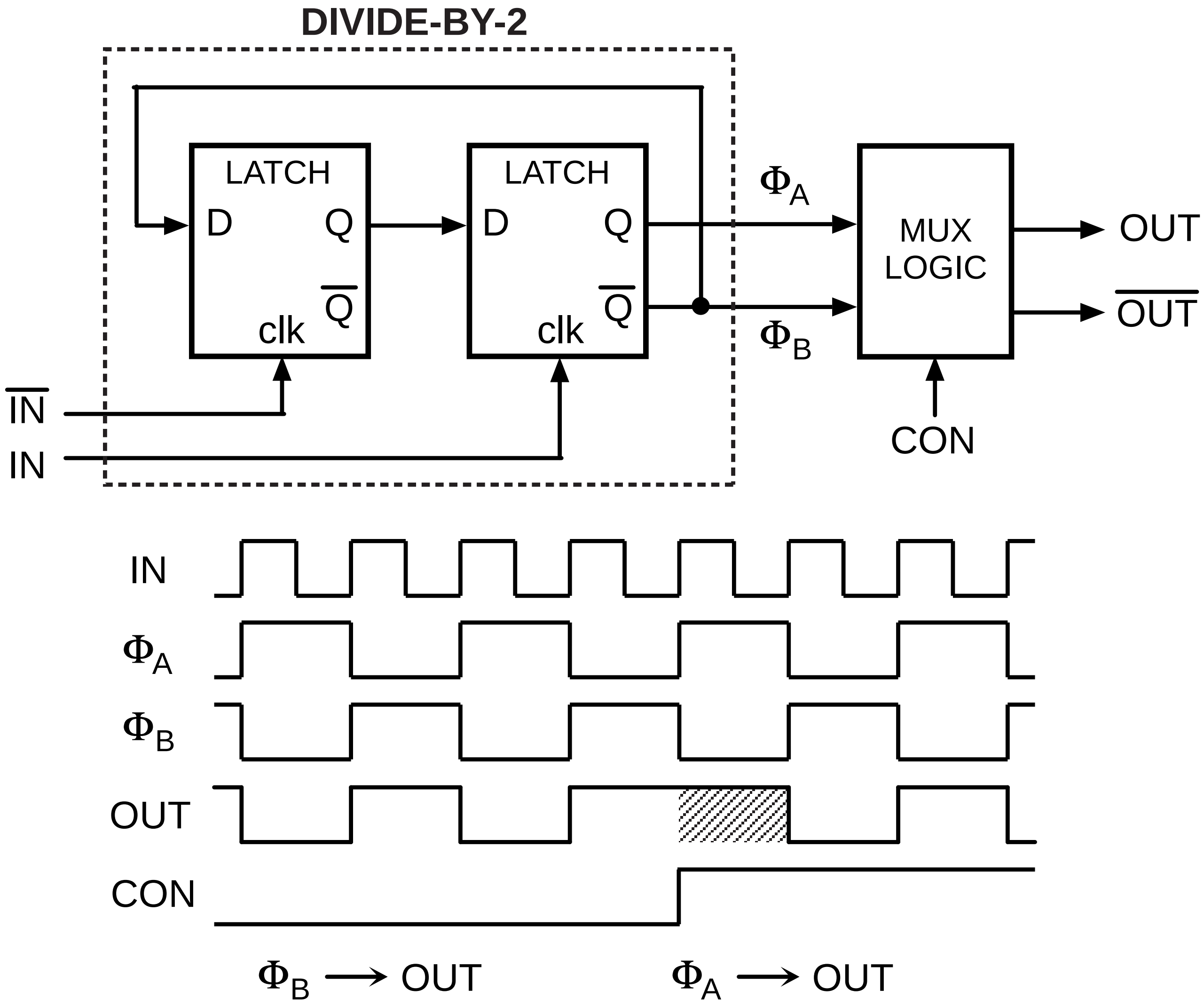


- **Maximum speed limited by latch *plus* gating logic**

$$\frac{T_{IN}}{2} > delay_2 + delay_3 + T_s$$

- **Gated divide-by-2/3 *fundamentally* slower than divide-by-2**

Divide-by-2/3 Using Phase Shifting



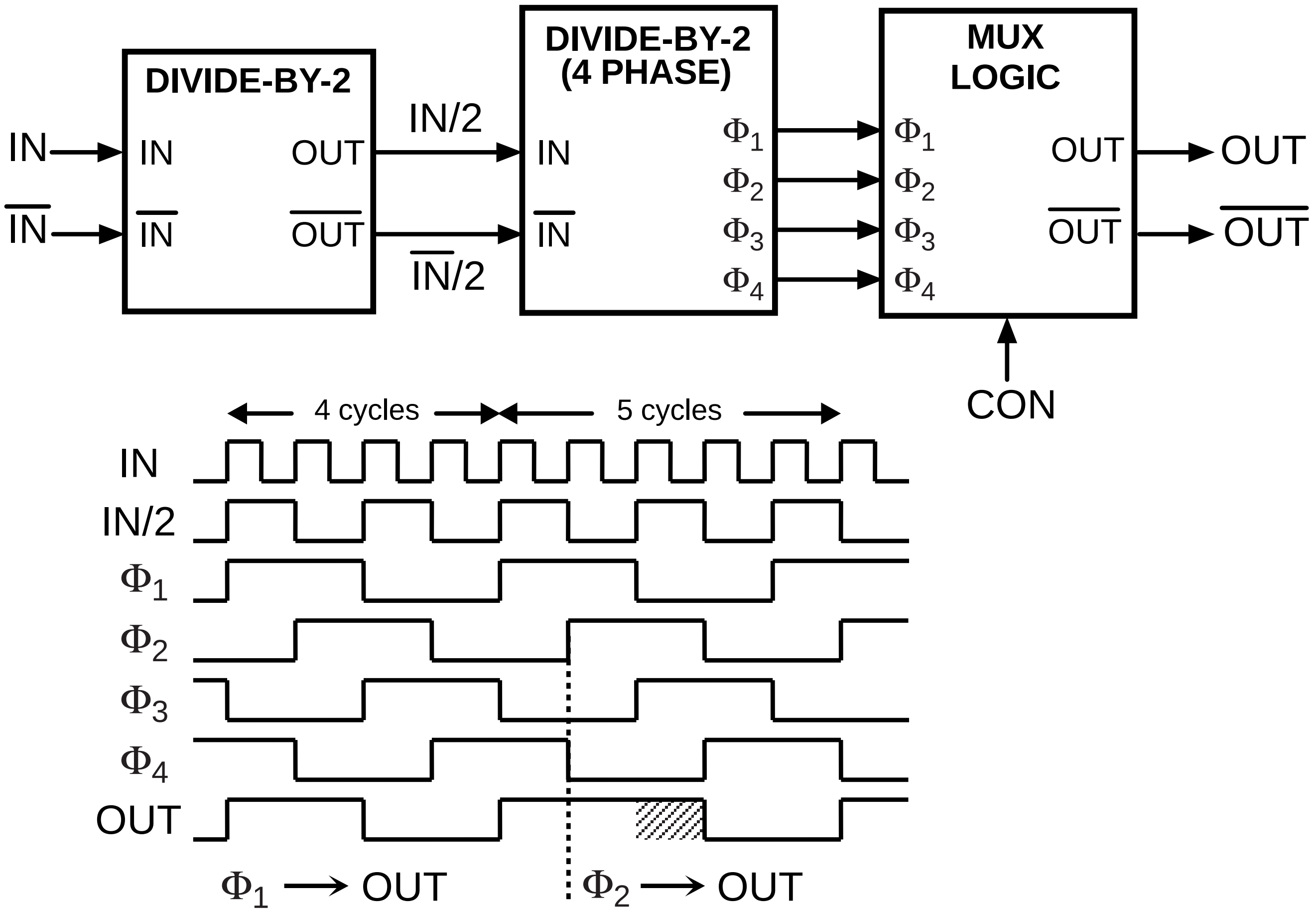
- **Achieves speed of divide-by-2 circuits!**
  - **MUX logic runs at half the input clock speed**

Implementation Challenges to Phase Shifting

- **Avoiding glitches**
  - **By assumption of sine wave characteristics**
    - Craninckx et. al., “A 1.75 GHz/3 V Dual-Modulus Divide-by-128/129 Prescaler …”, JSSC, July 1996
  - **By make-before-break switching**
    - My thesis: http://www-mtl.mit.edu/~perrott/
  - **Through re-timed multiplexor**
    - Krishnapura et. al, “A 5.3 GHz Programmable Divider for HiPerLan in 0.25μm CMOS”, JSSC, July 2000

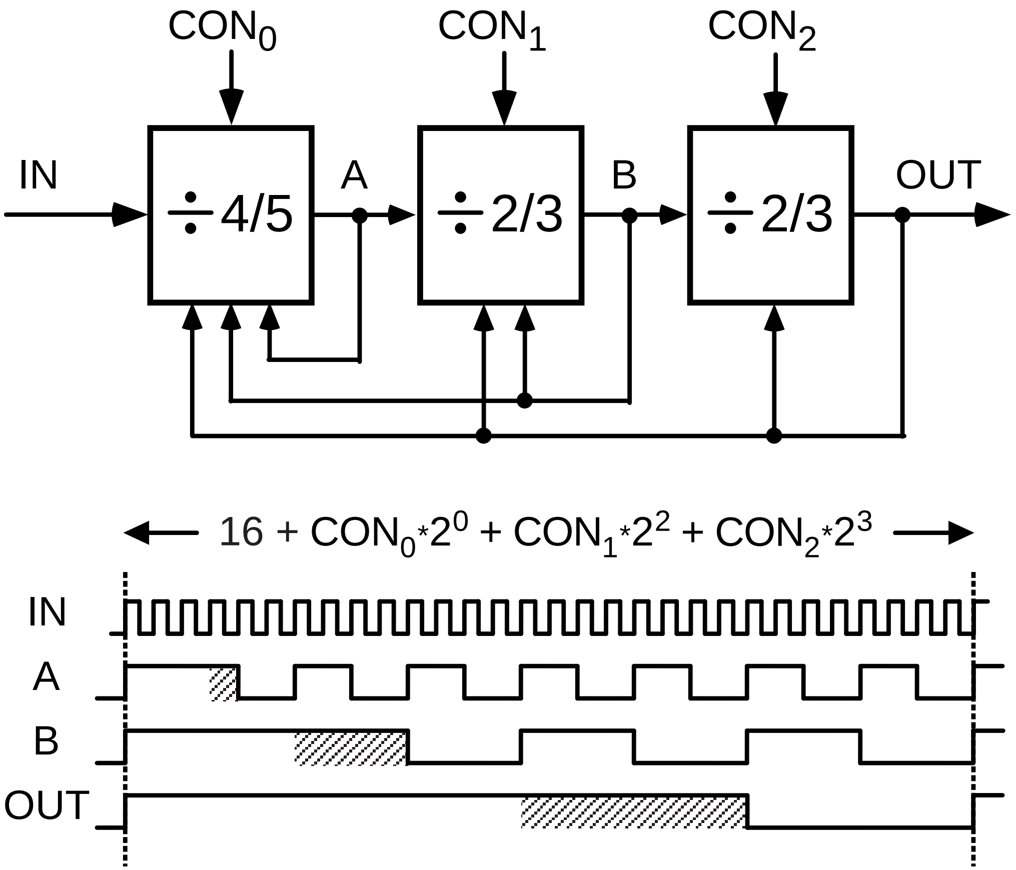
- **Avoiding jitter due to mismatch in phases**
  - **Through calibration**
    - Park et. al., “A 1.8-GHz Self-Calibrated Phase-Locked Loop with Precise I/Q Matching”, JSSC, May 2001

Further Reduction of MUX Operating Frequency



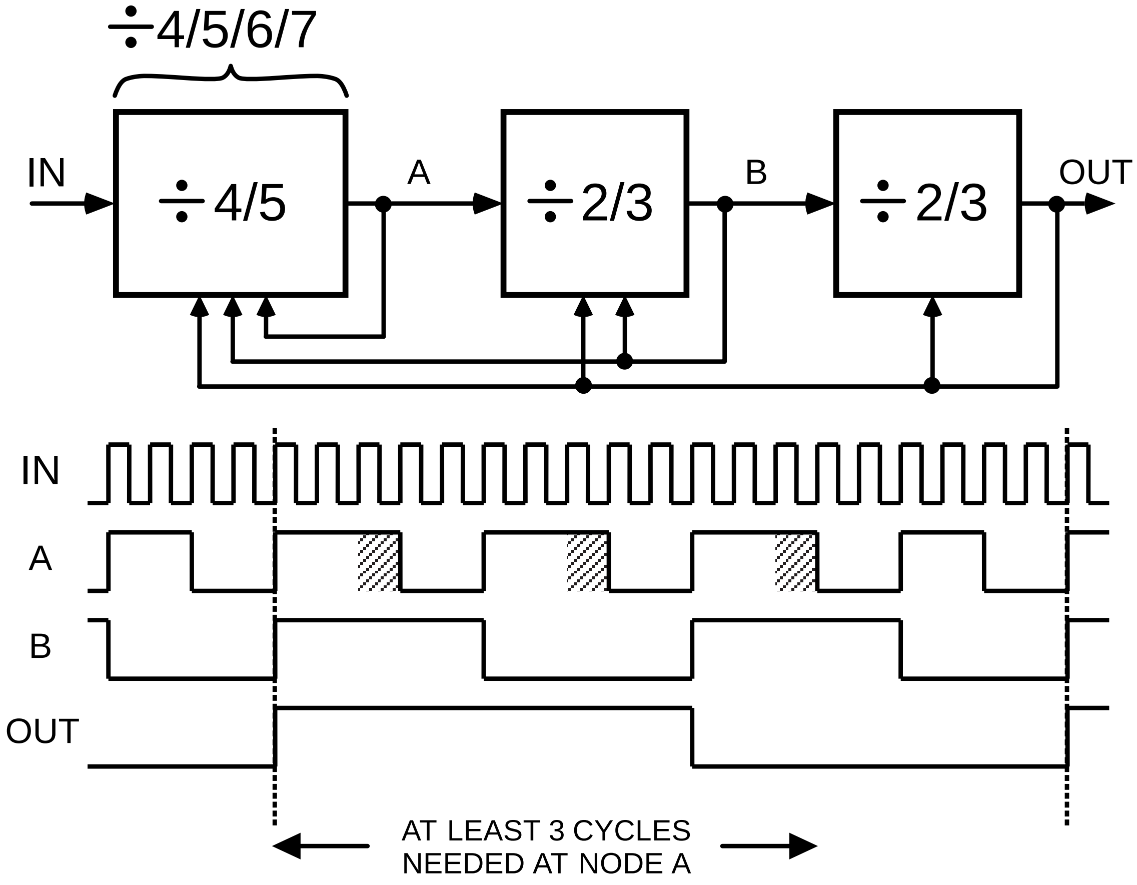
- **Leverage the fact that divide-by-2 circuit has 4 phases**
  - **Create divide-by-4/5 by cascading *two* divide-by-2 circuits**
    - Note that single cycle pulse swallowing still achieved
  - **Mux operates at one fourth the input frequency!**

Impact of Divide-by-4/5 in Multi-Modulus Prescaler



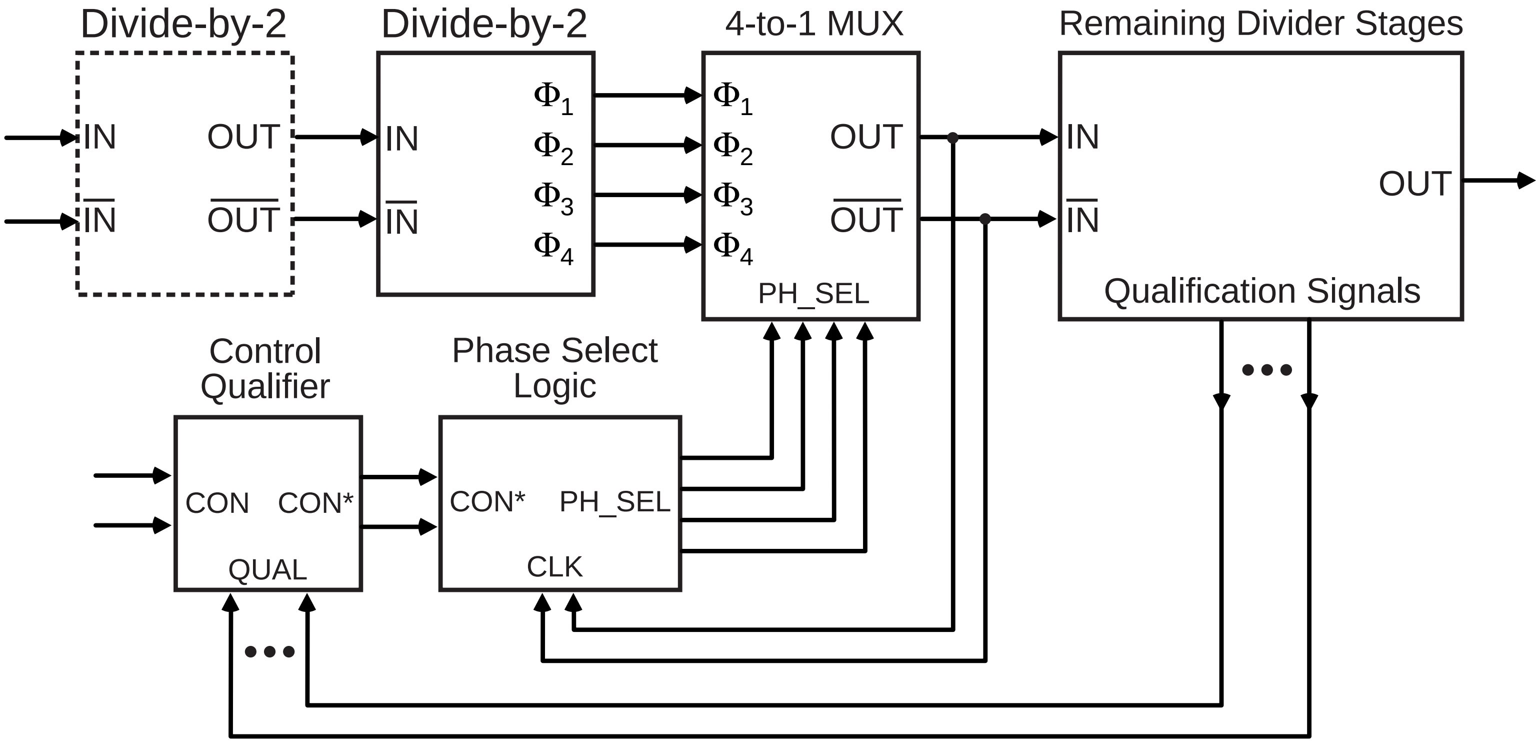
- **Issue – gaps are created in divide value range**
  - **Divide-by-4/5 lowers swallowing resolution of following stage**

Method to “Fill In” Divide Value Range



- Allow divide-by-4/5 to swallow more than one input cycle per OUT period
  - Divide-by-4/5 changed to Divide-by-4/5/6/7
- Note: at least two divide-by-2/3 sections must follow

Example Architecture for a Phase-Shifted Divider



- **Phase shifting in first divide-by-4/5/6/7 stage to achieve high speed**
- **Remaining stages correspond to gated divide-by-2/3 cells**
- **For details, see my thesis**
  - **http://www.cppsim.com/michael_h_perrott**