Short Course On
Phase-Locked Loops and Their Applications
Day 5, AM Lecture

Advanced PLL Examples (Part I)
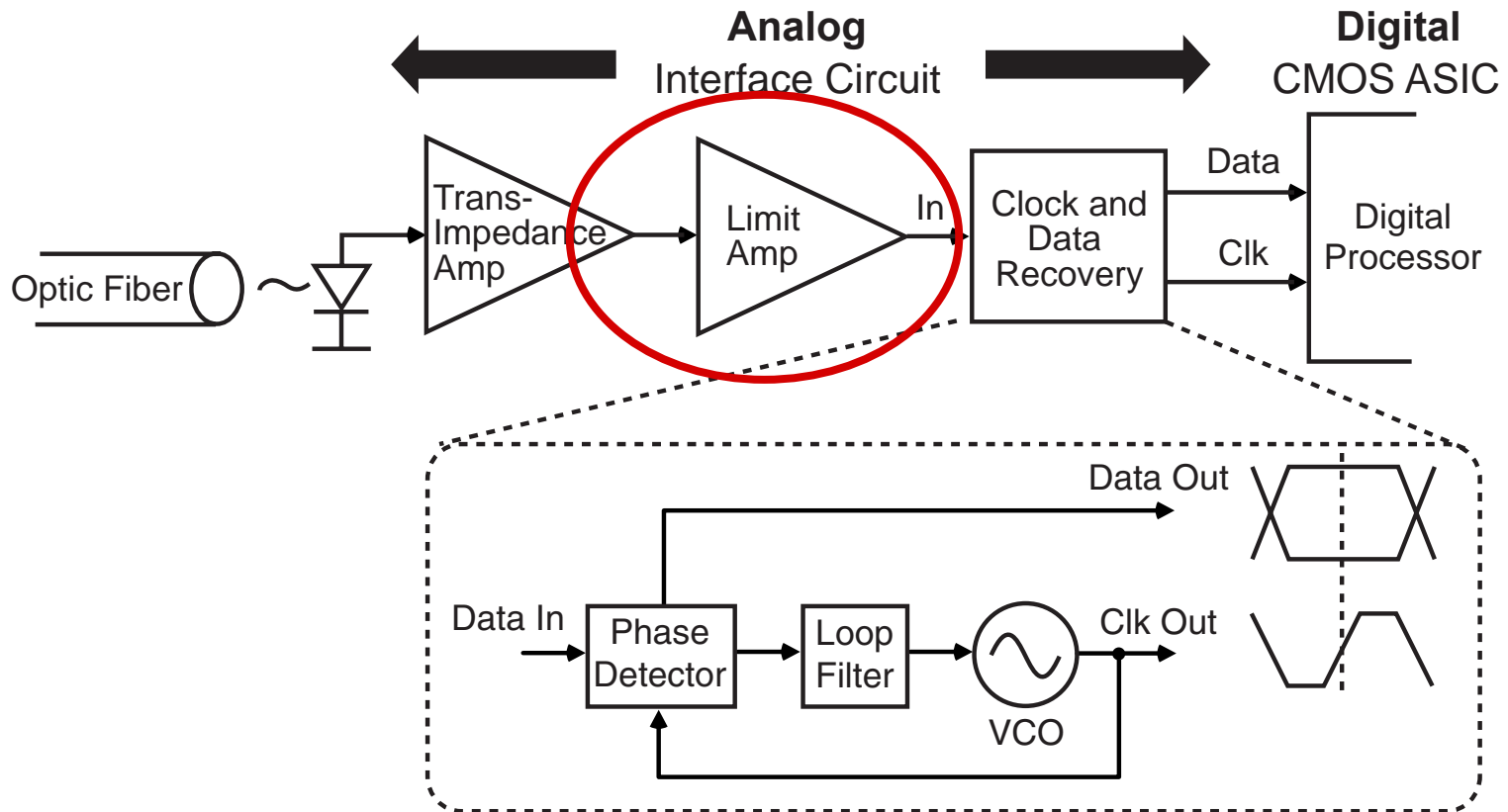
Michael Perrott

August 15, 2008

Outline

- **Fast offset compensation for CDR limit amps**

- **Fractional-N based DLL**

- **Low-jitter multiplying DLL**

- **Sub-harmonic injection-locked oscillator**

# A 3.125 Gb/s Limit Amplifier in CMOS with 42 dB Gain and
1us Offset Compensation

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A Fast Acquisition Limit Amp

Analog
Interface Circuit

Digital
CMOS ASIC

Optic Fiber

Trans-Impedance Amp

Limit Amp   In

Clock and Data Recovery

Data

Clk

Digital Processor

Data Out

Data In → Phase Detector → Loop Filter → VCO → Clk Out
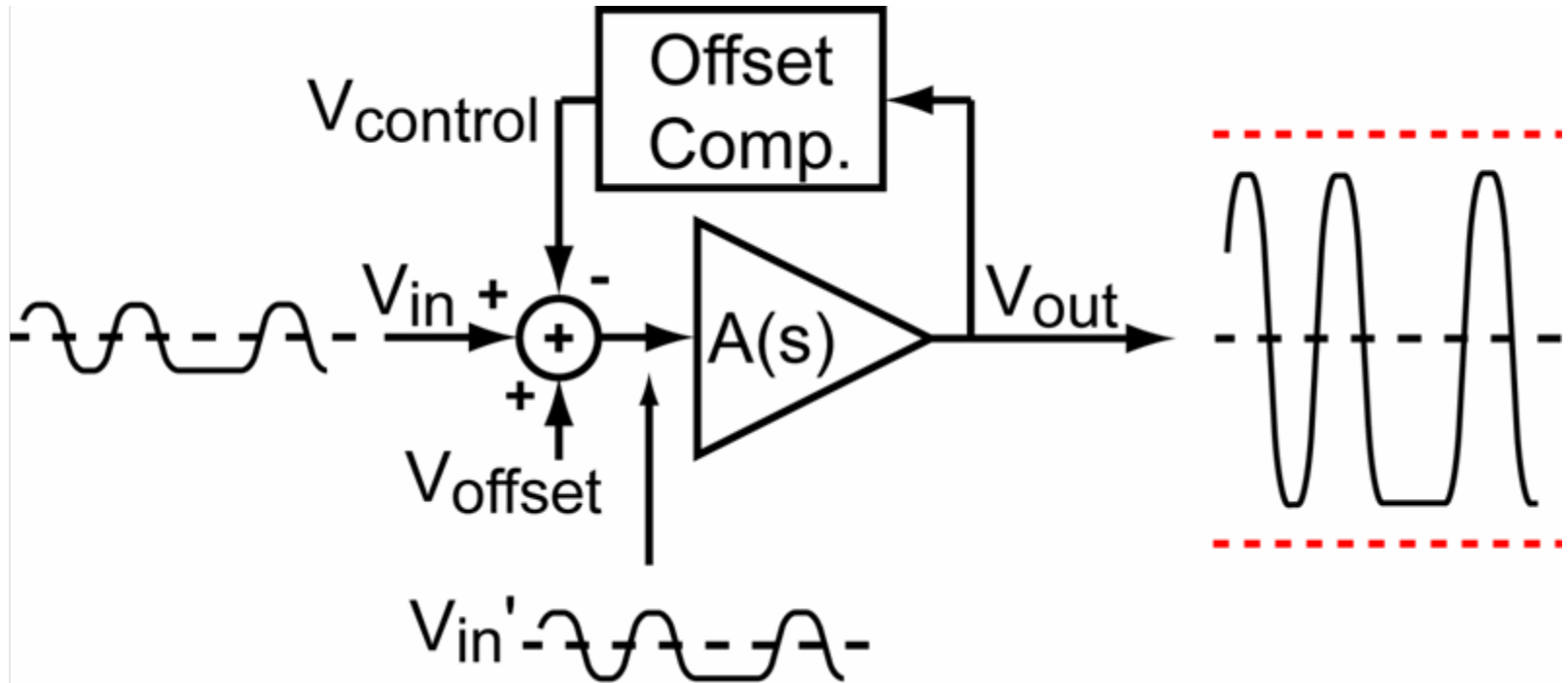
VCO

- **Acquisition time of CDR is limited by slow response of limit amp offset correction loop (typically milliseconds)**
- **Goal: improve speed of offset correction**

Motivation for Offset Compensation
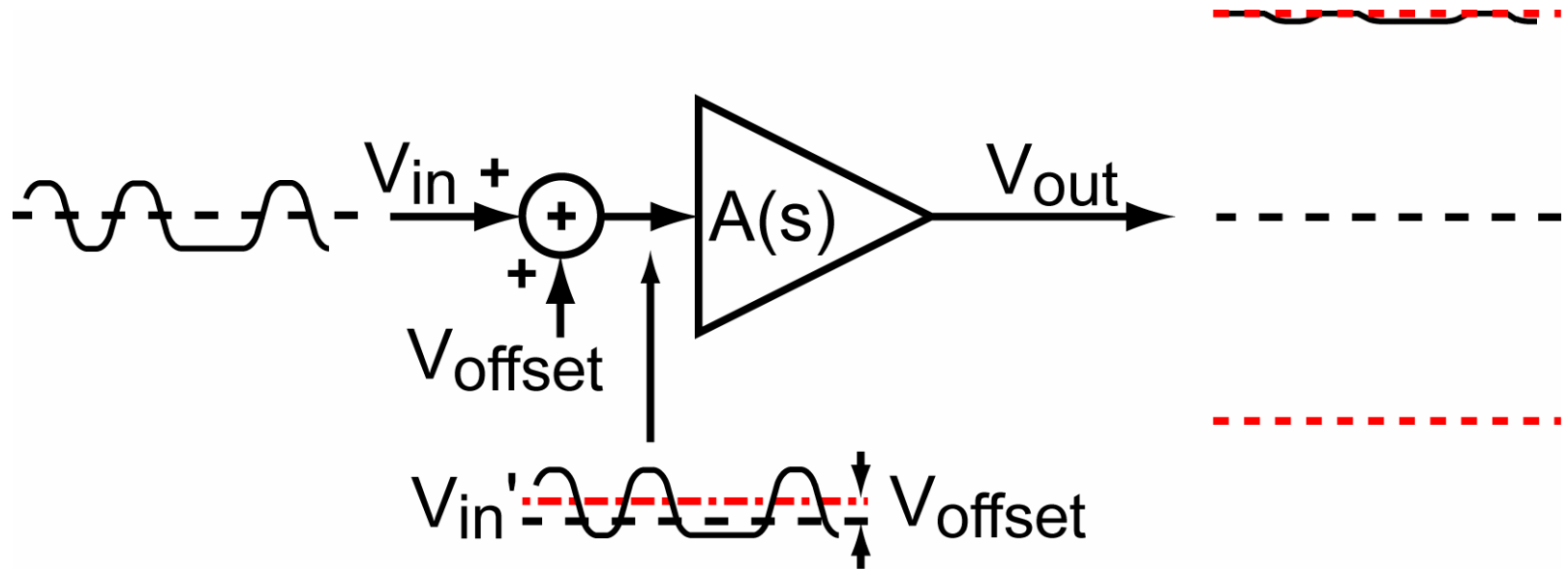
Without offset compensation the output of high gain amplifiers can saturate due to offset voltage alone
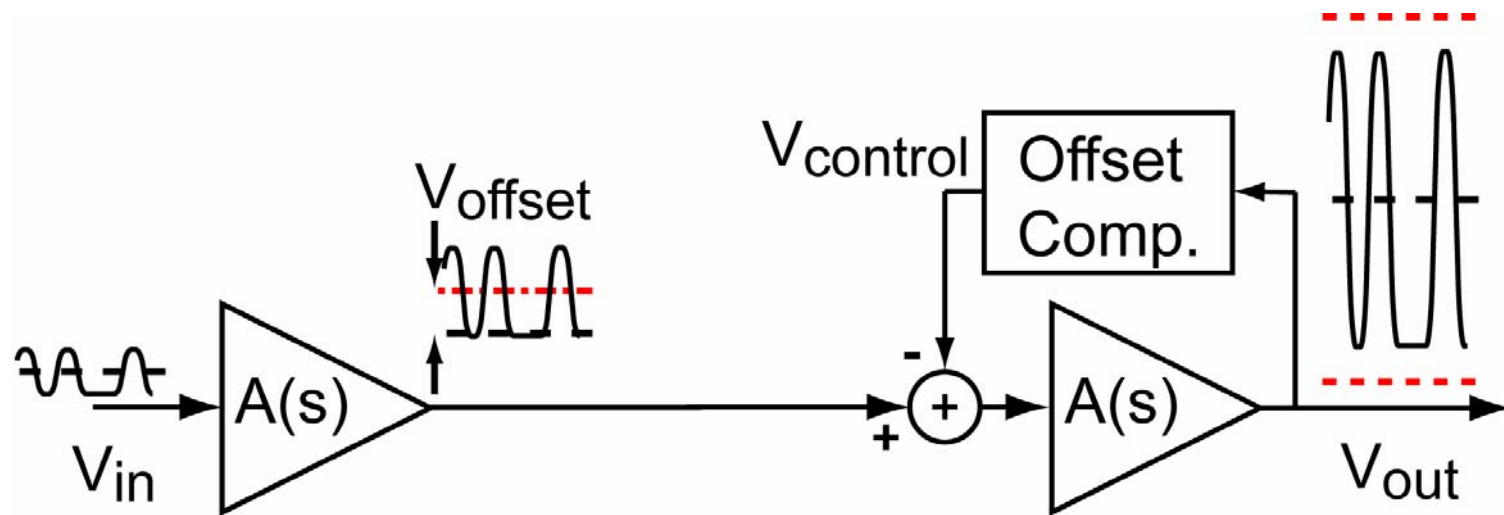
Motivation for Offset Compensation

Offset compensation is required for high gain amplifiers to prevent the output from saturating due to offset
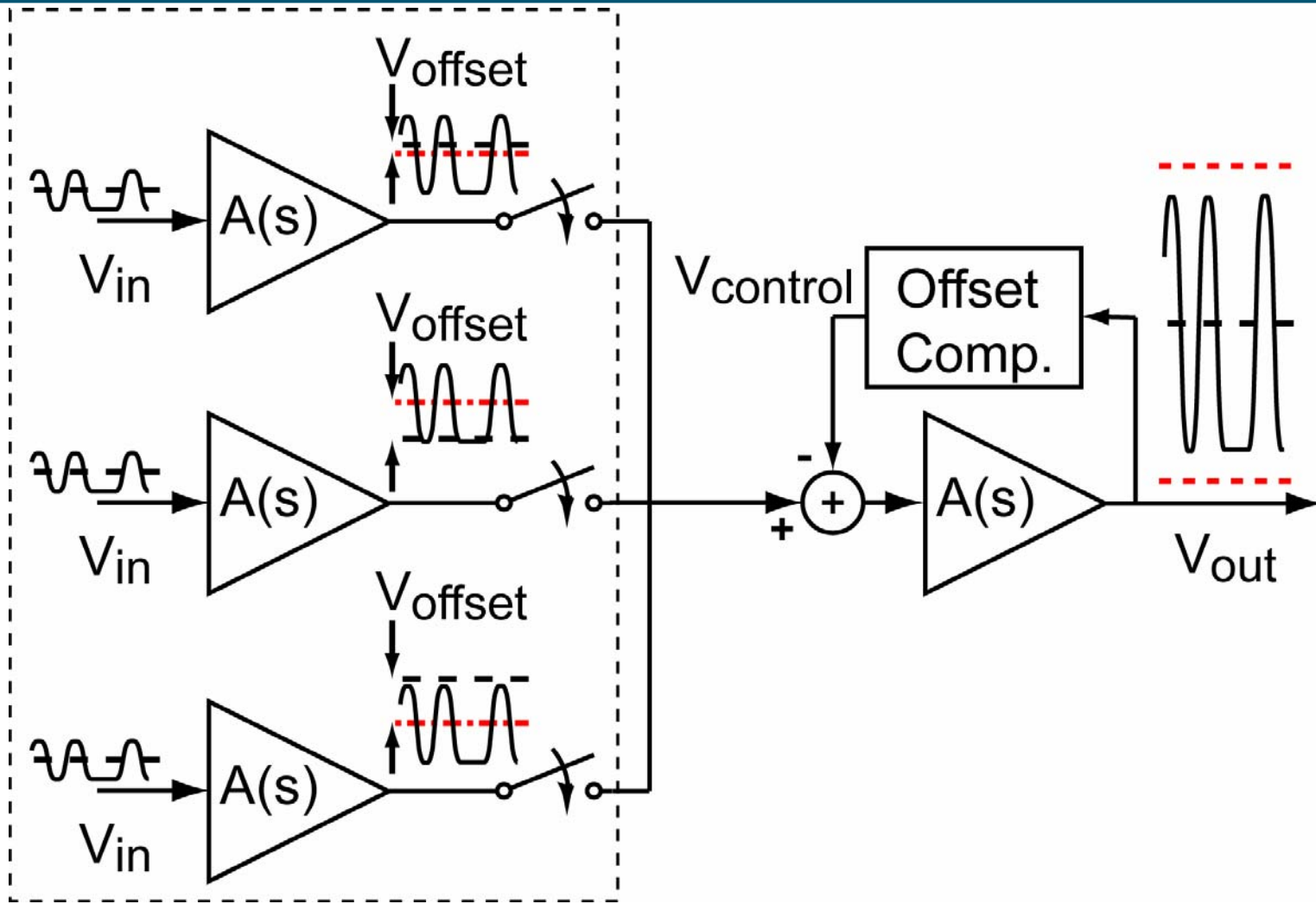
Classical offset compensation methods suffer from long compensation times

Why long settling times matter

Compensation only happens once in one-to-one links
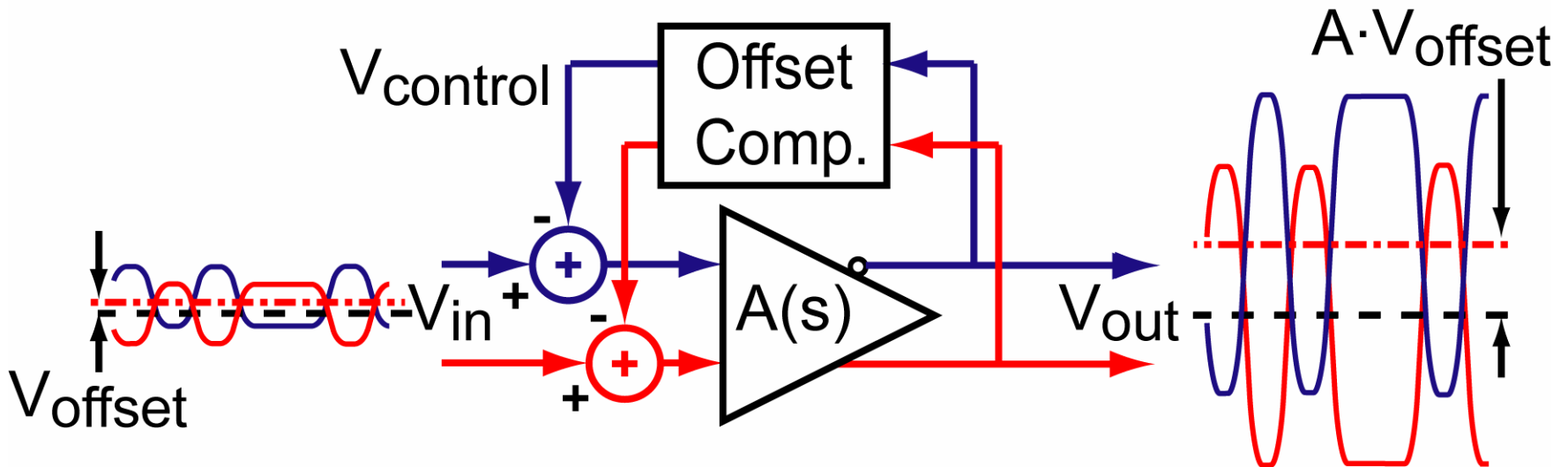Typical offset compensation time $\approx 1 ms$

Why long settling times matter

The compensation time determines how quickly we can switch between channels

Outline

$\Rightarrow$ Proposed method

$\Rightarrow$ Peak detector design

$\Rightarrow$ System Details

$\Rightarrow$ Measured results

$\Rightarrow$ Conclusions

Proposed Method – Key Assumptions

- Assume that the data path is differential and the two data paths have approximately equal gains
- Assume that we are processing NRZ data
- The output-referred offset is equal to the difference in output common-mode levels

Proposed Method – Key Assumptions

$$A \cdot V_{offset} = max[V_+] - max[V_-]$$

Traditional Peak Detector
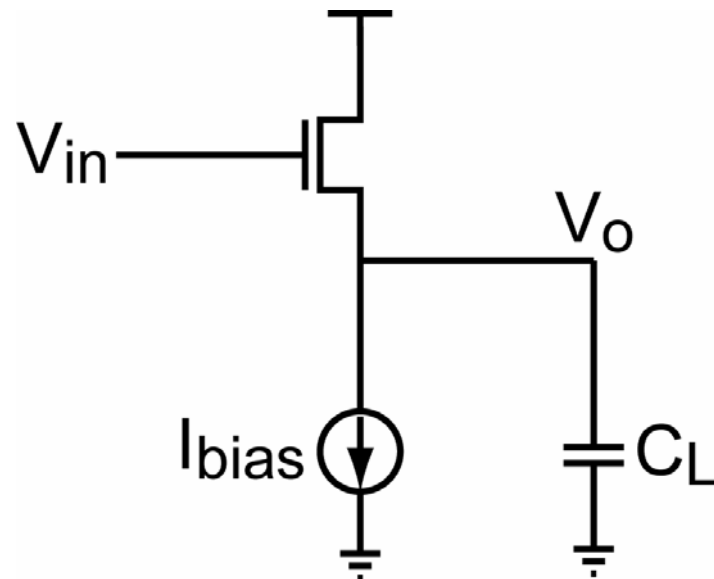
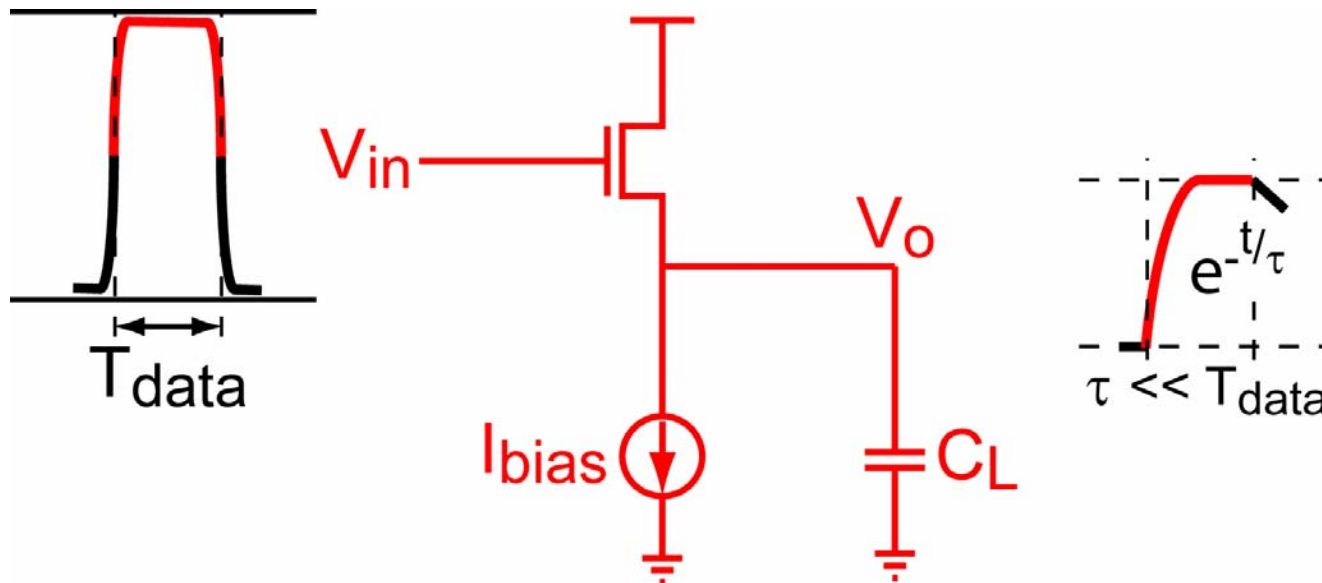
Consider operation of traditional
CMOS peak detector

Operation During Track Phase
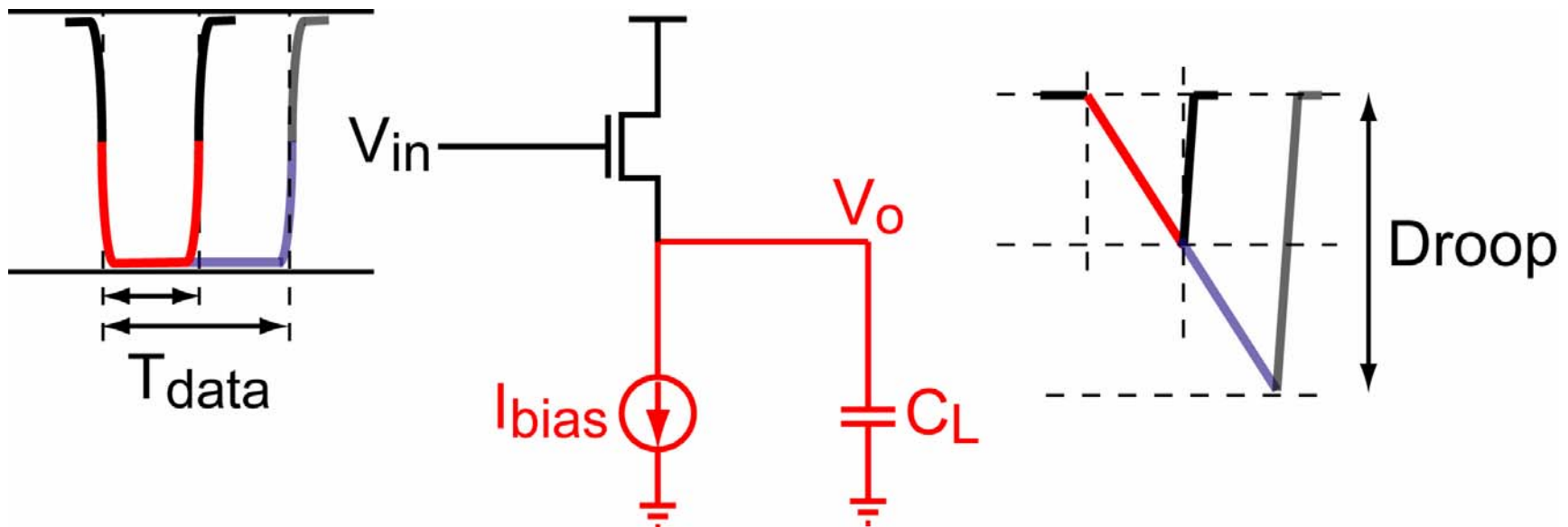
$$\frac{1}{\tau} \propto \frac{\sqrt{I_{bias}}}{C_L} \qquad \text{Slew Rate} \propto \frac{I_{bias}}{C_L}$$

Fast Offset Compensation $\rightarrow$ Large I_{bias}

Operation During Hold Phase
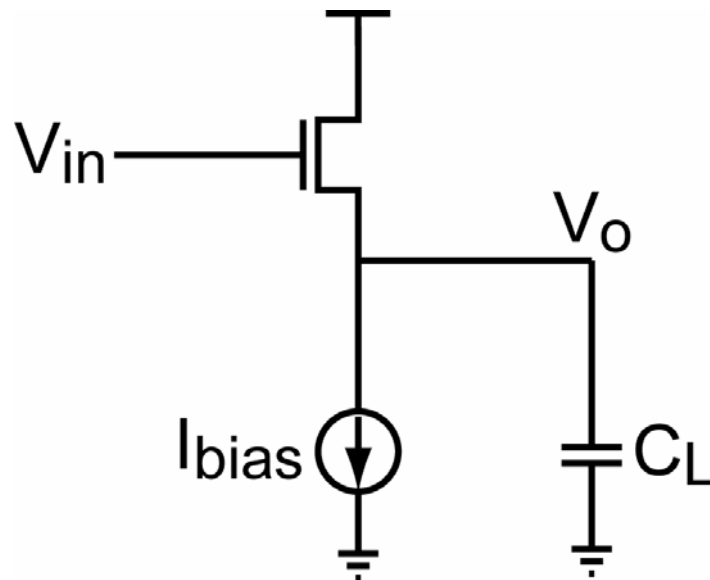
$$Droop = I_{bias} \cdot \frac{T_{data}}{C_L}$$

Droop proportional to both I_{bias} and T_{data}

Data dependent droop $\rightarrow$ Jitter (ISI)

Small Jitter $\rightarrow$ Small I_{bias}
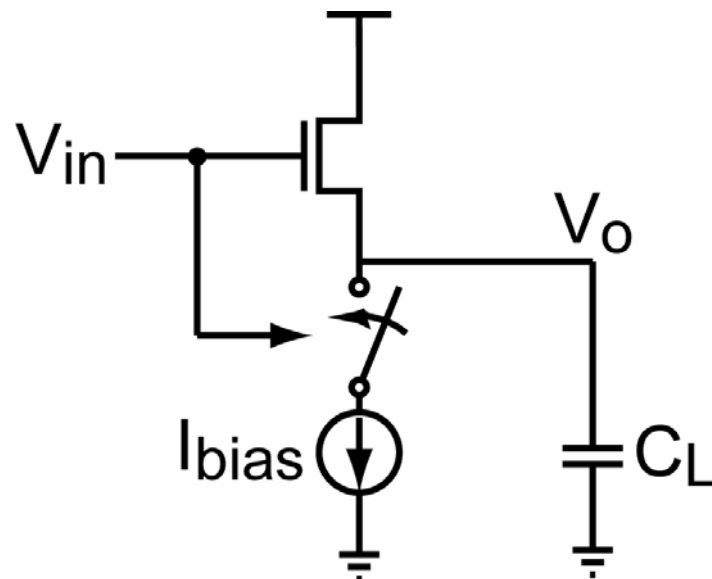
Trade-Off for Traditional Peak Detector

Trade-off betwen *settling time* and *jitter performance* due to Inter-Symbol Interference!

Fast Settling → *Large* I_{bias} Low Jitter → *Small* I_{bias}
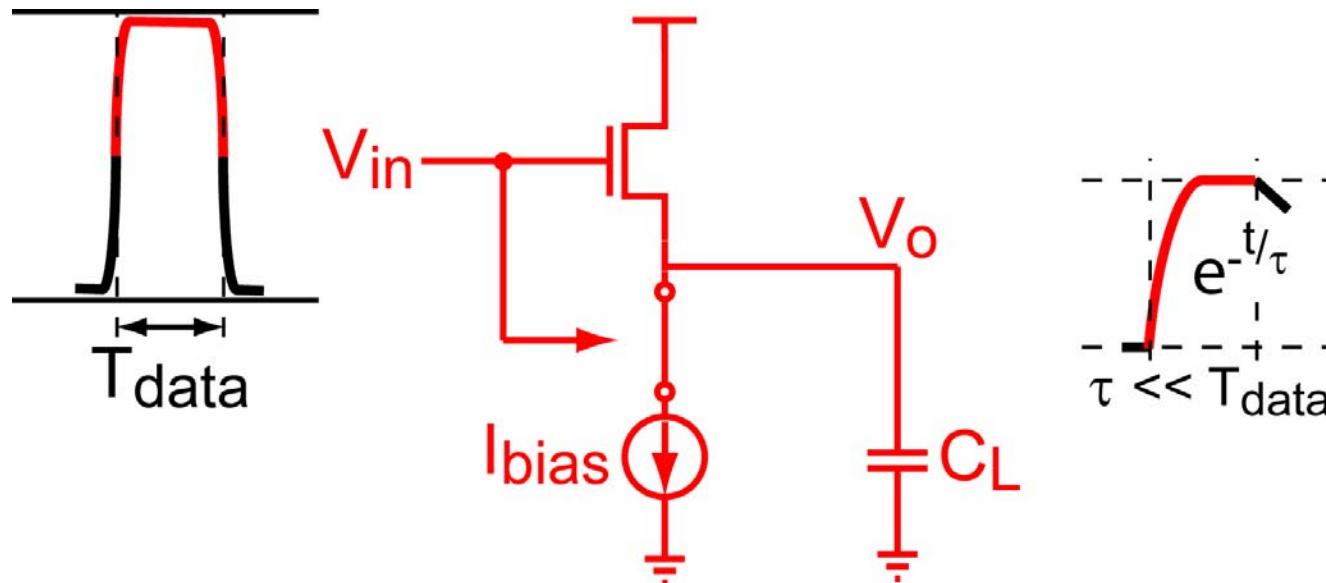
Can we modify the design to improve the trade-off?

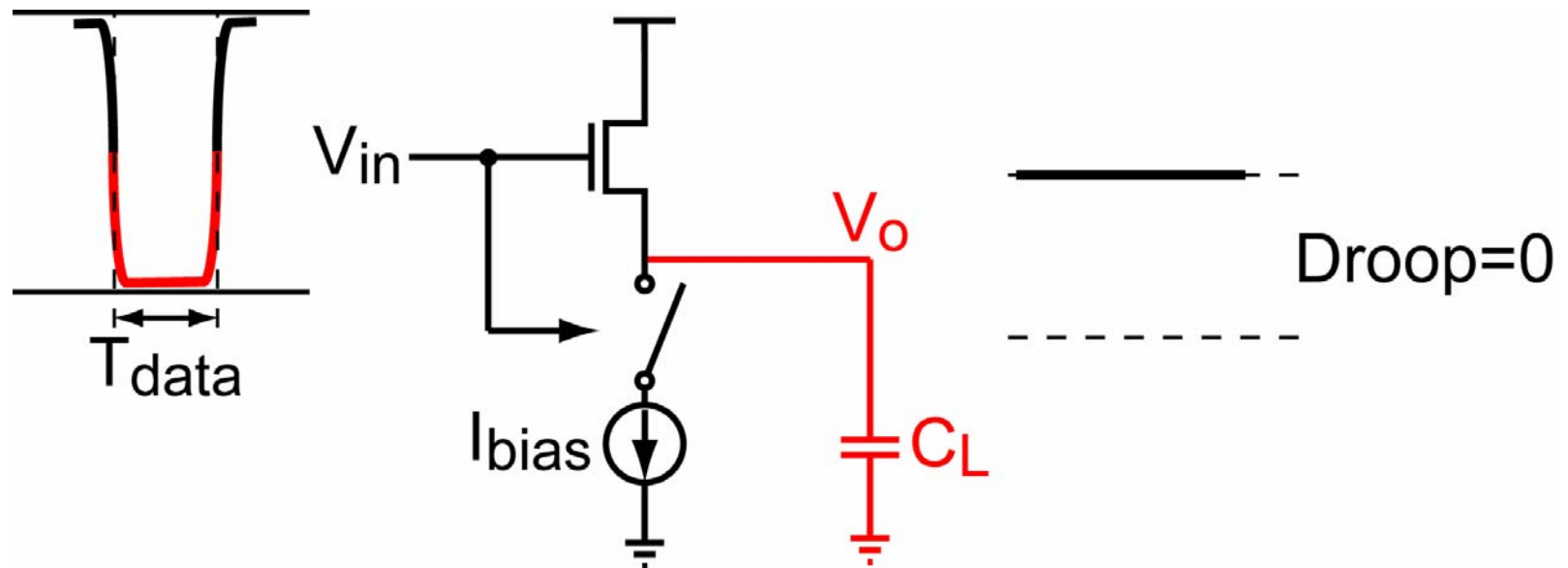## Add switch device that is controlled by the input

Proposed Solution – Track Phase

$$\frac{1}{\tau} \propto \frac{\sqrt{I_{bias}}}{C_L}$$

Slew Rate $\propto \dfrac{I_{bias}}{C_L}$
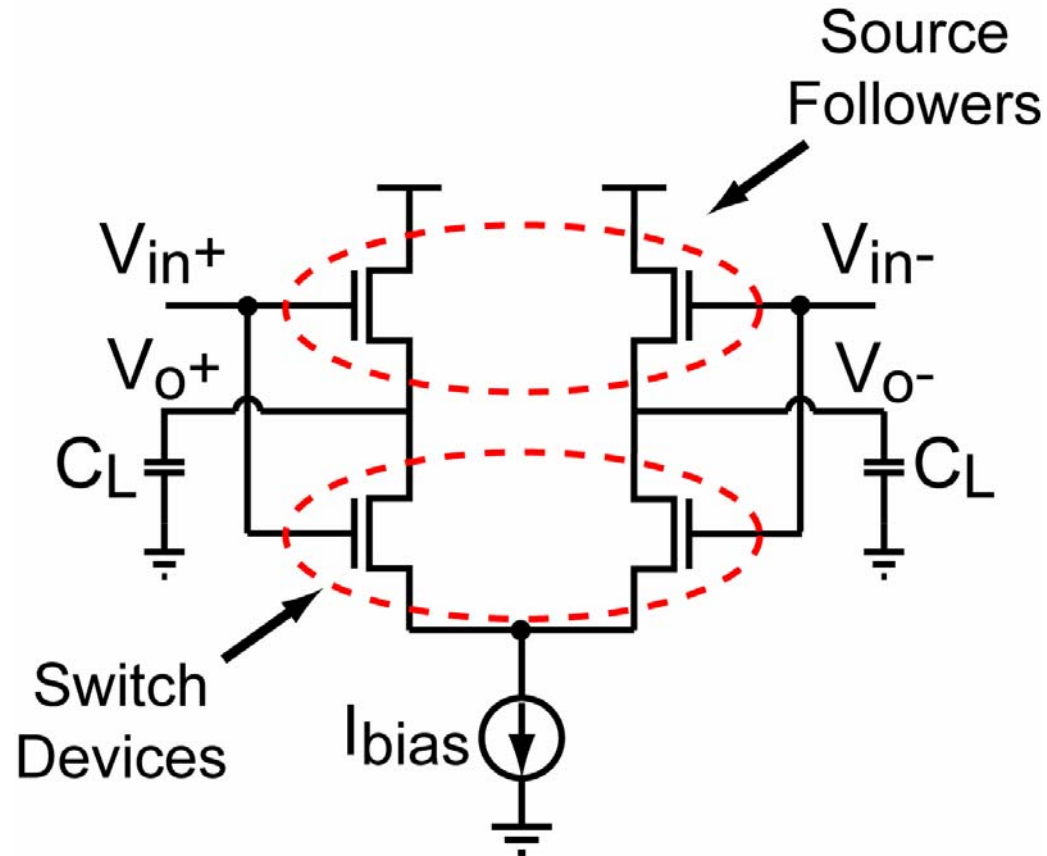

Same operation as original peak detector circuit

Proposed Solution – Hold Phase

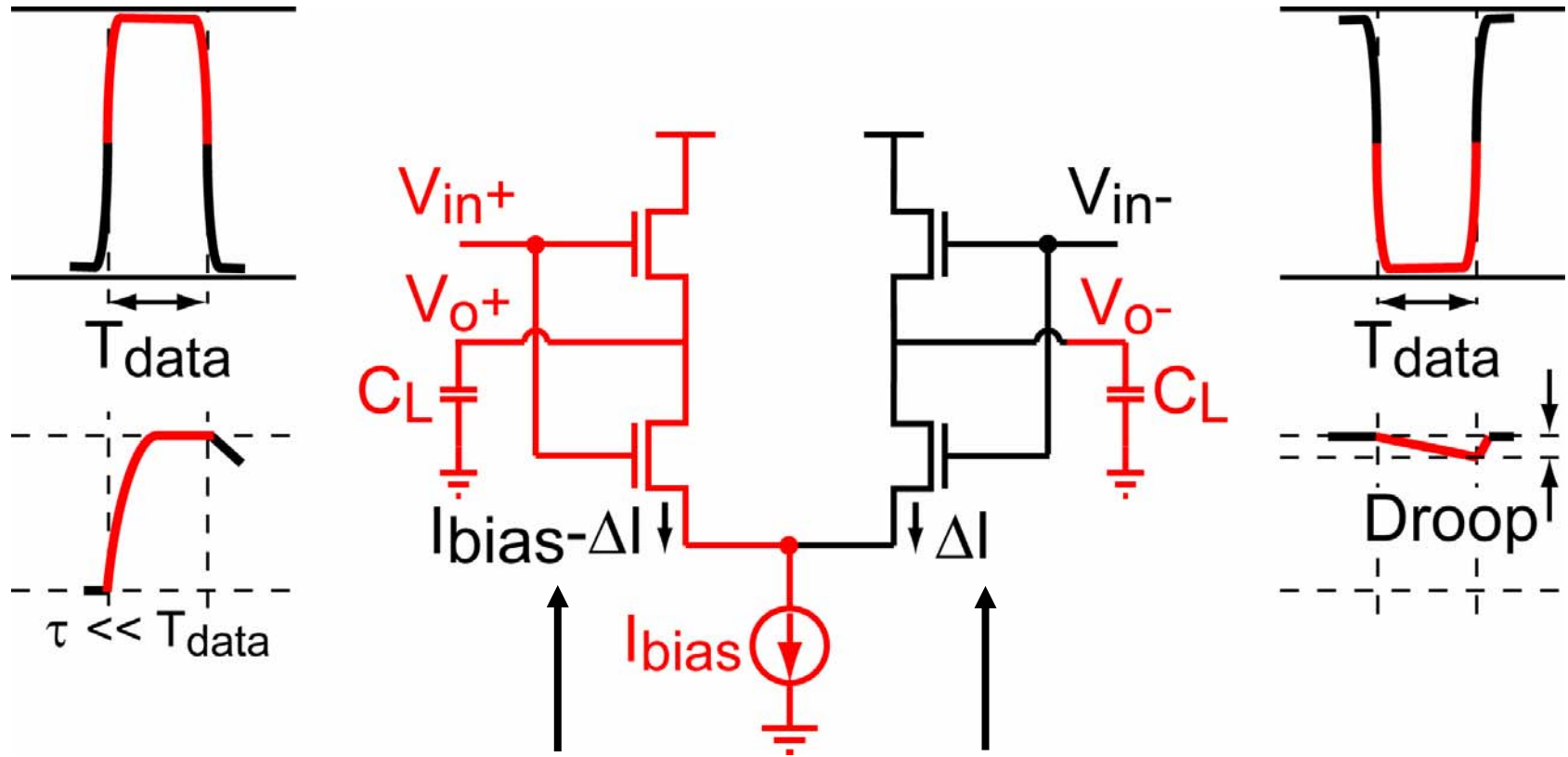Droop is ideally independent of both I_{bias} and T_{data}

Can achieve small jitter with a large I_{bias}
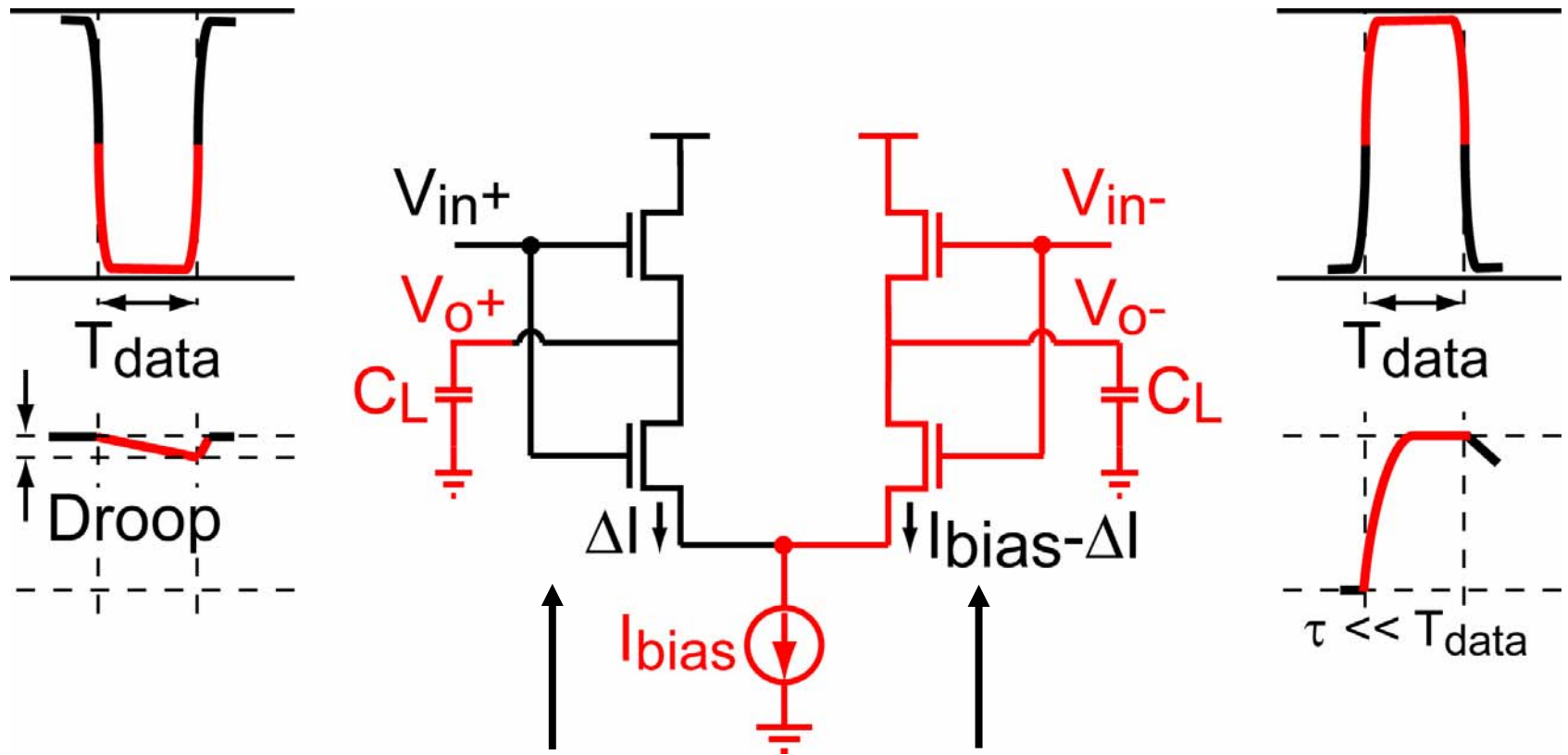
Proposed Solution – Differential Design

Use inputs to switch I_{bias} between
the two source-follower circuits

Proposed Solution – Operation
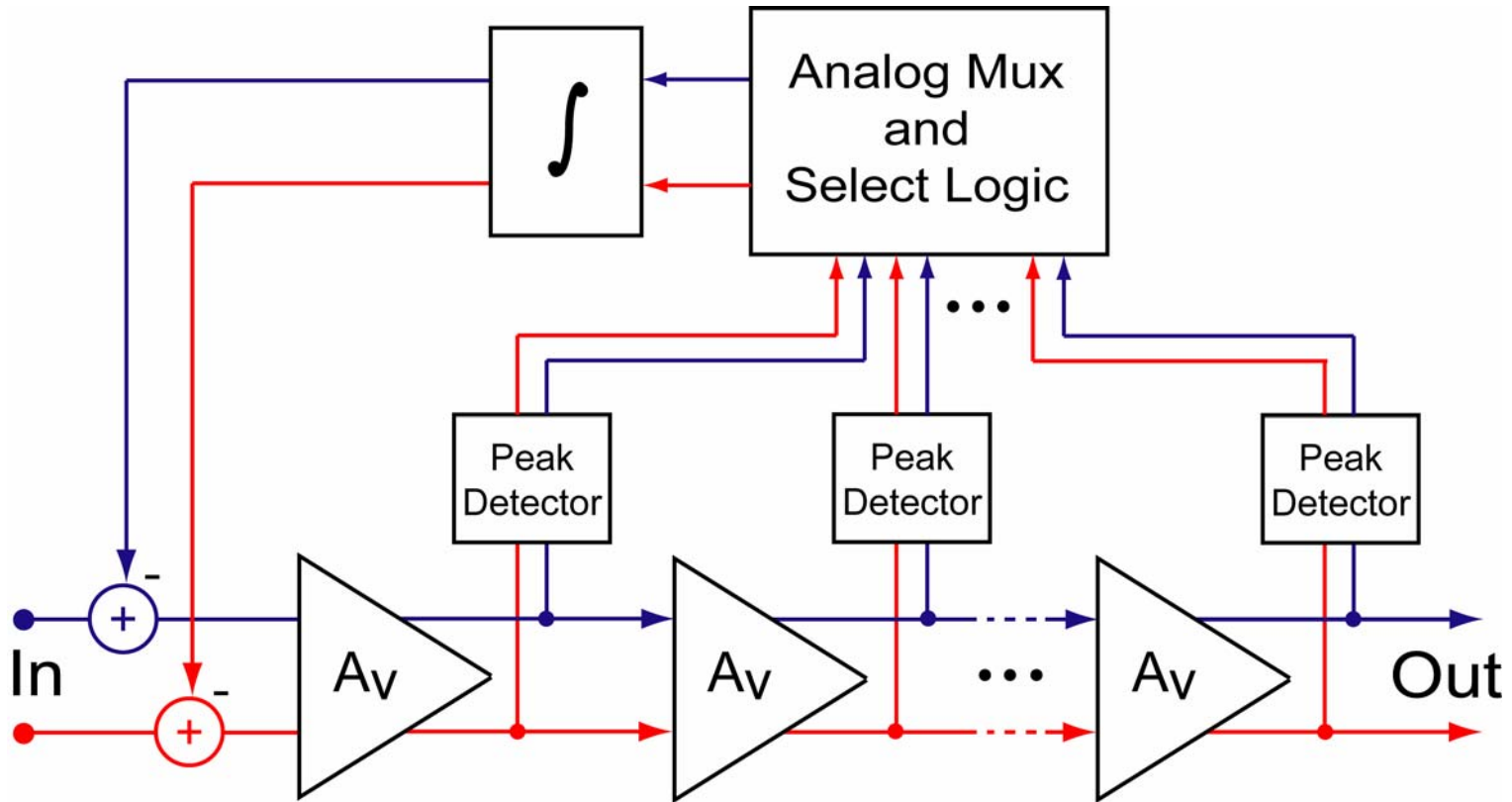

Incomplete switching causes non-zero droop

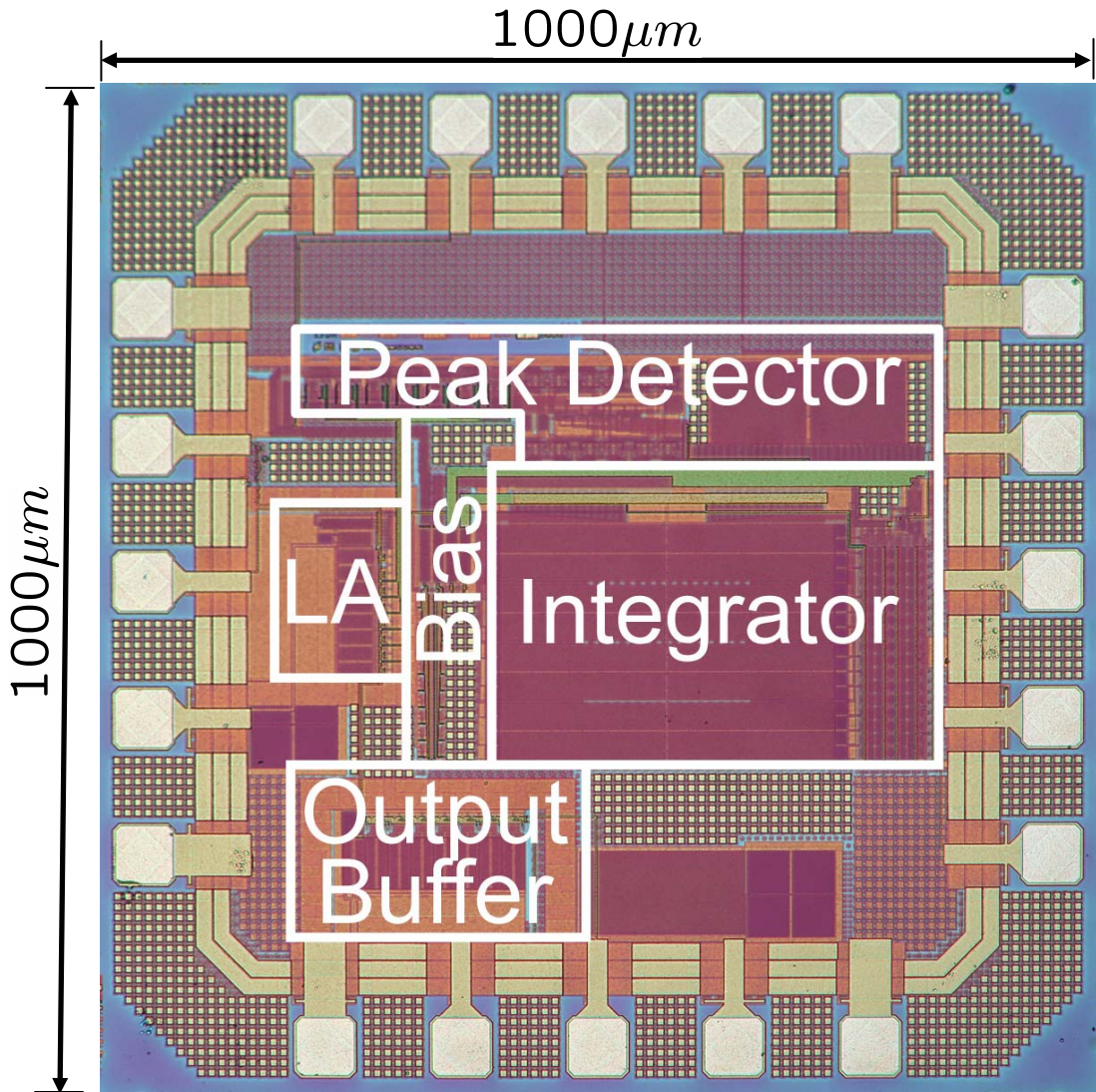Incomplete switching causes non-zero droop

Simultaneously achieve fast offset
compensation and low droop

Multi-Tap Compensation

- **Dynamic multi-tap control loops are required**
- **Peak detector at each amplifier output**
- **All loops have matched gain**

Test System – Die Micrograph

$1000\mu m$

$1000\mu m$

Peak Detector

Bias

LA

Integrator

Output Buffer

Fabricated in National Semiconductor's
$0.18\mu m$ CMOS process

- $3.125Gb/s$ limit-amp.
  - 42dB gain
  - 5GHz BW
- Compensation
  - time $< 1\mu s$
- Meet OC48 jitter specs.
  - $< 4ps_{RMS}$ @ 2.5Gb/s

- Total area: $1mm^2$
- Active area: $0.5mm^2$
- Supply Voltage: 1.8V
- Total Power: 338mW
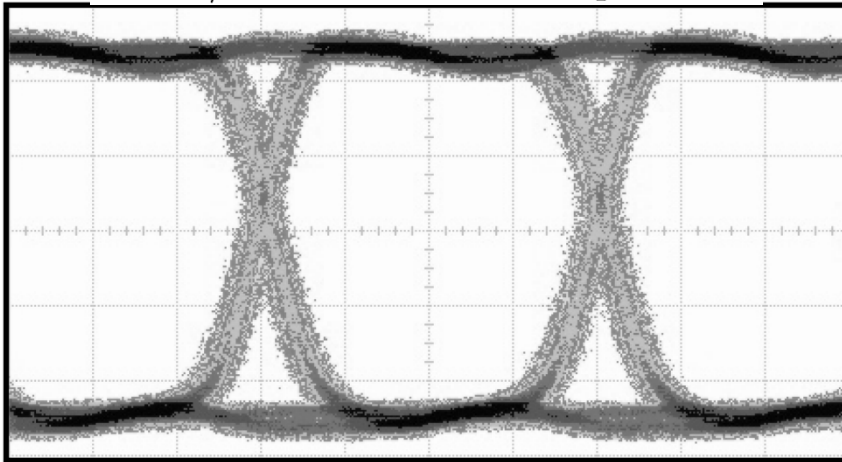- Power of LA & Offset
  - Compenstion: 113mW

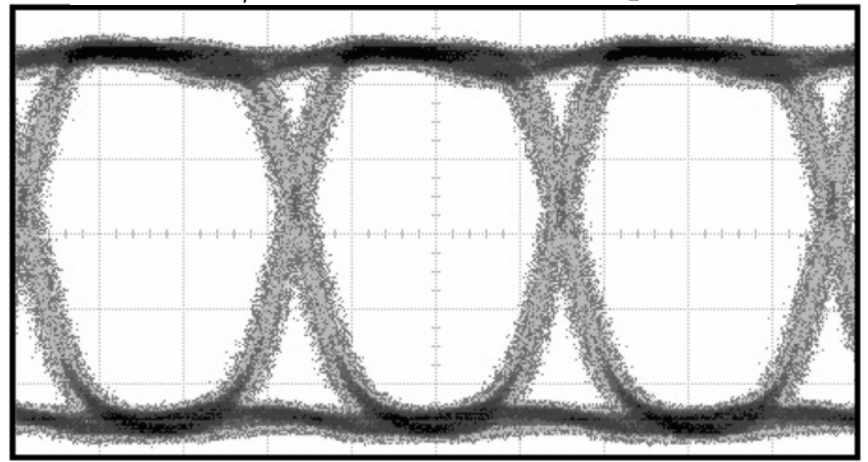Eye diagrams with $2.5mV_{pp}$ PRBS $2^{31} - 1$ input

Offset Compensation Settling time $\approx 1\mu s$

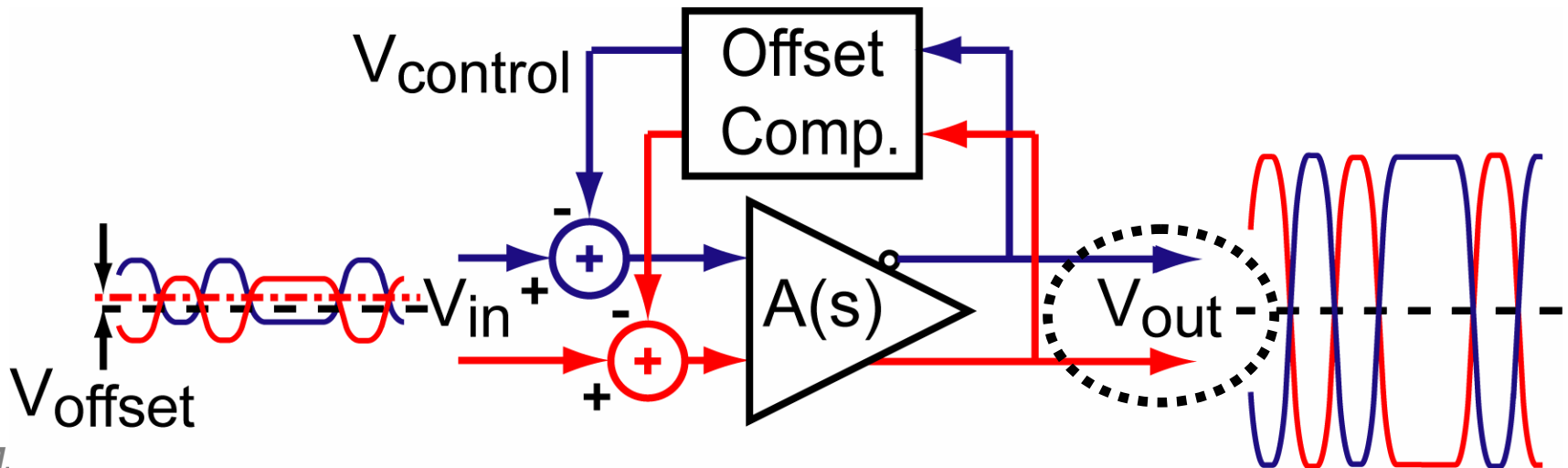$2.5Gb/s \rightarrow Jitter = 3.71ps$ RMS

$3.125Gb/s \rightarrow Jitter = 5.90ps$ RMS

Horizontal Scale: 100ps/div   Vertical Scale: 50mV/div

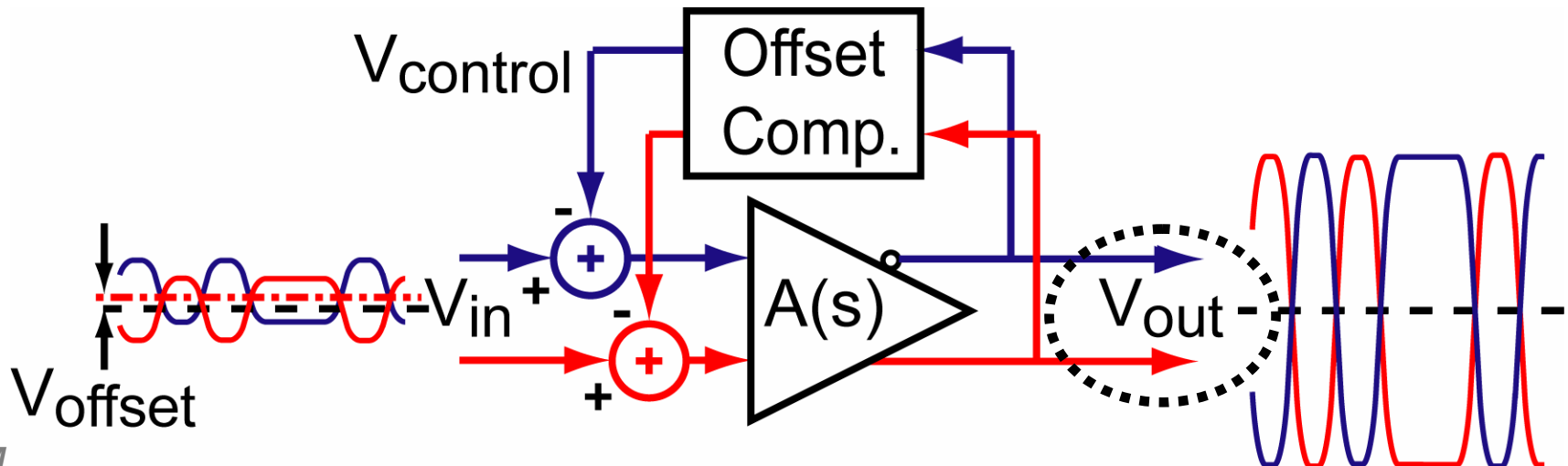Horizontal Scale: 100ps/div   Vertical Scale: 50mV/div

$V_{control}$

Offset Comp.

V_{in}

$A(s)$

V_{out}

V_{offset}

Test System – Measured Results

Offset Compensation Settling time $\approx 1\mu s$

Input Amp	Data Rate		
	1.0Gb/s	2.5Gb/s	3.125Gb/s
2.5mVpp	3.94	3.71	5.90
10mVpp	2.65	2.86	6.30
50mVpp	1.13	2.52	7.98

Meets OC-48 Jitter Spec (< 4.0ps RMS) down to $V_{in,pp} = 2.5mV$

V_control

Offset Comp.

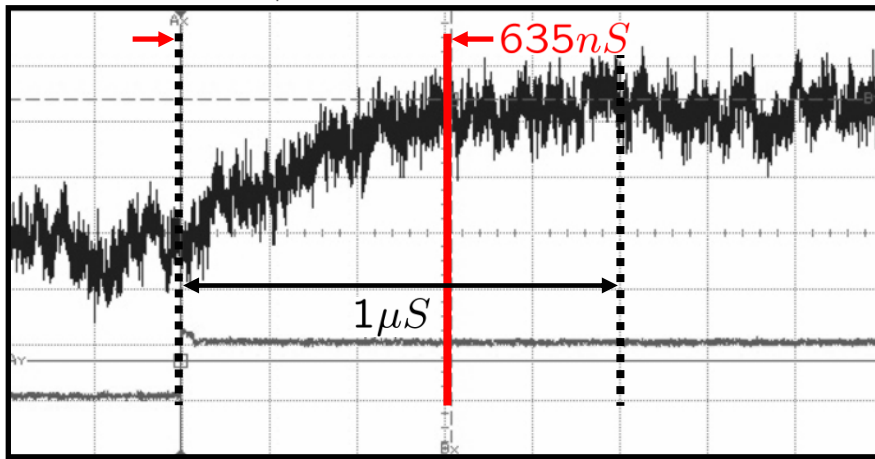V_{in}

$A(s)$

V_{out}

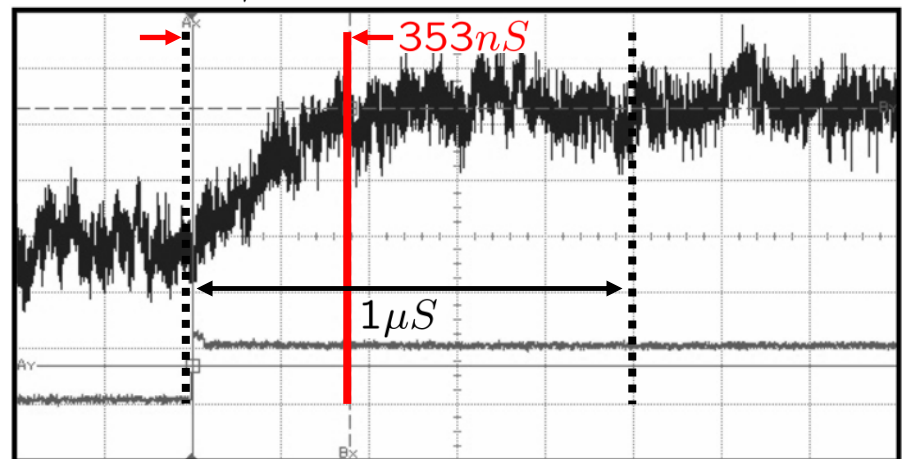V_{offset}

Test System – Measured Results

Control voltage step-response with a $5.0mV_{pp}$ PRBS $2^{31} - 1$ input

Compensation Settling time goal $\approx 1\mu s$
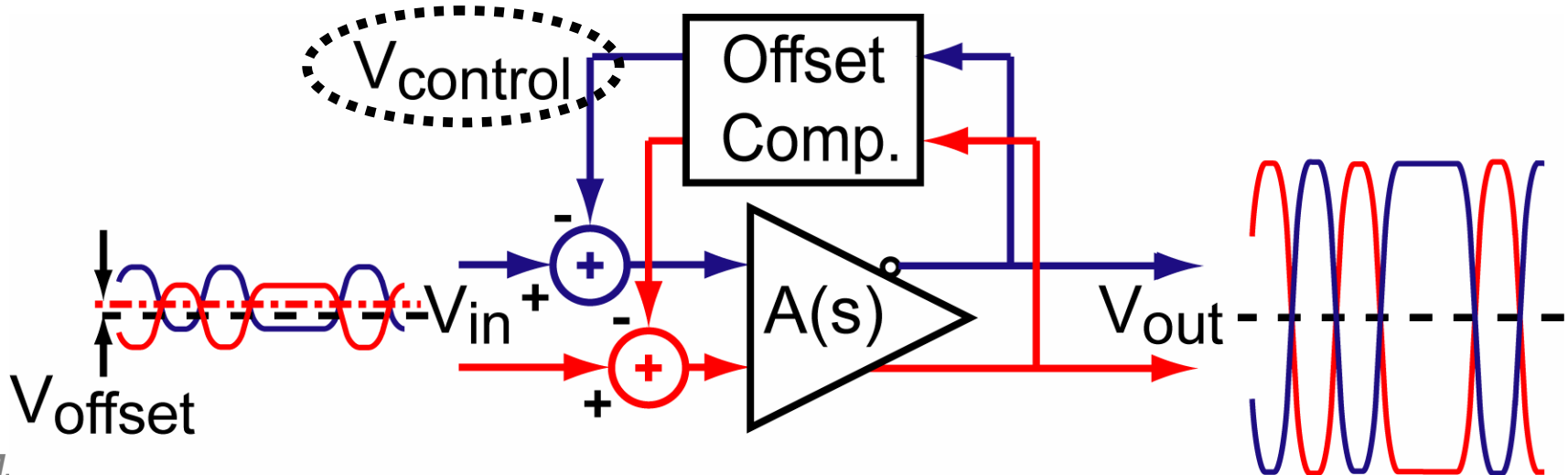$3.125Gb/s \rightarrow Jitter = 5.75ps$ RMS

635nS

1μS

Horizontal Scale: 200ns/div   Vertical Scale: 5mV/div

Compensation Settling time goal $\approx 0.33\mu s$
$3.125Gb/s \rightarrow Jitter = 5.90ps$ RMS

353nS

1μS

Horizontal Scale: 200ns/div   Vertical Scale: 5mV/div

$V_{control}$

Offset Comp.

V_{in}

V_{offset}

$A(s)$

V_{out}

Summary

- **Proposed peak detector design enables a *1000x improvement* in the trade-off between settling time and output jitter by changing relationship between peak detector bandwidth and output droop**

- **Implemented and tested system with proposed offset compensation method that has *2.5mVpp input sensitivity* and that meets OC48 jitter specifications (< 4ps RMS @ 2.5Gb/s)**

- **Behavior model download:**
  - **http://www.cppsim.com**

A Delay-Locked Loop using a Synthesizer-based Phase Shifter for 3.2 Gb/s Chip-to-Chip Communication

Chun-Ming Hsu, Charlotte Y. Lau, Michael H. Perrott

Massachusetts Institute of Technology

Delay-Locked Loop for Data Recovery
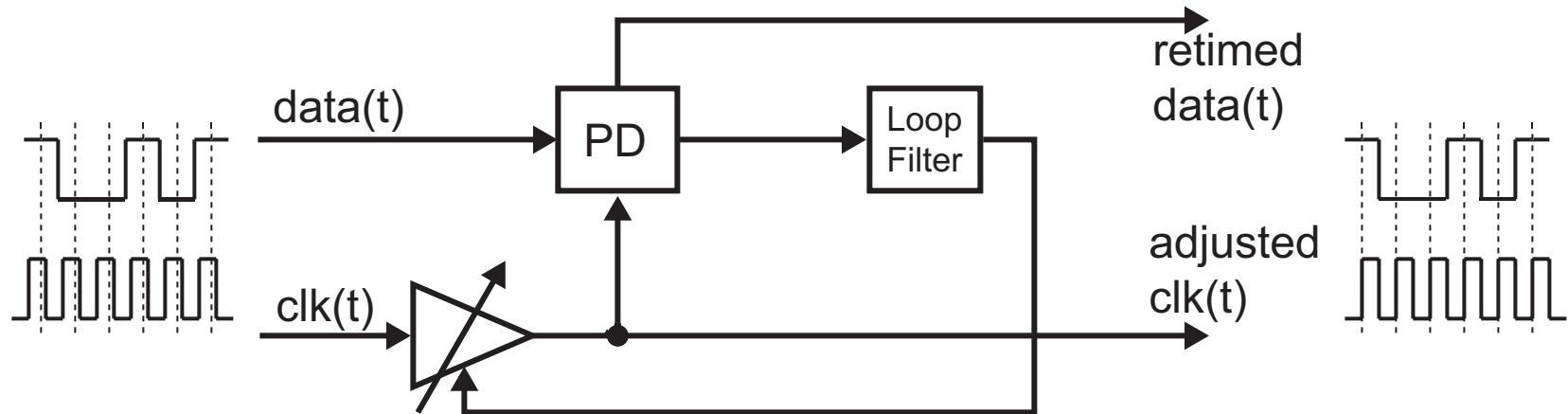
- **In some applications, a reference clock that is perfectly matched in frequency to data sequence is available**
  - **Phase mismatch is present due to different propagation delays between clock and data on the PC board**
- **A delay-locked loop limits adjustment to phase (as opposed to phase and frequency)**
  - **Faster, and much simpler to design than PLL structure**

Delay-Locked Loop using Phase-Interpolator

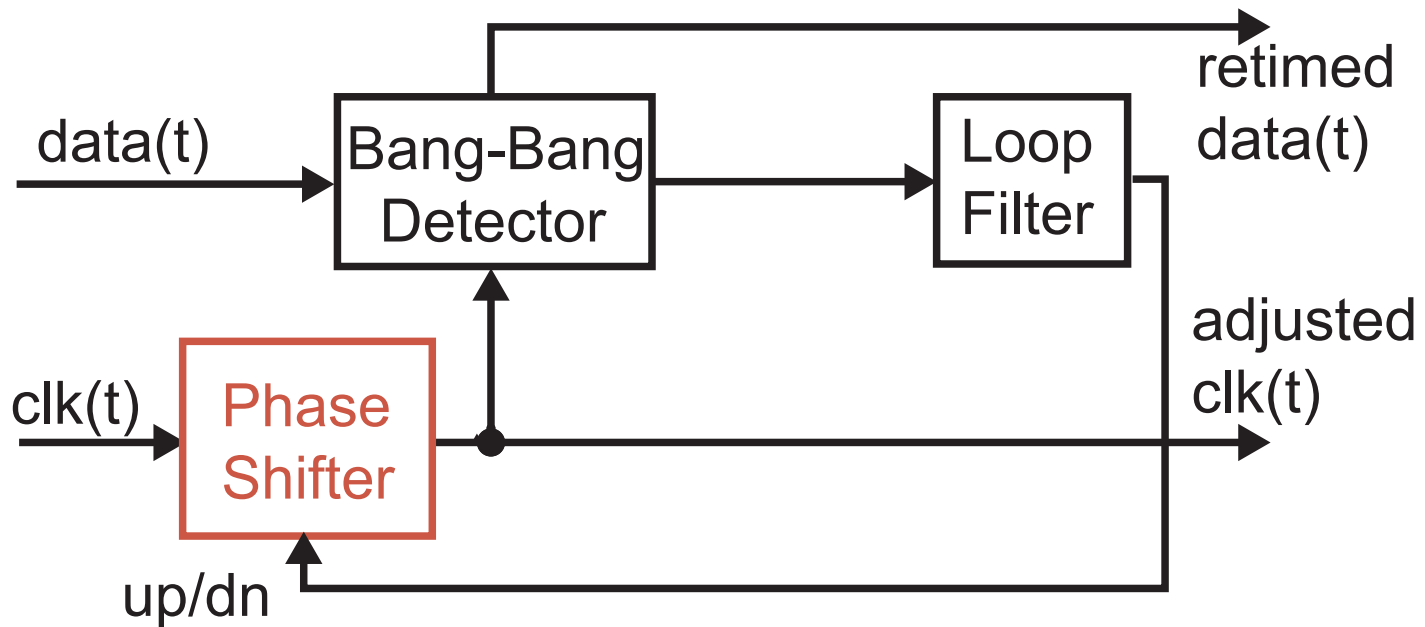Phase interpolator

Adjusted clk Phase
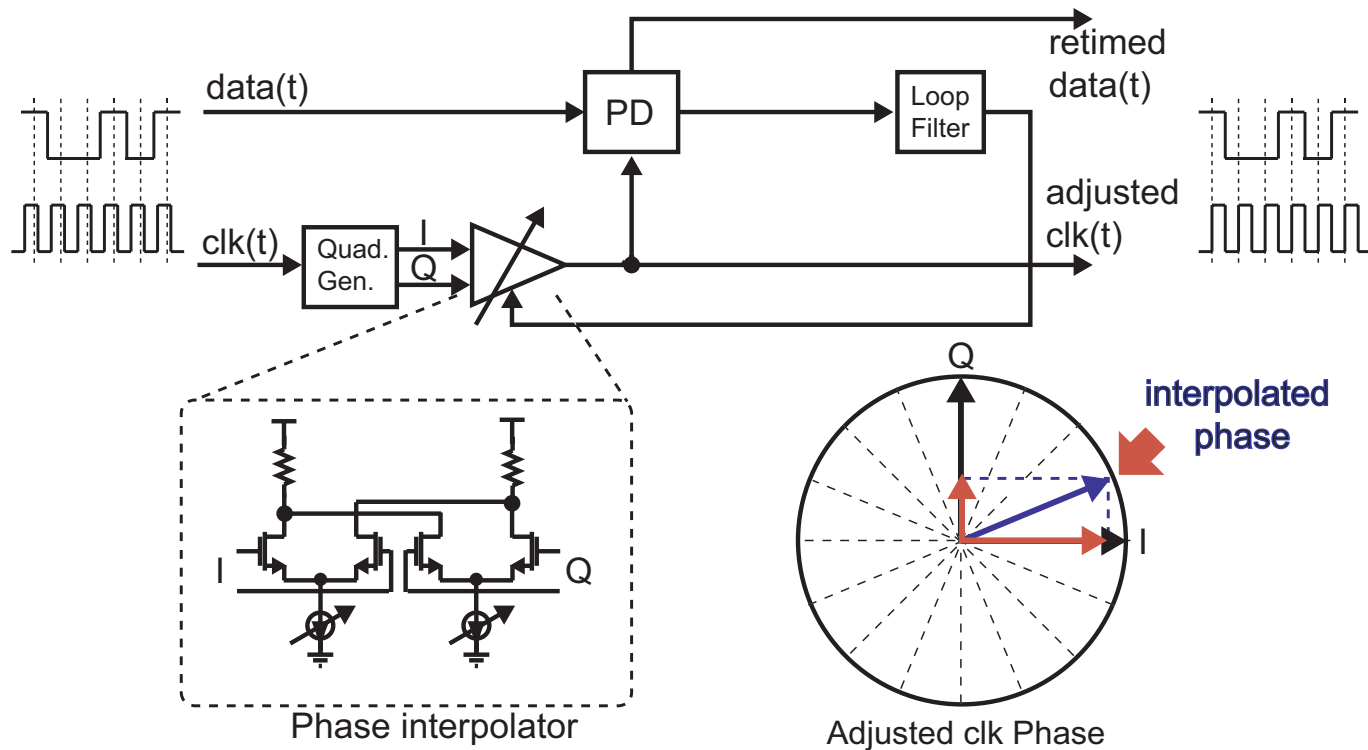
- **Infinite delay range and good jitter performance**
- **Issue:**

**Good matching needed for accurate phase control,
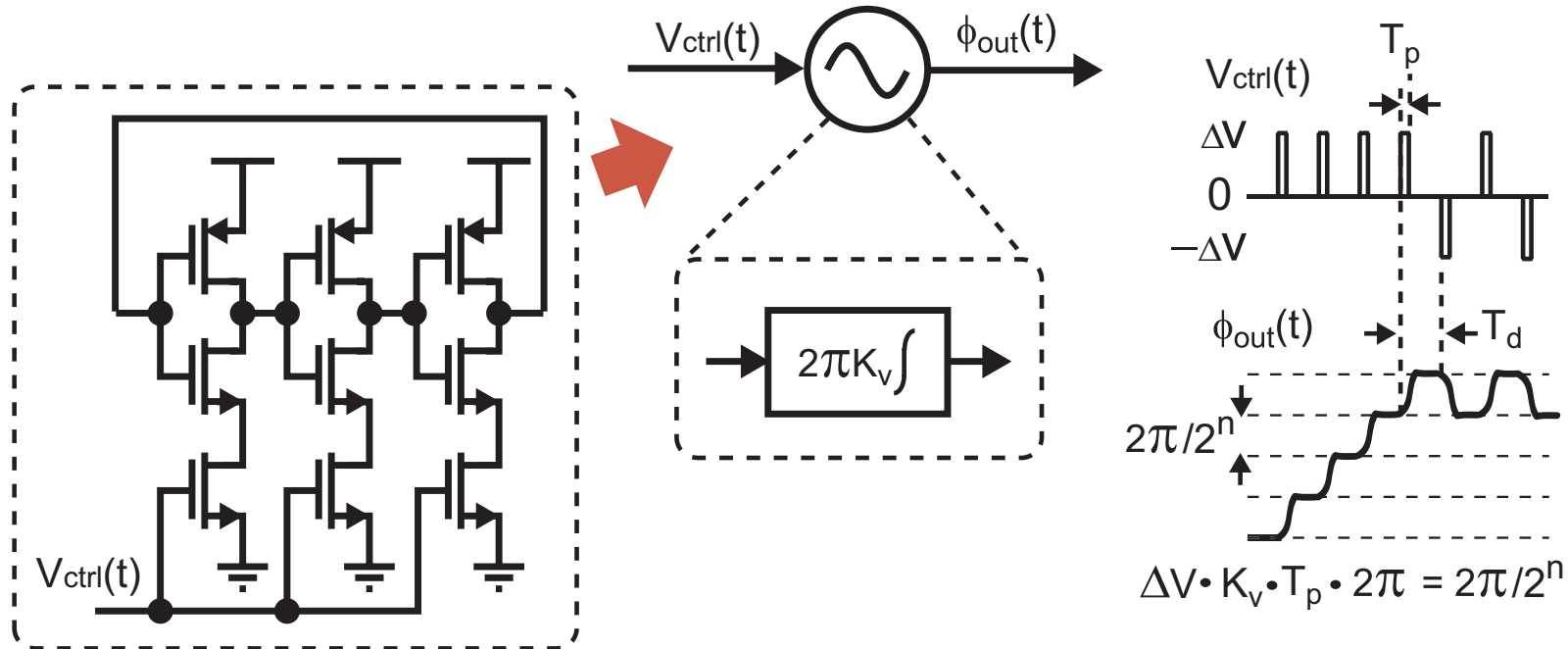but future processes promise high variation …**

Can we eliminate the need for good matching?

Proposed DLL

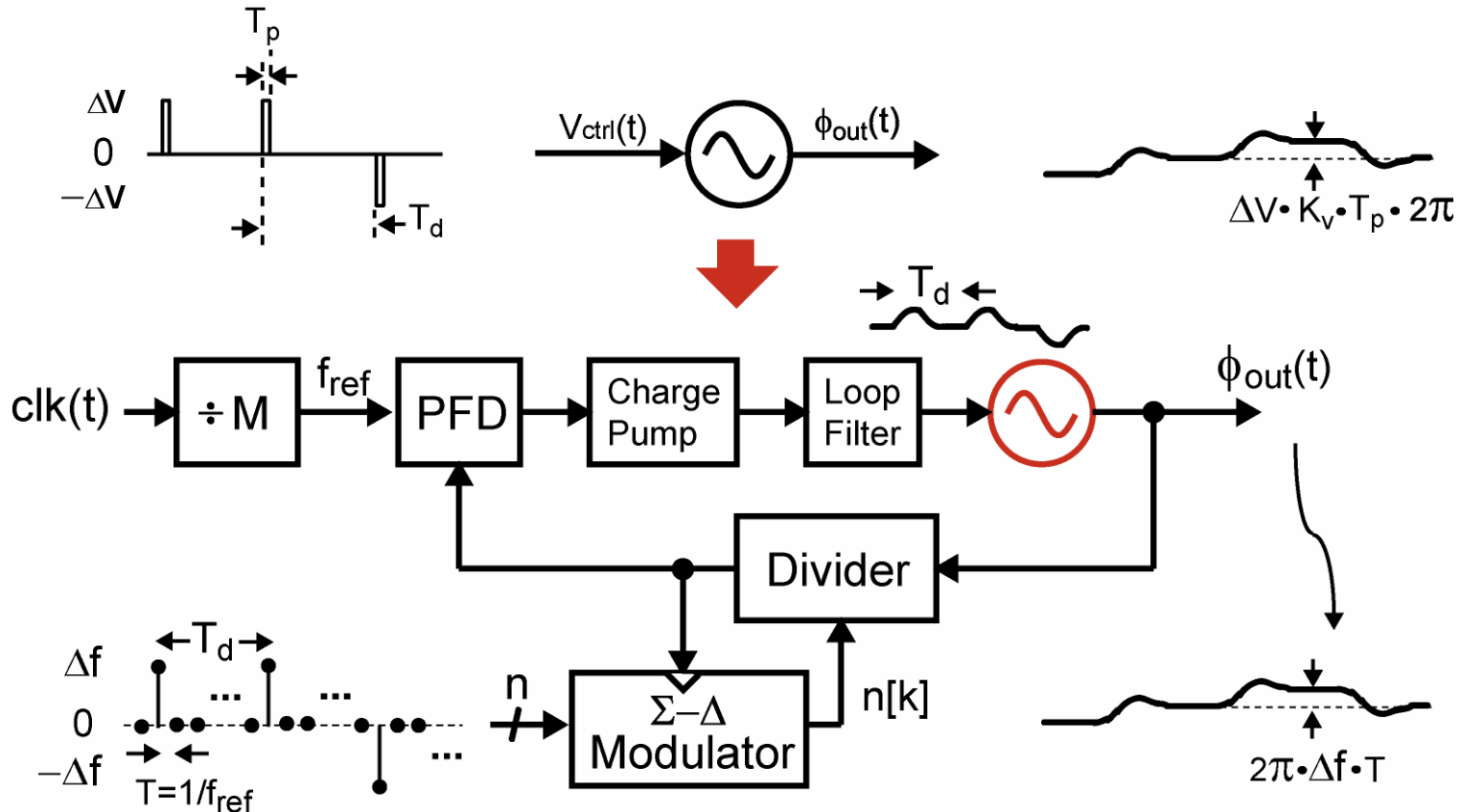- **Use Σ-Δ frequency synthesizer as a phase shifter**

VCO-based Phase Shifter

$$\Delta V \cdot K_v \cdot T_p \cdot 2\pi = 2\pi/2^n$$

- **VCO output phase increases or decreases by a step when a pulse is fed into it**

- **Fine phase resolution and infinite range are achieved**
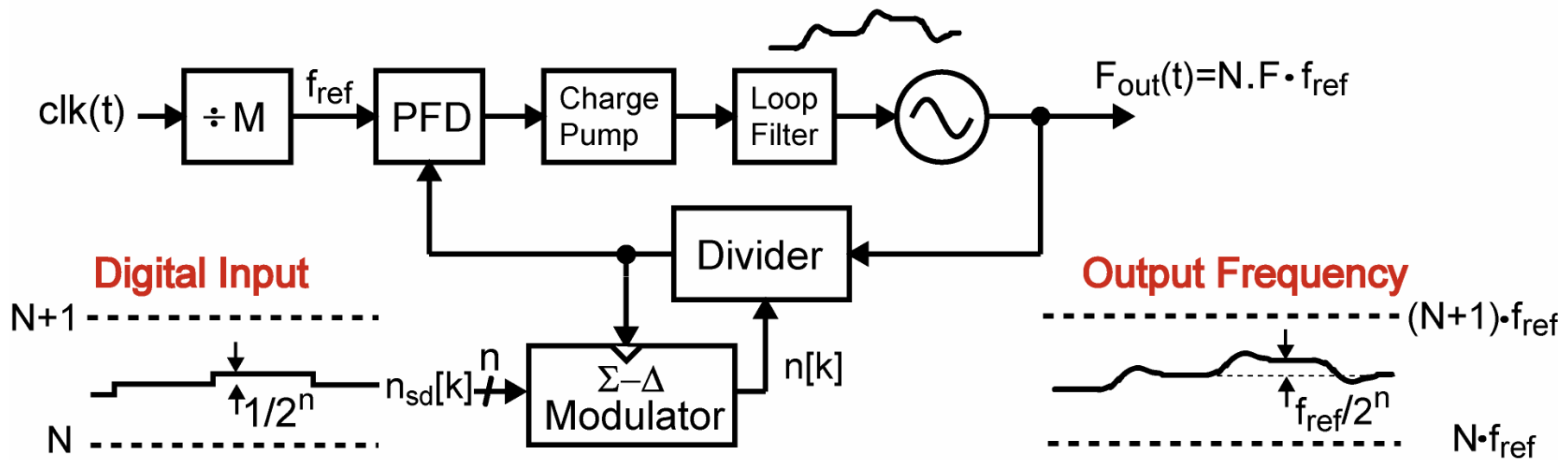
Issue1: How to control the VCO frequency accurately?
Issue2: How to control the phase step accurately?

# Solution: Synthesizer-based Phase Shifter

- **Use a PLL to lock VCO frequency to received clock**
- **Use Σ-Δ technique *in digital domain* to control the VCO phase**

Most Synthesizer Applications Look at Frequency

■ **Fractional output frequency is provided by a fractional-N frequency synthesizer**

Here We Will Look at Phase ....

$\phi_{out}(t) = 0.F \cdot 2\pi$

Digital Input

N+1

$T = 1/f_{ref}$, $1/2^n$

N

Output Phase

2π

$2\pi/2^n$

0
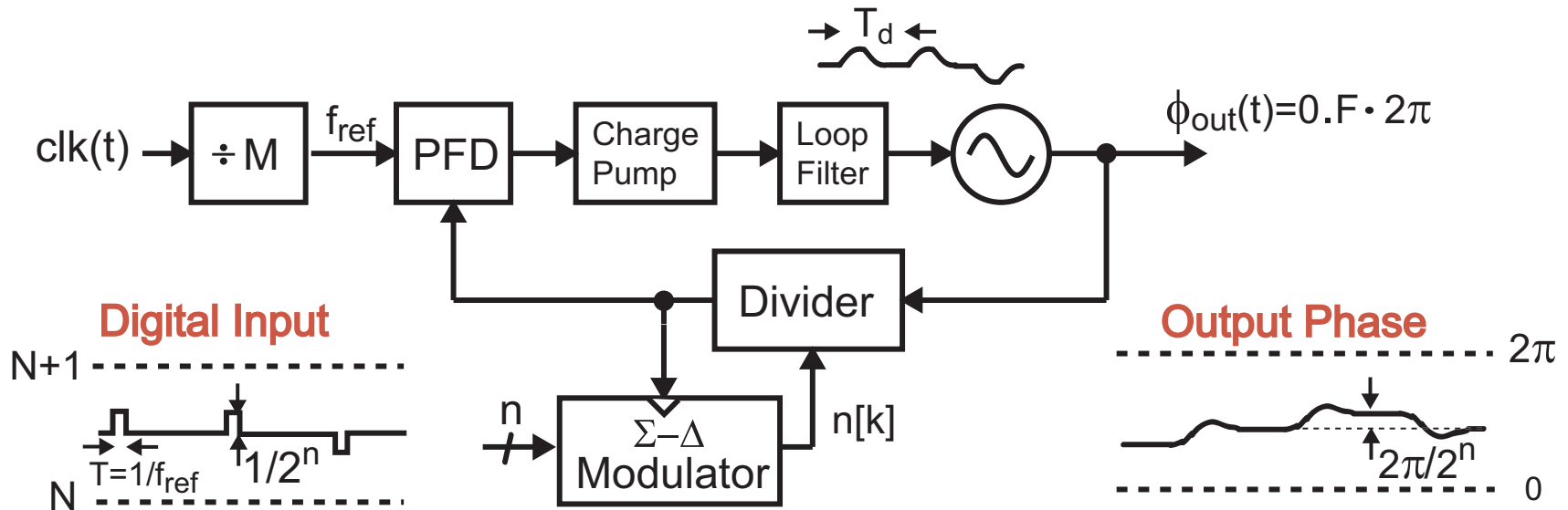
- **Phase step decreases together with pulse height**

Phase step is determined only by the number of bits of the Σ-Δ modulator ➡ No process, voltage, and temperature (PVT) variations

Design Consideration of the Phase Shifter
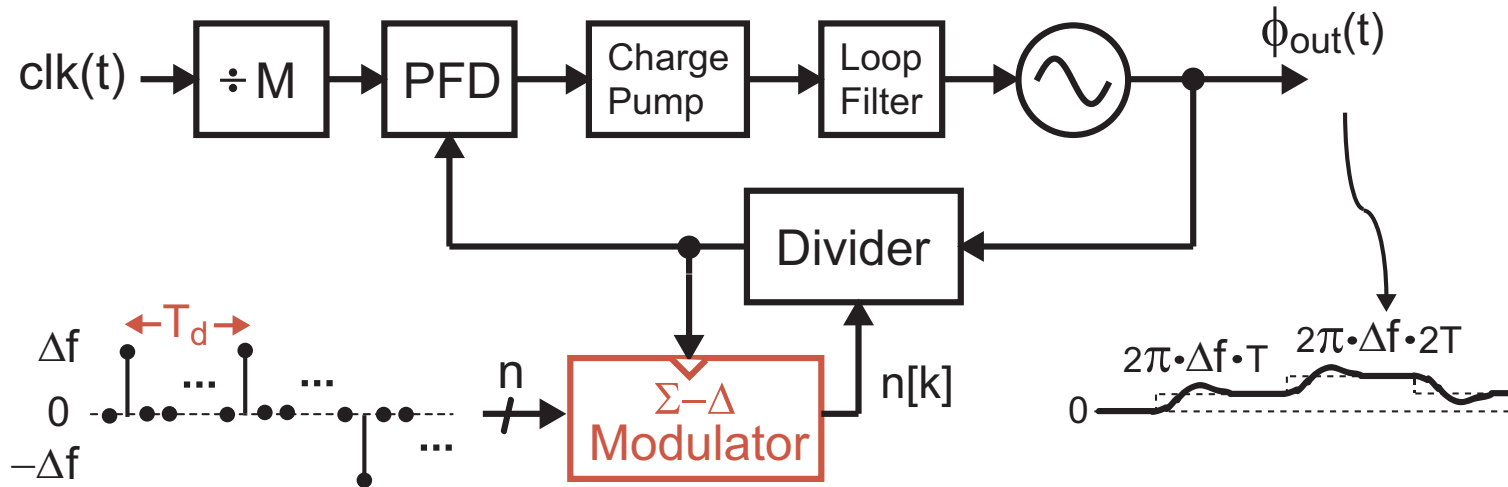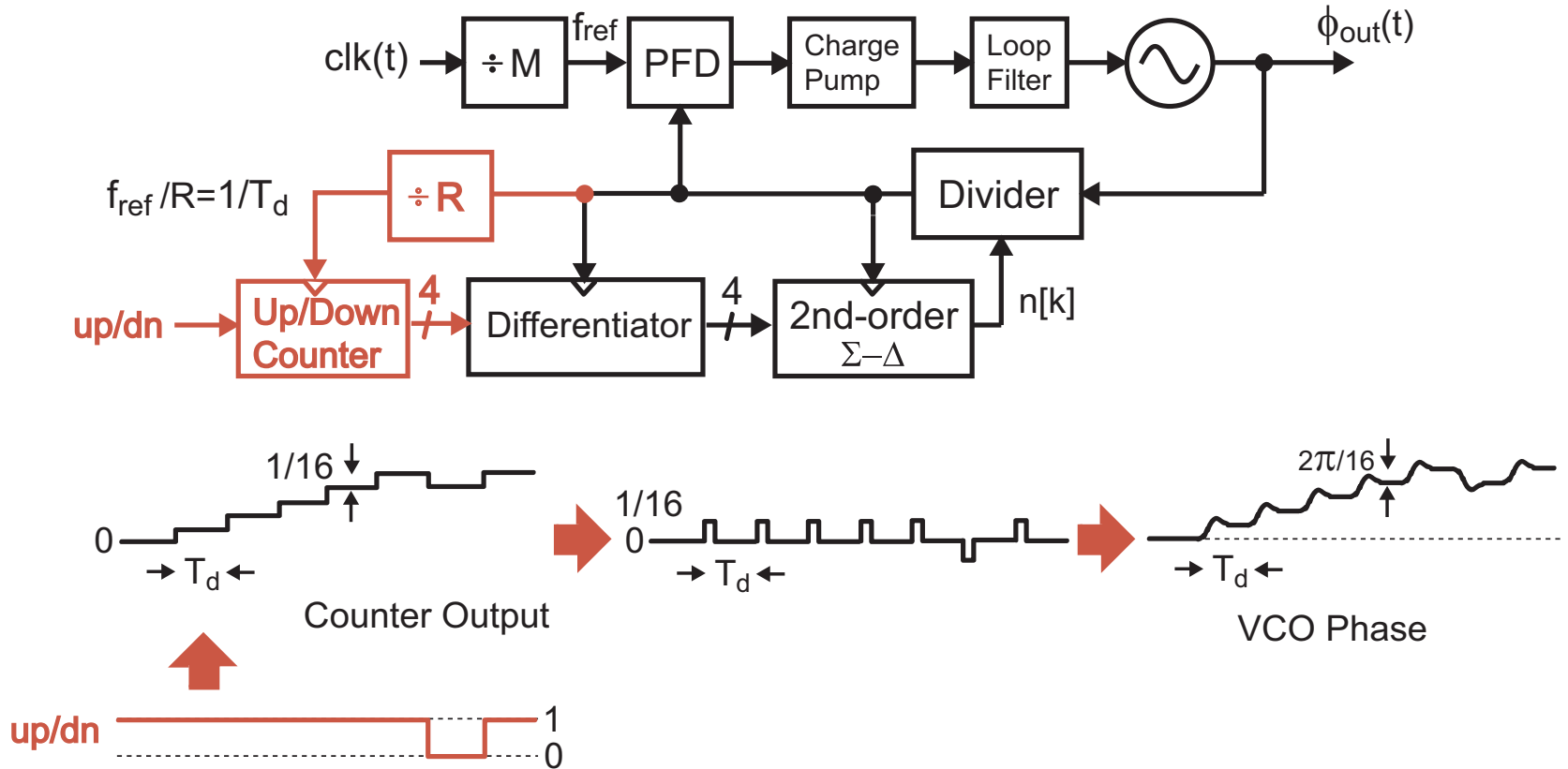

- **Wait enough time before feeding next pulse to allow proper settling of VCO phase ➡ T_d > 1/bandwidth**

- **How to implement a simple Σ-Δ modulator?**

Phase Shifter Guided by Staircase Input
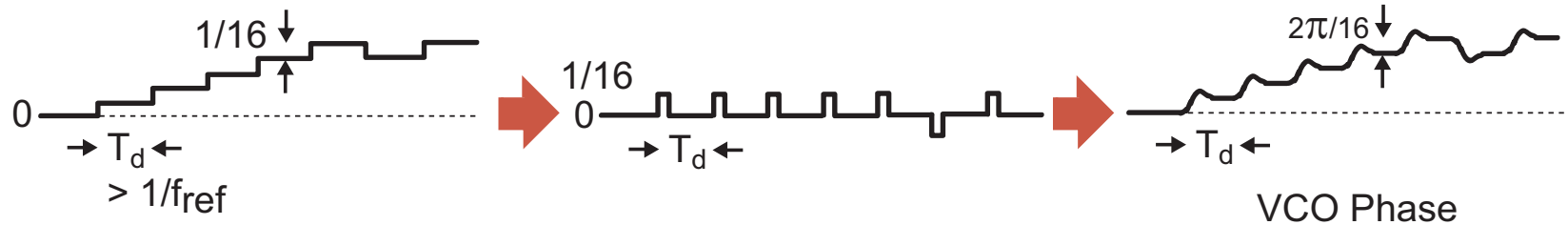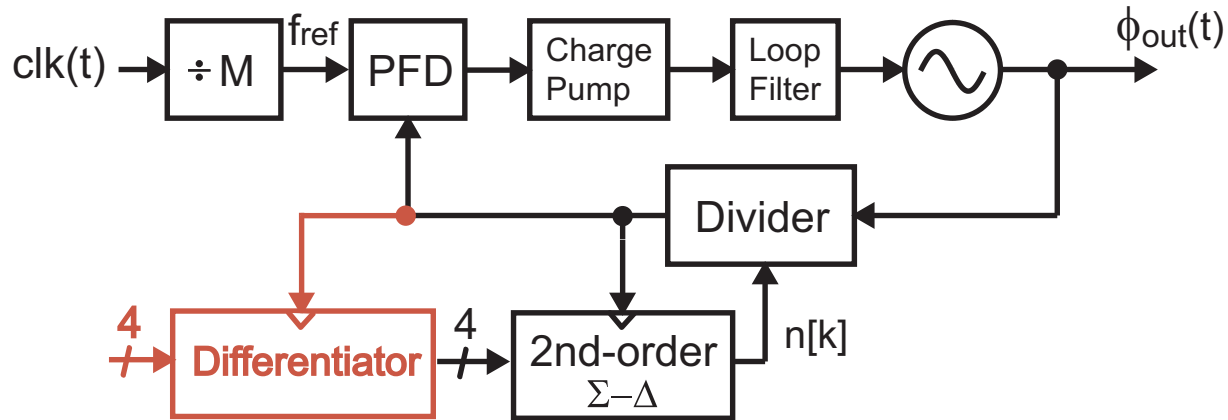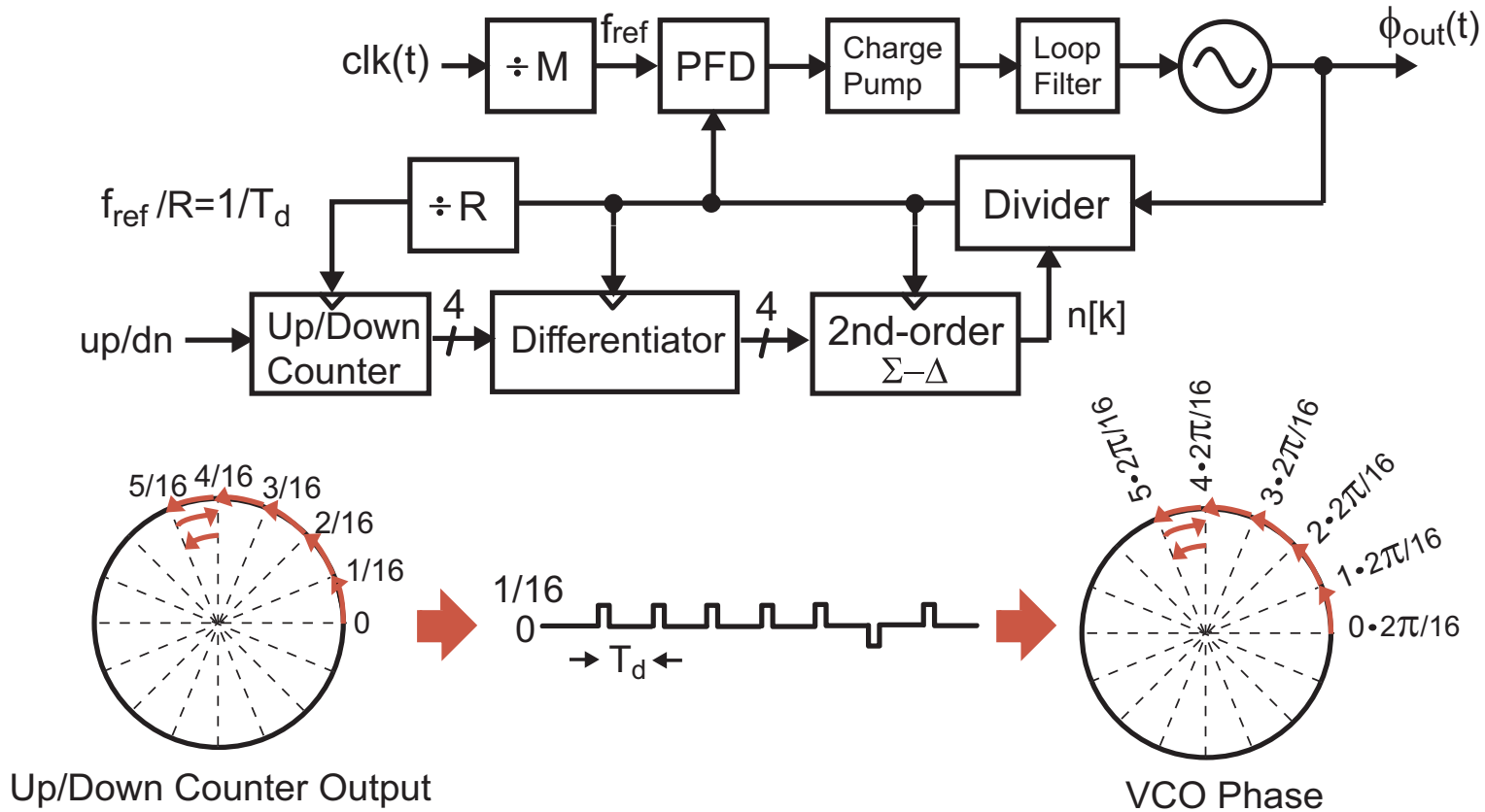

- **Use a differentiator to generate the pulses from a staircase input**

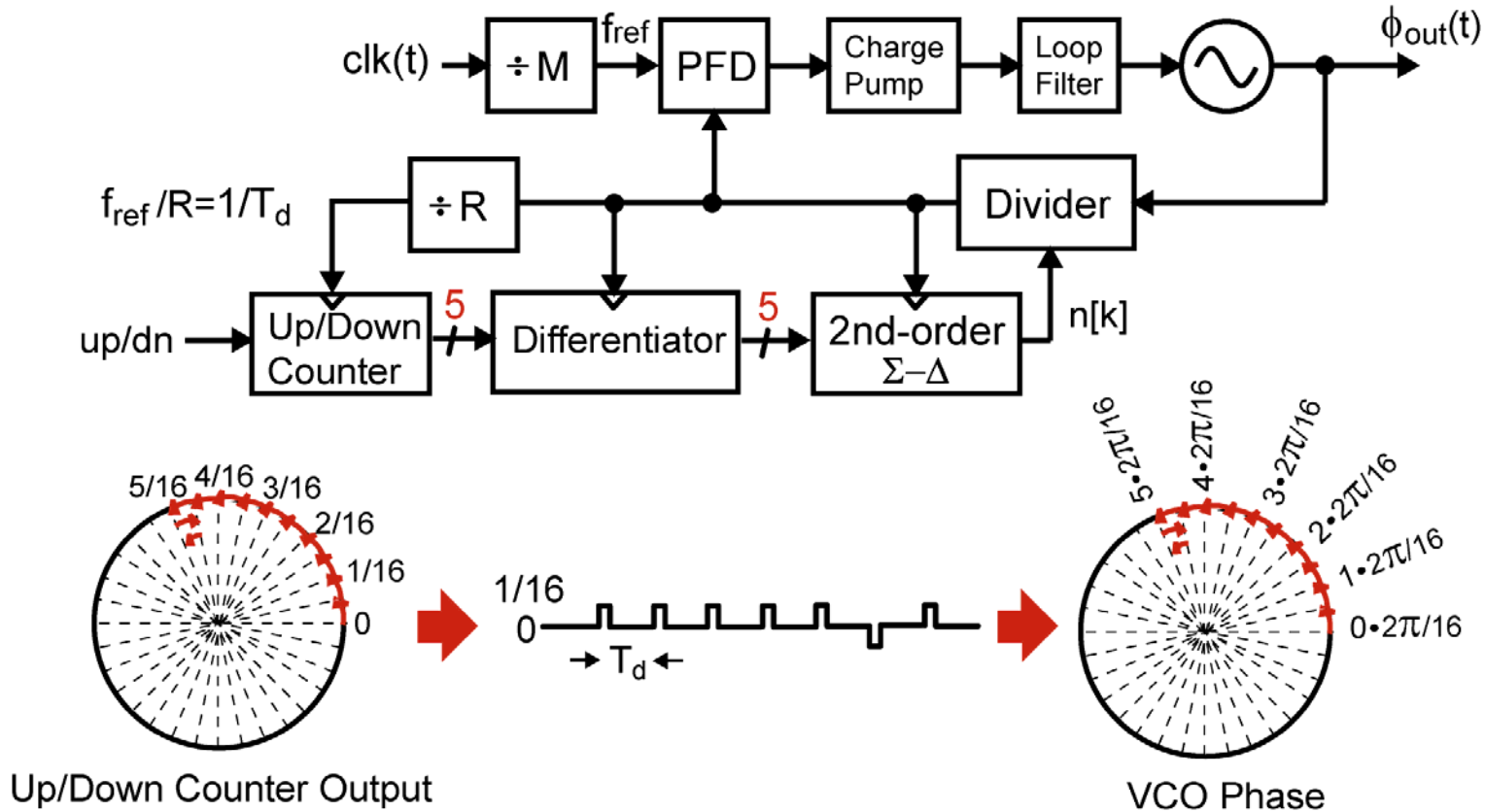# *Phase Shifter Guided by Up/Down Counter*

- **VCO phase shifts according to Up/Down counter**
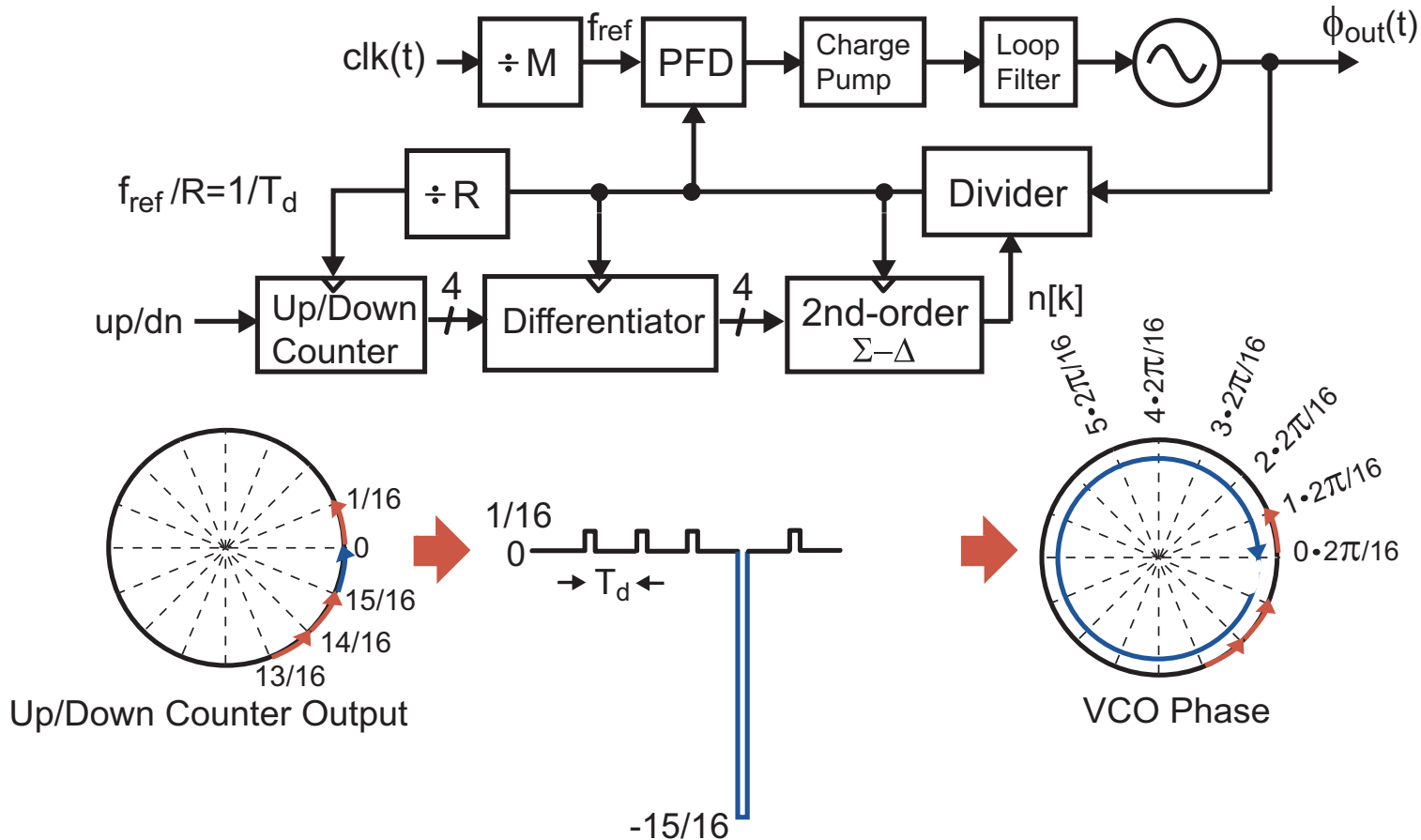
Phase Shifter Guided by Up/Down Counter (cont'd)

Up/Down Counter Output

VCO Phase

- **VCO phase shifts according to Up/Down counter**

Phase Shifter Guided by Up/Down Counter (cont'd)

Up/Down Counter Output

VCO Phase

- **Phase resolution improves by increasing number of bits in the hardware**

Problem: Up/Down Counter Overflows

Up/Down Counter Output

VCO Phase

- **Large negative pulse caused by overflow rotates VCO phase by a large step in the wrong direction**

- **Phase shifter provides a phase range of only 2π**

Solution: Add Overflow Signal to Output
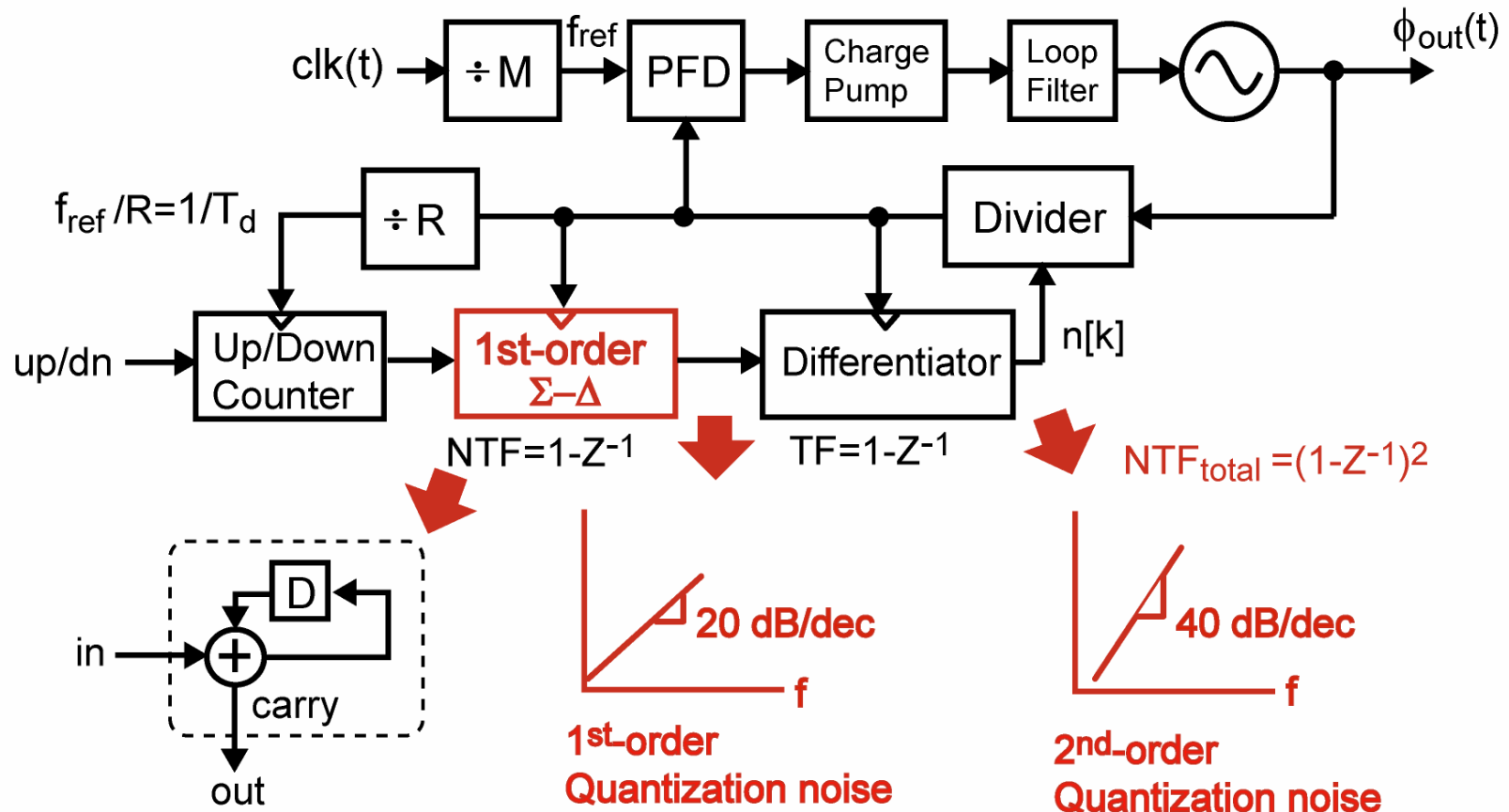

Up/Down Counter Output

VCO Phase
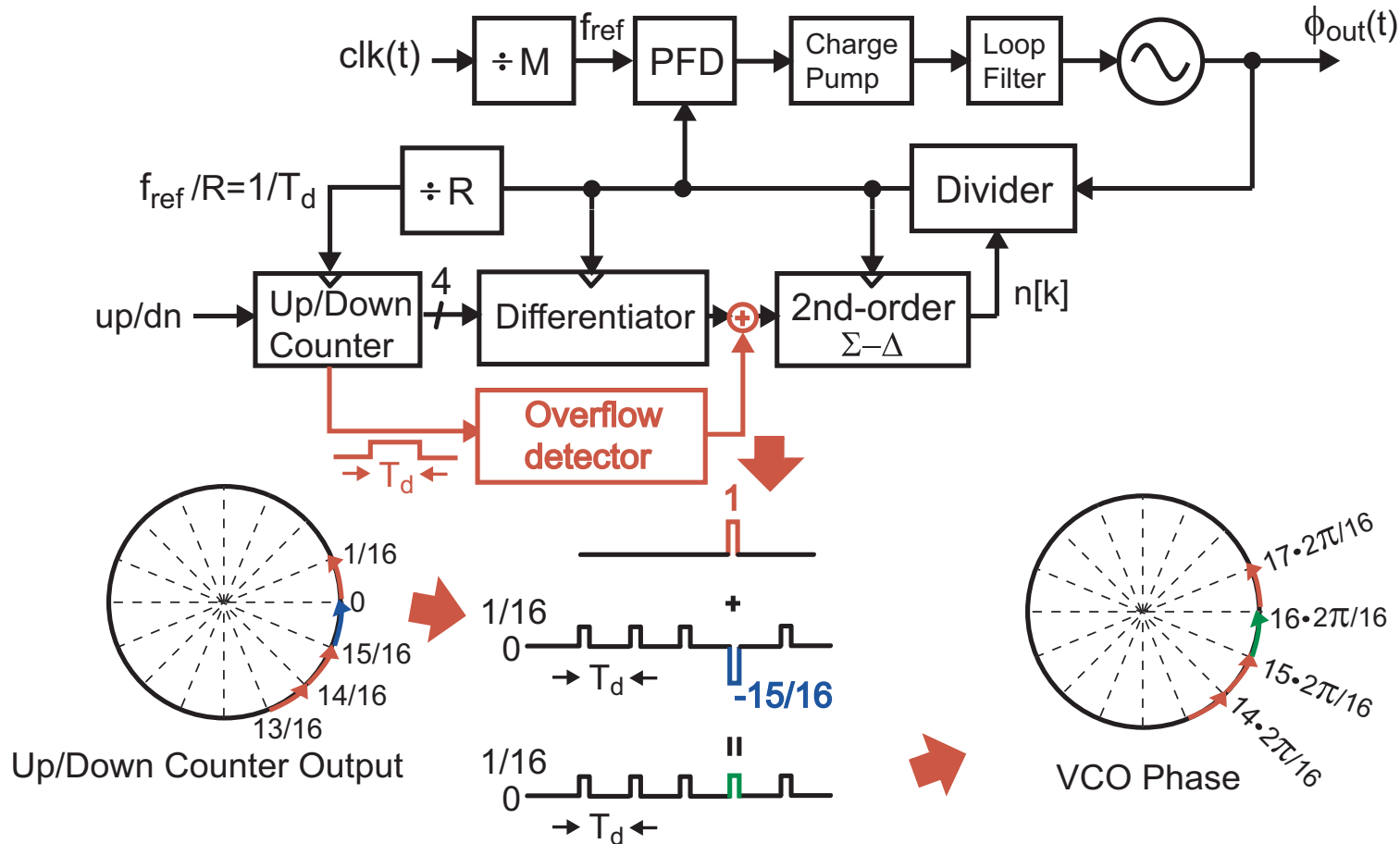
- **Generate a +1 pulse to cancel the undesired -15/16 pulse**
- **Phase shifter provides an infinite phase range**

Quantization Noise of Phase Shifter
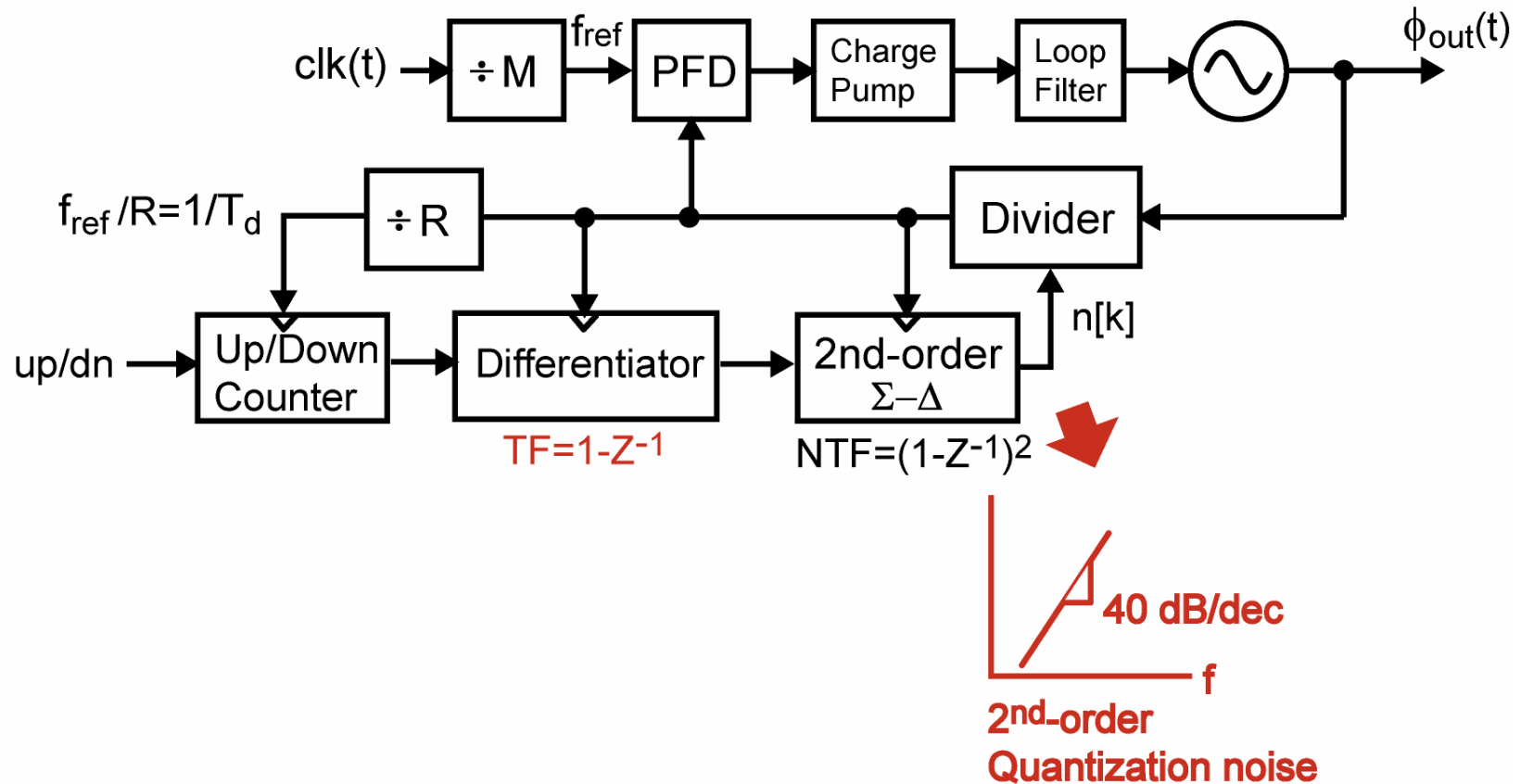
- **Second-order quantization noise exists**
- **Transfer function of a differentiator is the same as noise transfer of a first-order Σ-Δ modulator**
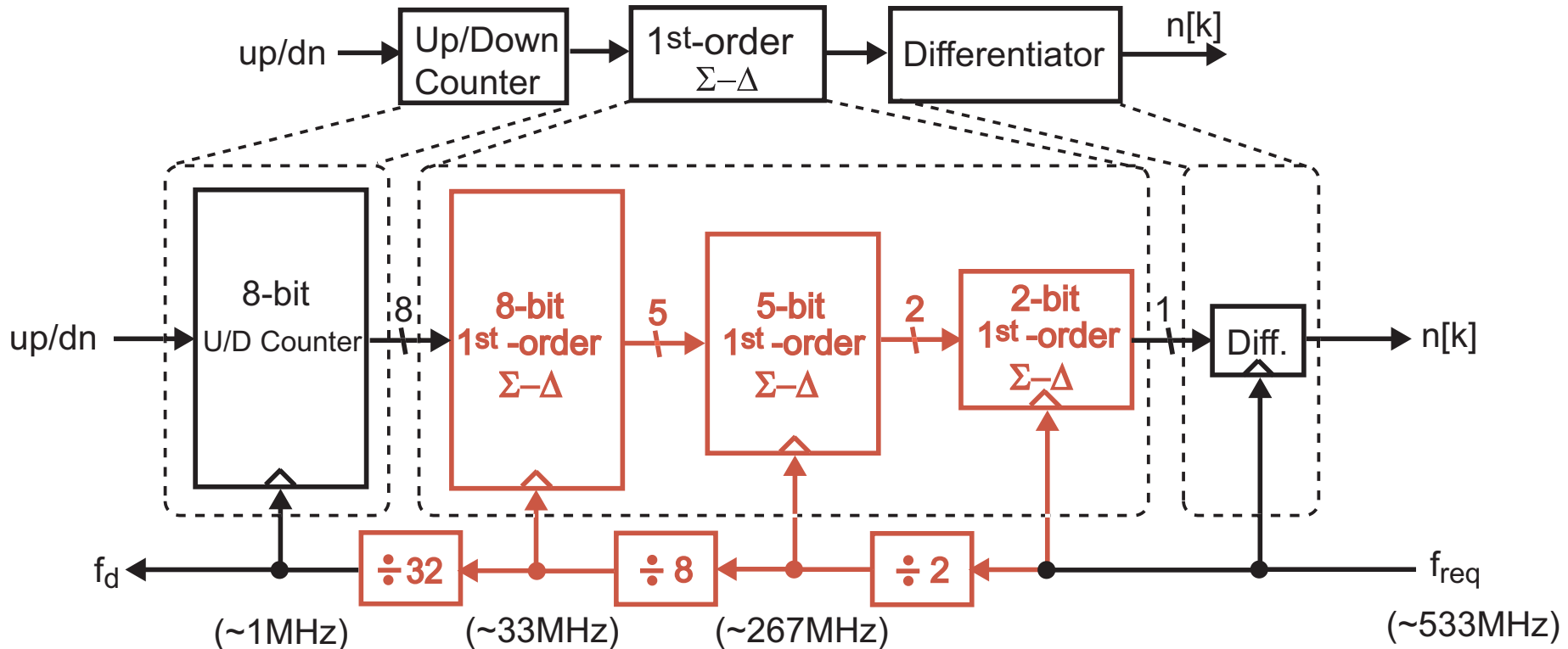
Quantization Noise of Phase Shifter (cont'd)

- **Change the order of differentiator and modulator**
- **Same quantization noise obtained with a first-order Σ-Δ modulator** ➡ **Less circuit complexity**

Proposed Σ-Δ Modulator
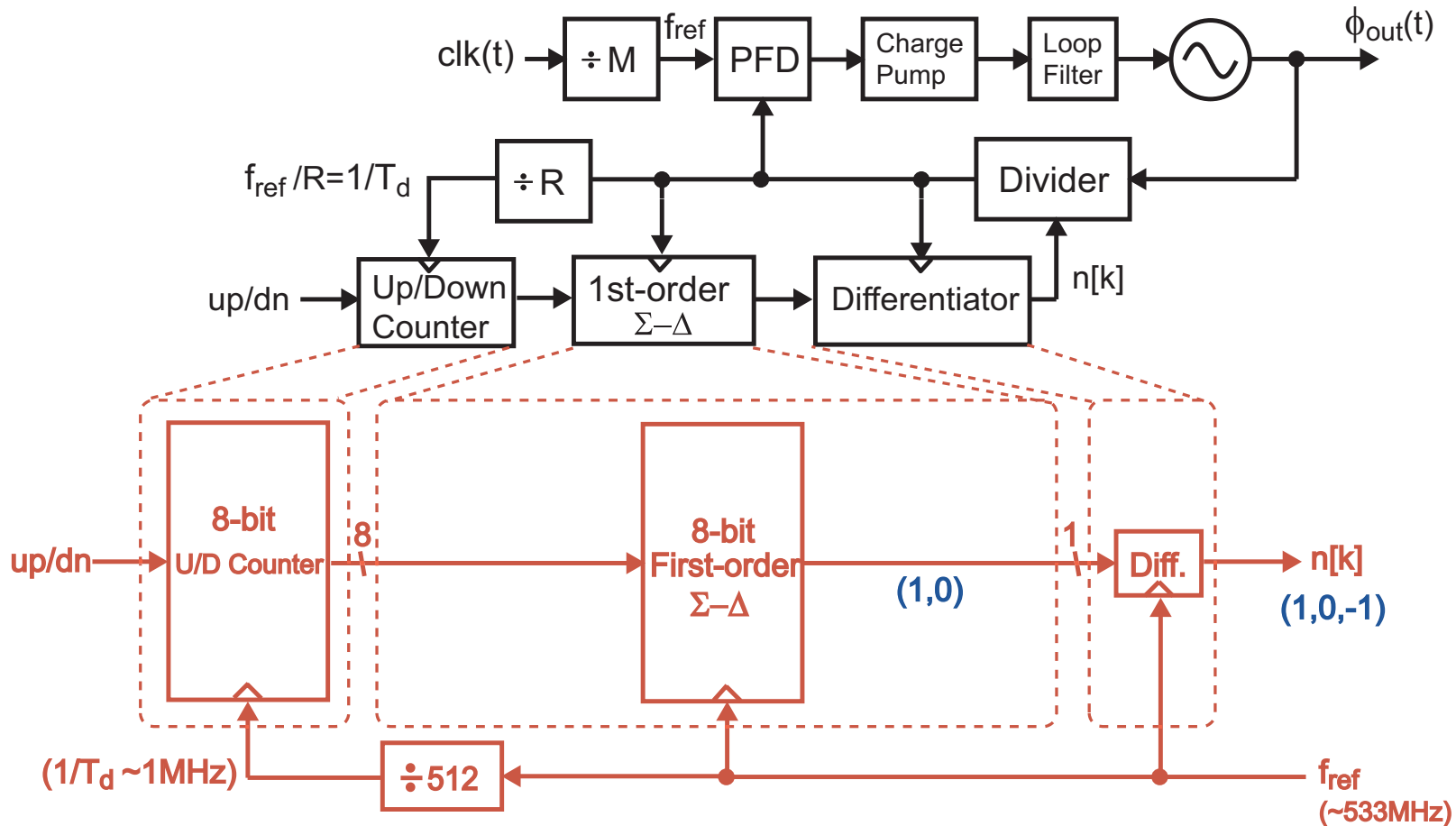
- **Output is three-value (1,0,-1)**
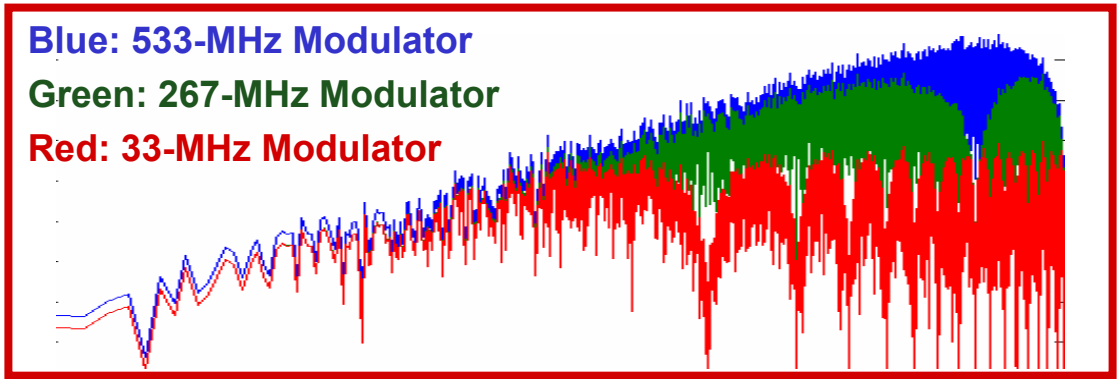- **Divider with three division ratios (N-1, N, N+1) is necessary**
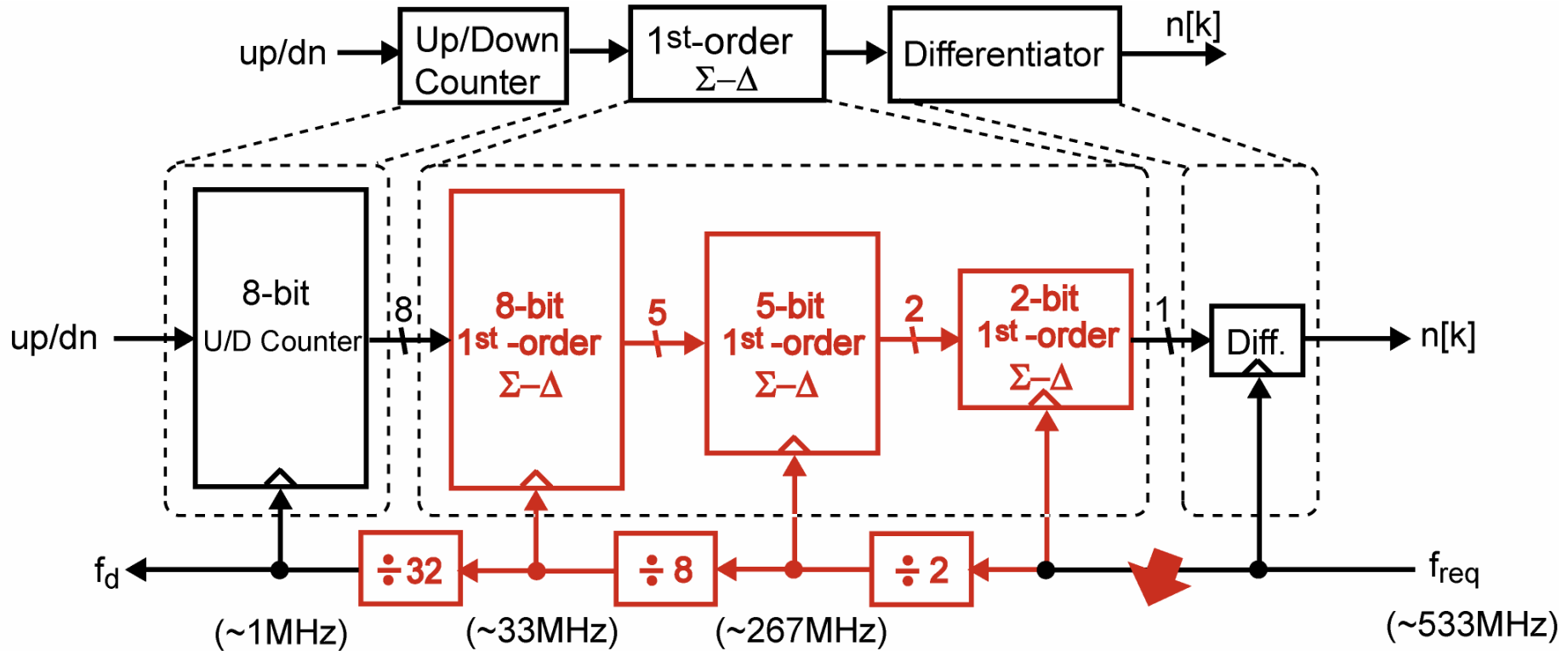
Proposed Σ-Δ Modulator (cont'd)

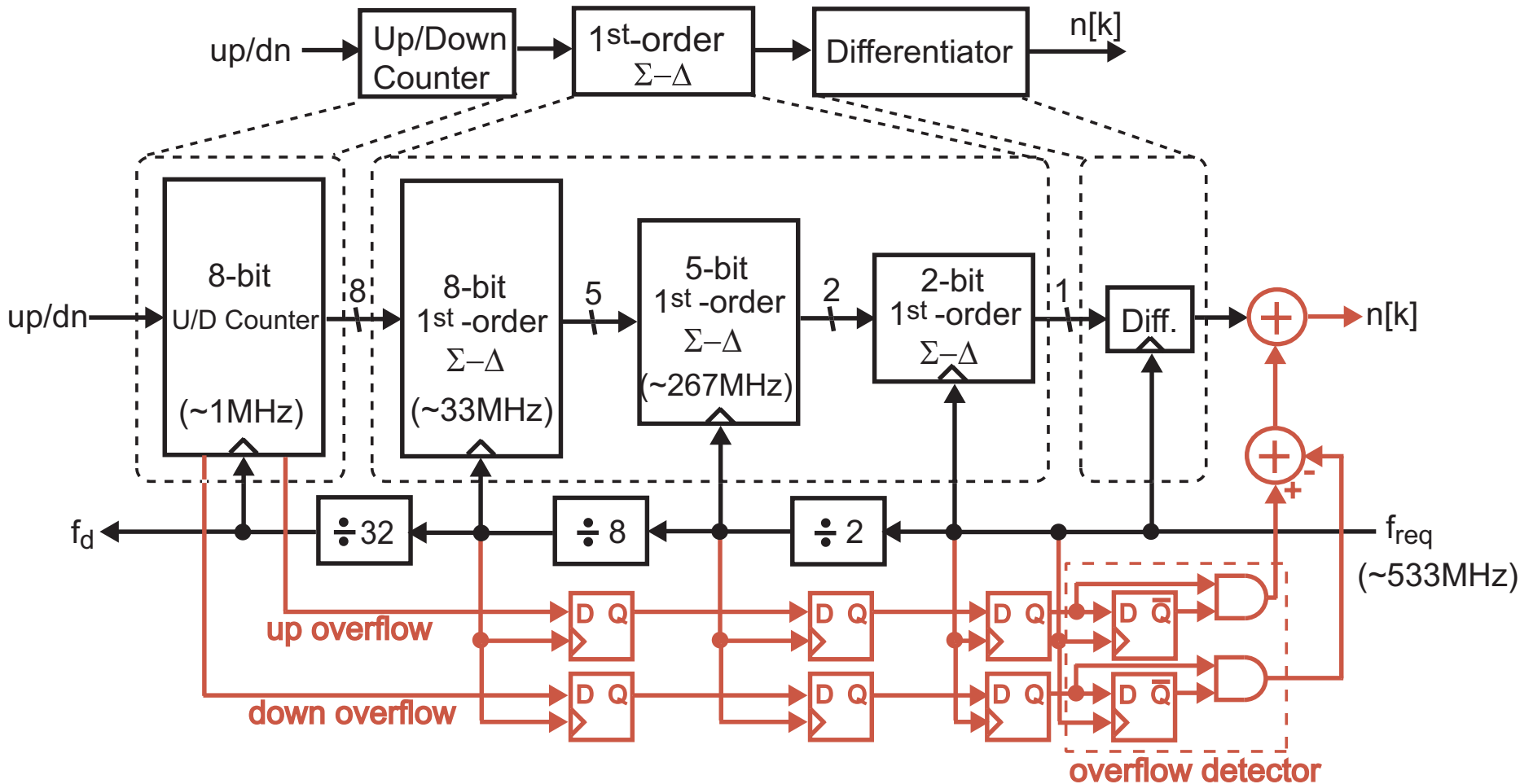- **Multiple first-order Σ-Δ Modulators are used**
  - **Bit number decreases as operating frequency increases**
  - **Metastability and synchronization problems are avoided**

Easy Design and low power

Proposed Σ-Δ Modulator (cont'd)

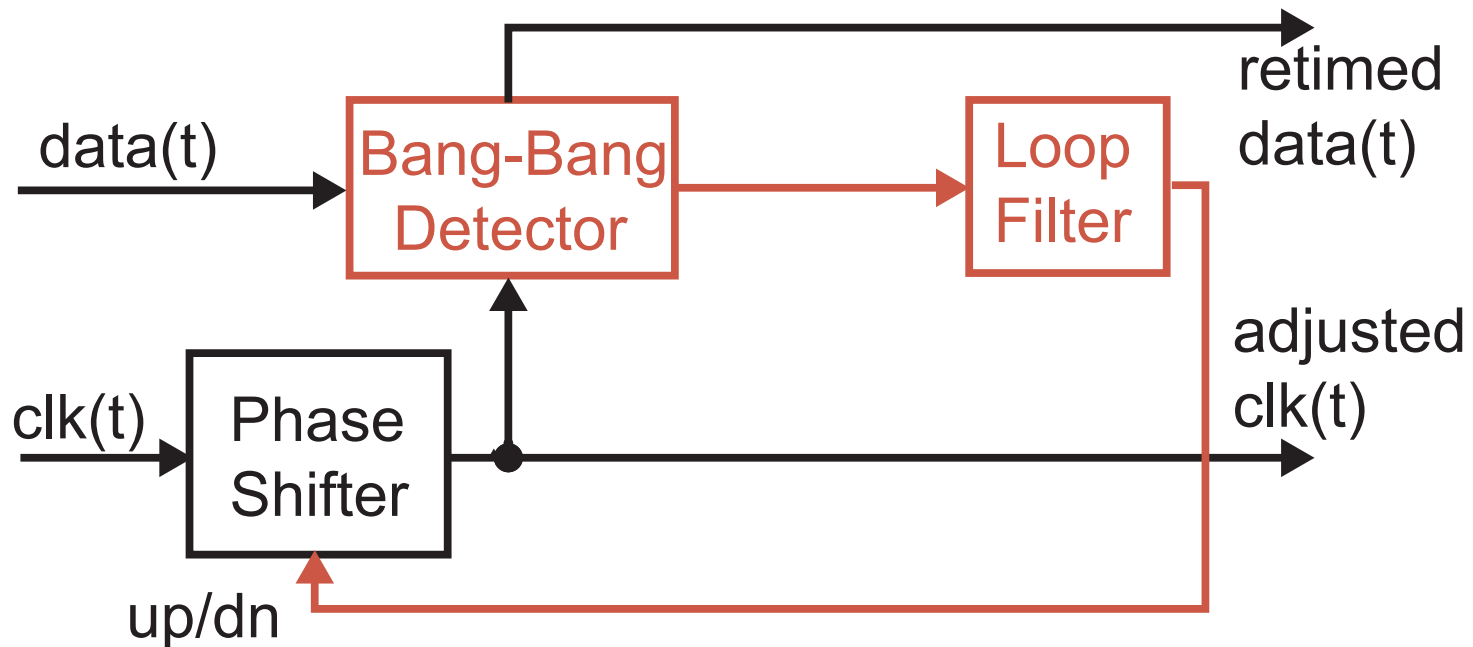# Proposed Σ-Δ Modulator (cont'd)

- **Overflow signals are realigned to main signals in each domain**
- **Output is still three-value even with the extra adder**

Proposed DLL

- **Use Bang-Bang detector for phase comparison**

Proposed Bang-Bang Architecture
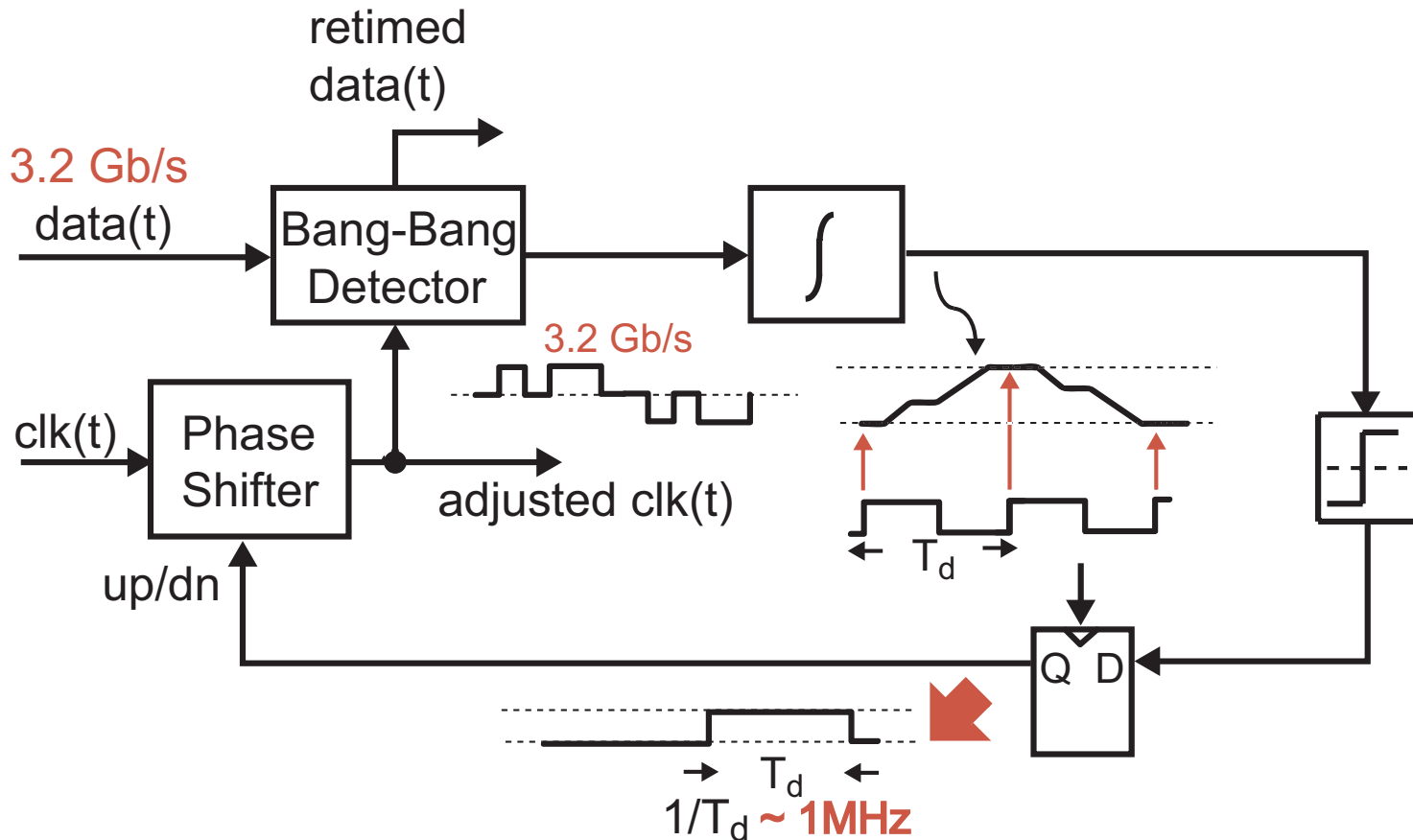
- **An analog integrator, whose output is saturated to VDD or GND, is used to accumulate bang-bang detector output**

DLL Prototype Chip for 3.2 Gb/s Communication
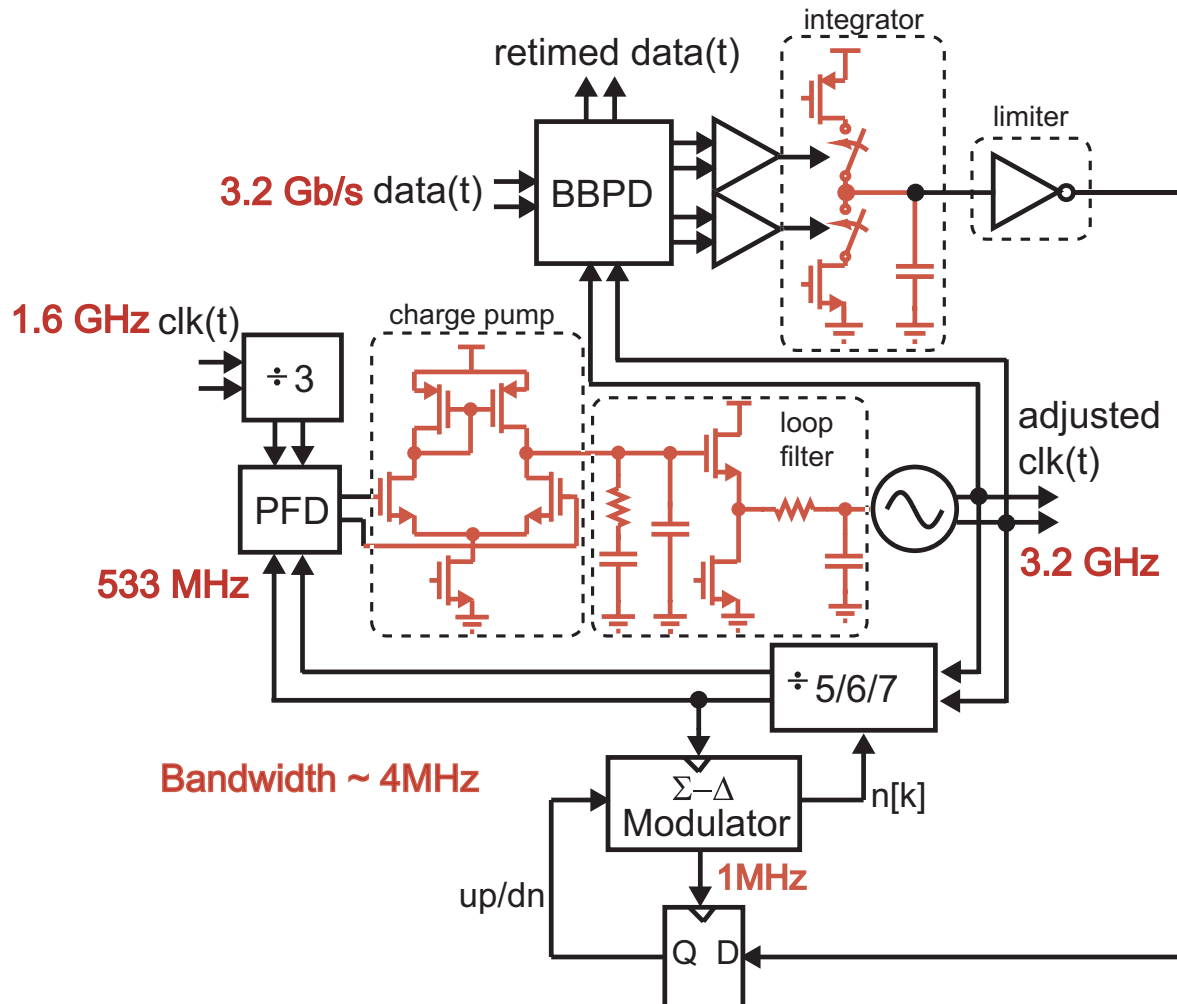
- **8-bit Σ-Δ modulator → 1.4° phase resolution**
- **Simple analog components without need of good matching**

Chip Microphotograph

- **Implemented by 0.18um CMOS Process**
- **Core Area:**
  600um X 700 um
- **1.8 V, 55 mA (excluding I/O buffer)**

DLL Measured Jitter
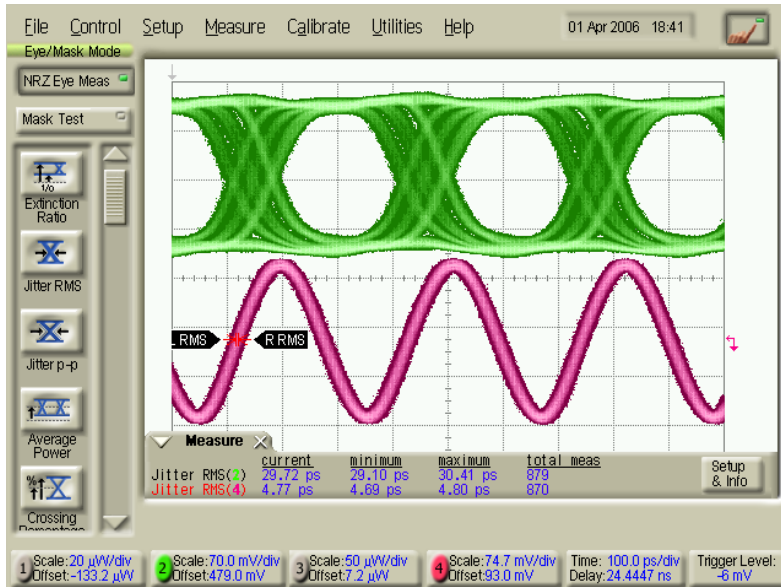
- **Left: 3.2Gb/s PRBS 2^{31}-1**
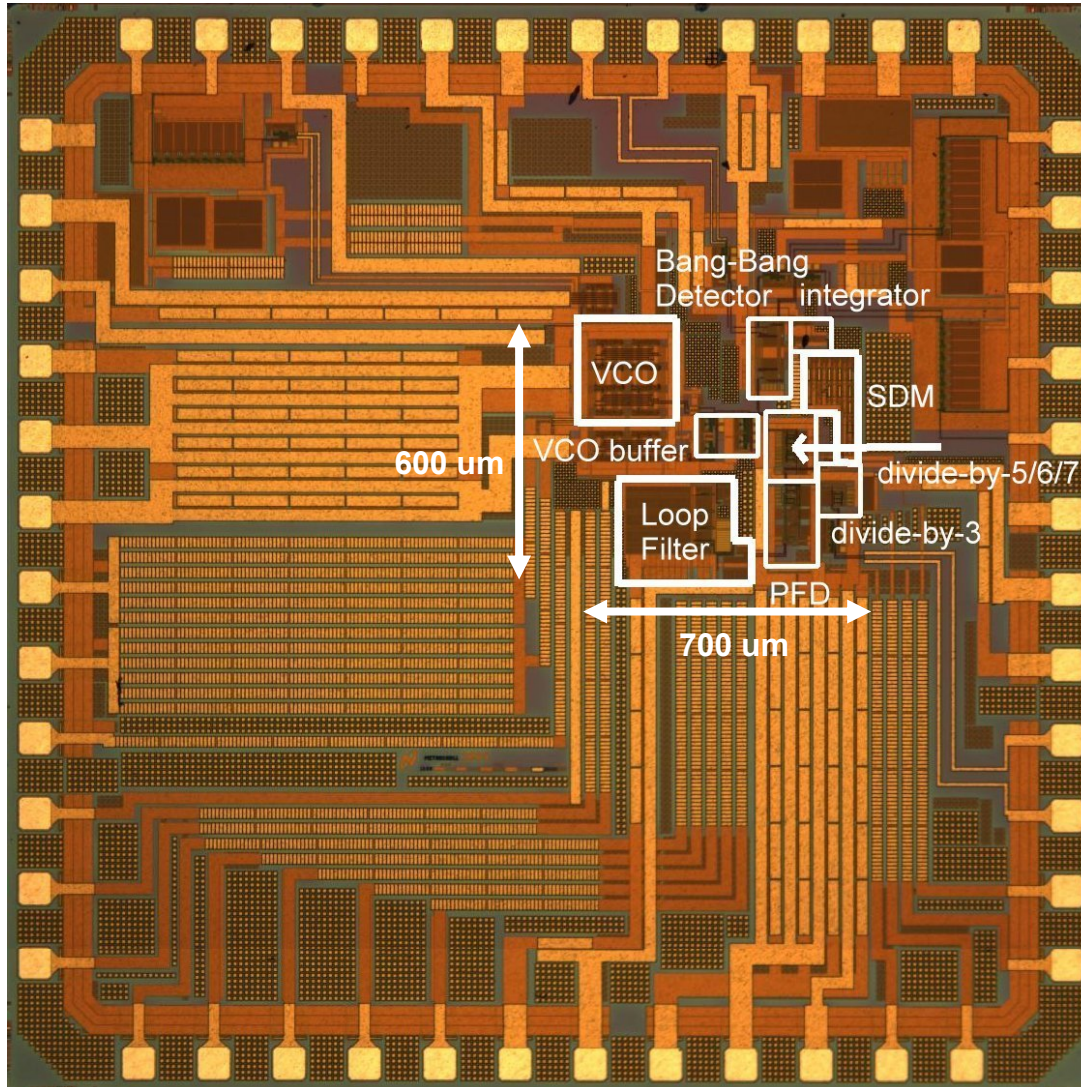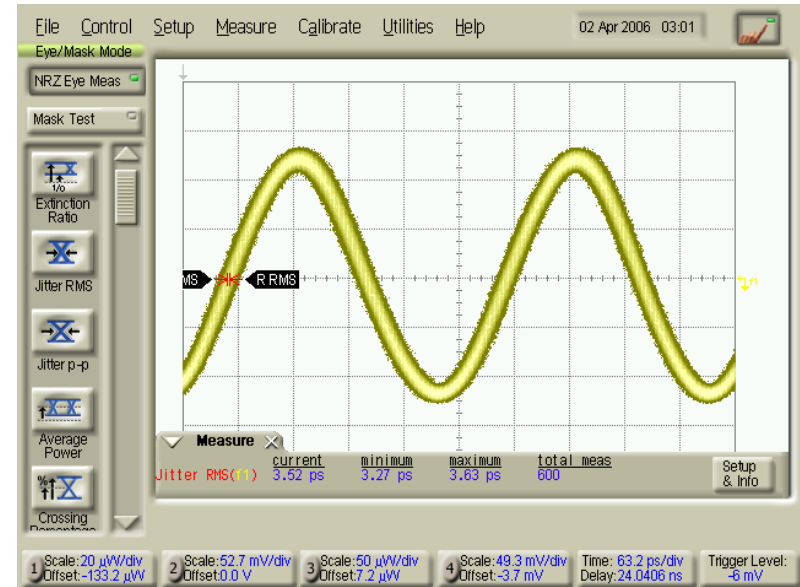 - **Single-ended clock jitter < 4.8ps**
  - **Single-ended data jitter < 30.5ps**
- **Right: 3.2Gb/s PRBS 2^{31}-1**
  - **Differential clock Jitter < 3.7ps**
- **BER < 10^{-12}**

From Measurement
3.4 ps from thermal noise (mainly from VCO and pump)

From Behavior Simulation
jitter due to bang-bang detector and $\Sigma-\Delta$ modulator is on the same order as the thermal noise

Remaining Jitter
probably from output buffer

Non-ISI-limited DLL Jitter

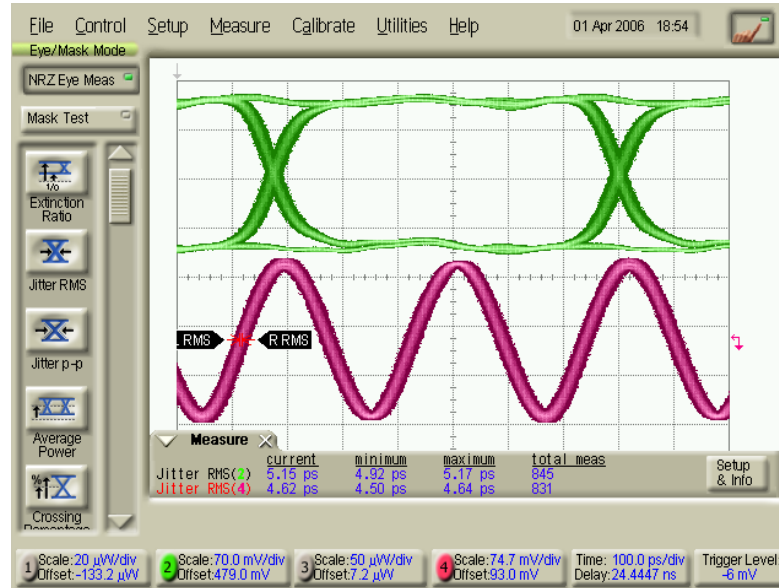- **1.6Gb/s PRBS 2^7-1**
  - **Single-ended clock Jitter < 4.7ps**
  - **Single-ended data jitter < 5.2ps**
- **BER < 10^{-12}**

Conclusion

- **A DLL architecture is proposed**
  - Σ-Δ synthesizer is used as the phase shifter
  - A compact and low-power Σ-Δ modulator
  - Simple Bang-bang detector is used for phase detection
- **Prototype is implemented for 3.2 Gb/s chip-to-chip communication**
- **The DLL provides a digitally-controlled phase adjustment with fine-resolution and infinite-range that is not sensitive to PVT variations**
- **The overall architecture is insensitive to mismatch**
  - Well suited for more advanced CMOS processes with high variability

Low Jitter, Highly Digital, MDLL-based Clock Multiplier

Belal M. Helal, Matthew Z. Straayer, Gu-Yeon Wei[*] and Michael H. Perrott

# *Motivation*

- **Issue: Clock multiplication using phase-locked loops complicates the design of digital chips.**

- **Goal: Achieve a highly digital clock multiplier that can be easily ported across different CMOS processes.**
 - **Do not compromise on jitter performance**
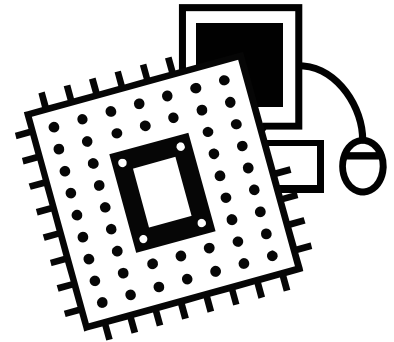
We will present a non-PLL based clock multipliers that achieves sub-ps jitter performance

PLL: Typical Architecture for Clock Multiplication
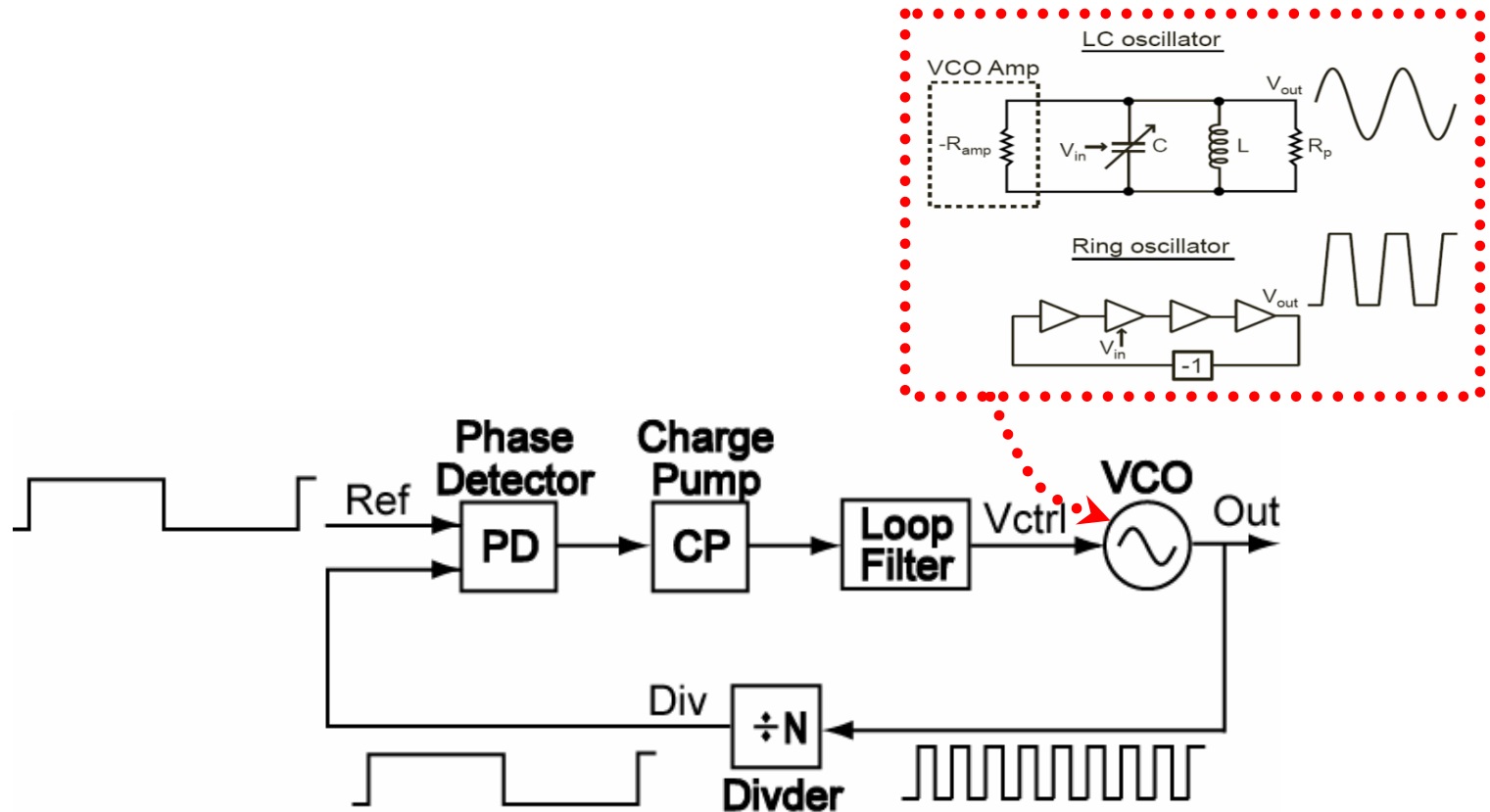
- **Application determines VCO type**
  - **Lowest noise** → **LC oscillator**
  - **Smallest area** → **Ring oscillator**

- **How to reject the high phase noise of a ring oscillator?**

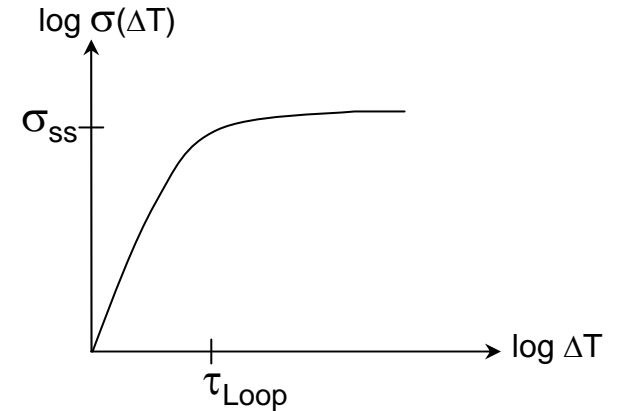# *Rejection of High Phase Noise in Ring Oscillators*
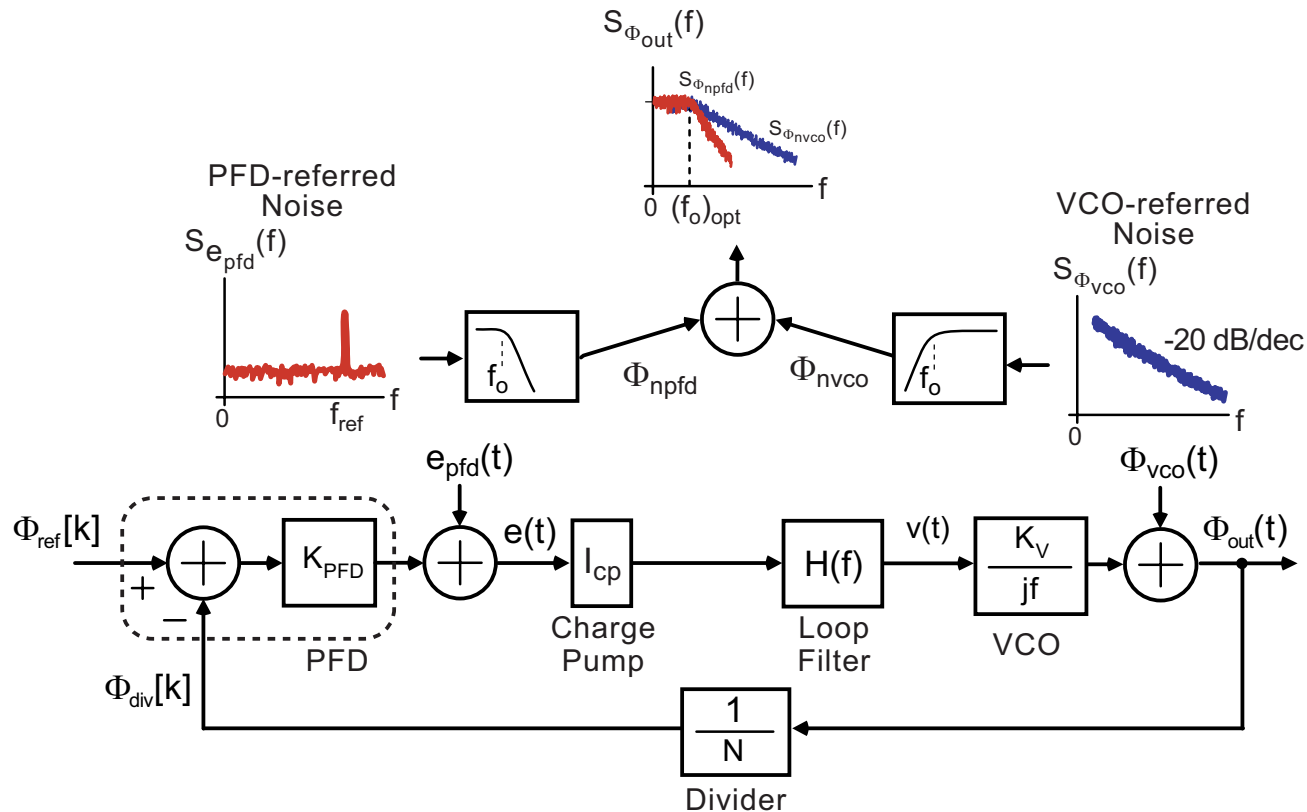
- **Phase noise contributors: VCO and PFD noise**
  - **Affected differently by PLL bandwidth, f_0**
- **VCO noise: high-pass filtered   PFD noise: low-pass filtered**
  - **Tradeoff: bandwidth ↑ → VCO noise ↓ , PFD noise ↑**
- **Can we suppress VCO noise without large bandwidth?**

Time Domain View: Reducing VCO Jitter
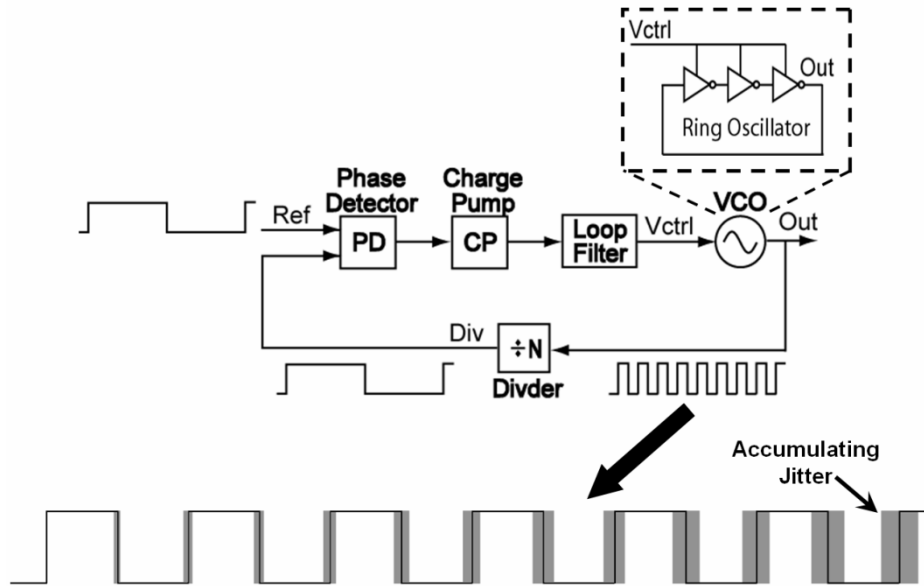
McNeill, *JSSC,*
June 1997

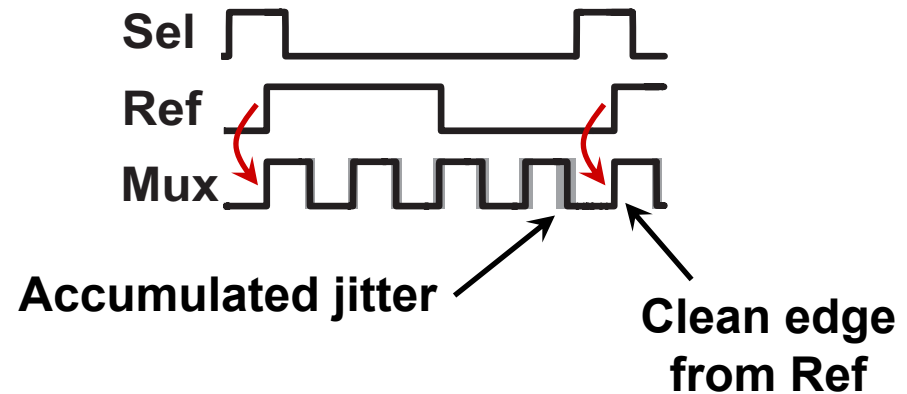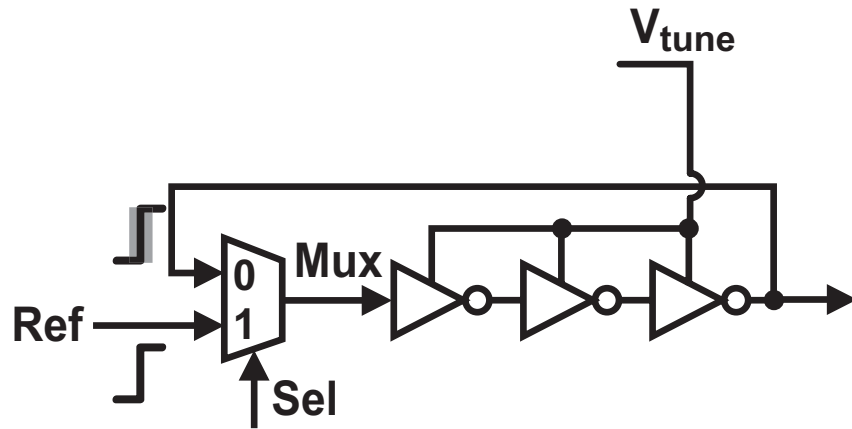- **Problem: Jitter accumulates with time according to loop dynamics to a steady state level, σ_{ss}**

- **Solution: reset jitter at a rate faster than the loop BW**
  - **How?**
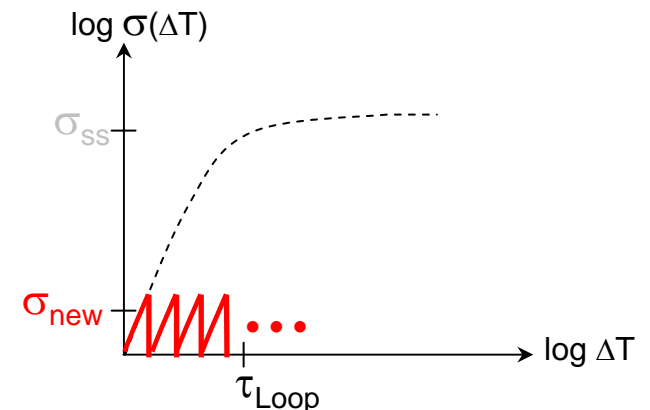
Multiplying DLL Concept

- **Goal: Create a higher frequency clock from an input reference signal**

- **Replace jittery edge with clean Reference edge**
  - **Accumulated jitter is periodically removed**

The Benefit of the MDLL Approach

Ye, Jansson, Galton, *JSSC*, Dec. 2002
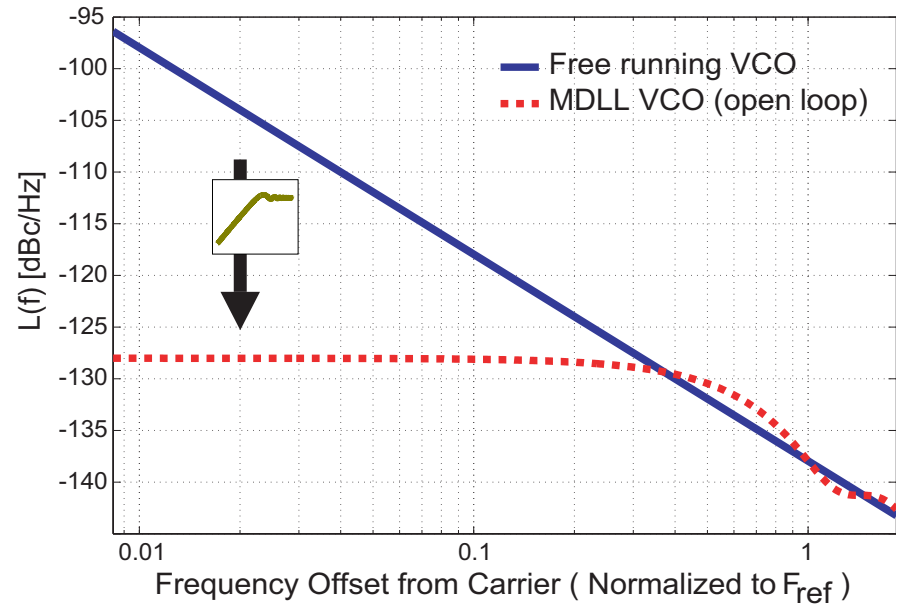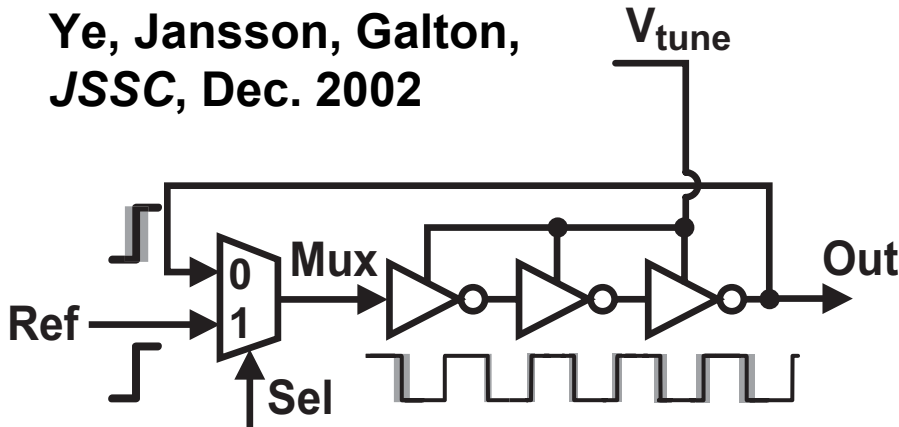
- **Phase noise of ring oscillator is suppressed by the periodic multiplexing of reference edge**
- **Transfer function approximates a 1st order high pass filter**
  - $f_{hpf} \approx f_{Ref} / 4$

High bandwidth suppression of phase noise independent of loop bandwidth

Deterministic Jitter in MDLLs
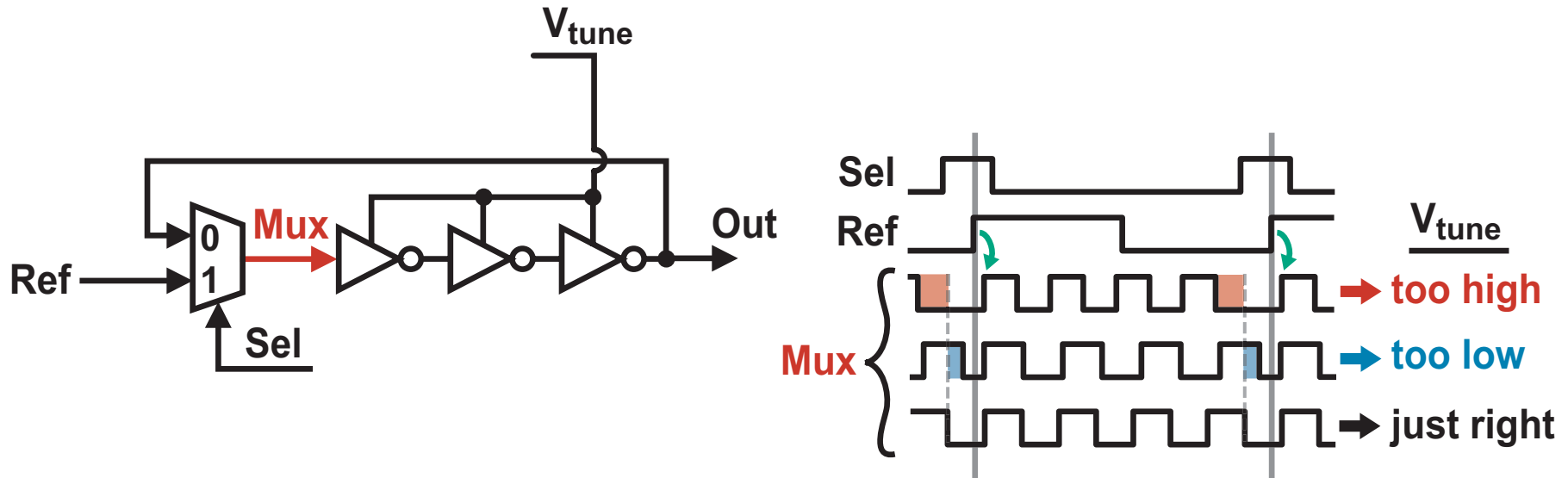
- **Key issue: Need to precisely tune ring oscillator frequency**
- **Offset in frequency results in inconsistent period**
  - **→ deterministic jitter**

Goal: Reduce deterministic jitter to the level of random jitter

Deterministic Jitter Observed in Output Spectrum

- **Deterministic jitter shows up as reference spurs**

- **Relationship by Fourier analysis**

$$\Delta \approx T_{out} \times 10^{Spur(dBc)/20}$$

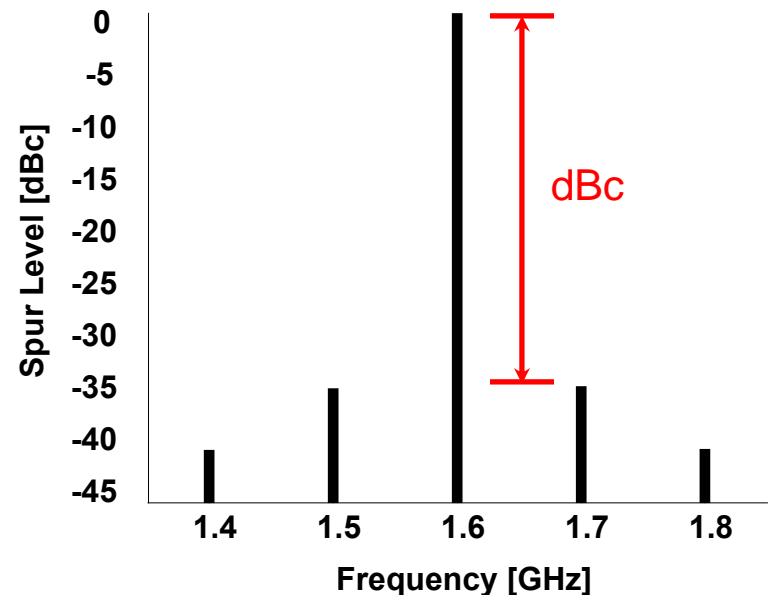**Deterministic Jitter can be estimated from reference spurs**
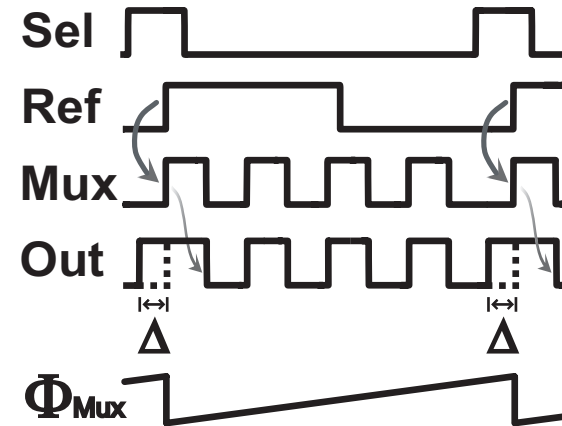
Classical Analog Approach
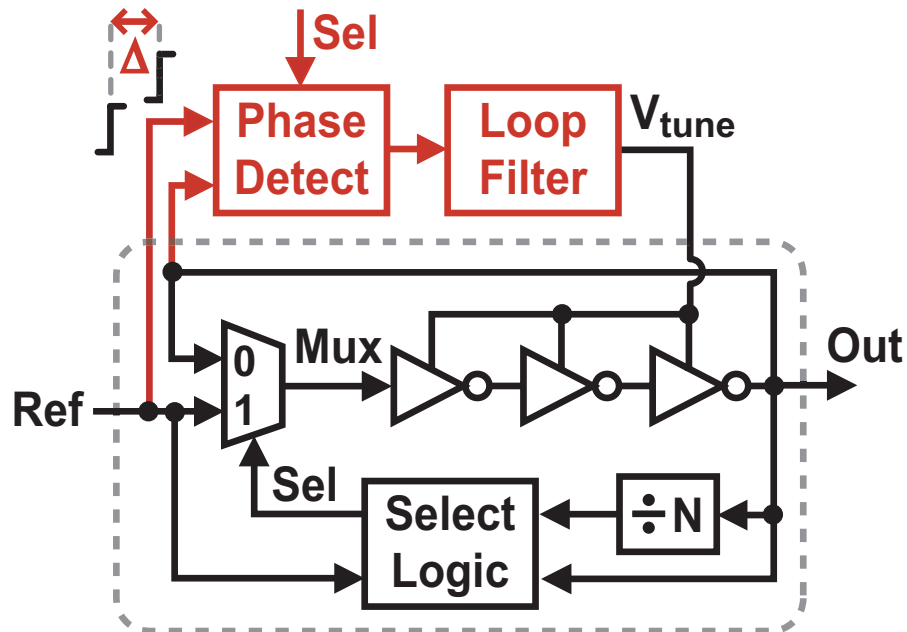
Farjad-Rad et. al., *JSSC*, Dec. 2002.
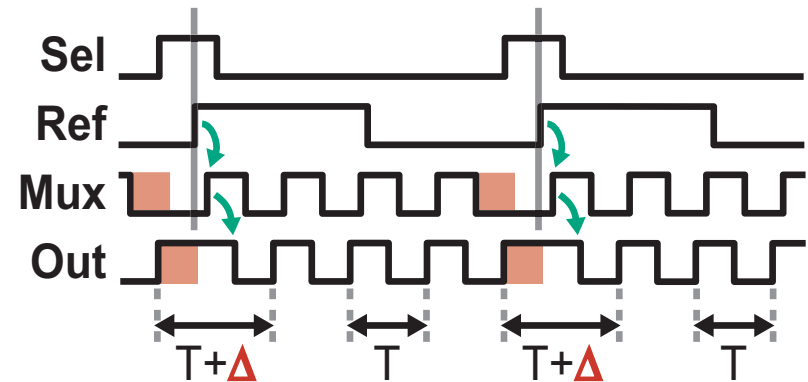
- **Key idea: Compare edges of MDLL output and reference to detect error (Δ)**
  - Integrate error to adjust V_{tune}
- **The problem: Mismatches and offsets in the phase detector and integrator limit reduction of Δ**

Low deterministic jitter is challenging to achieve

Proposed Detection Approach
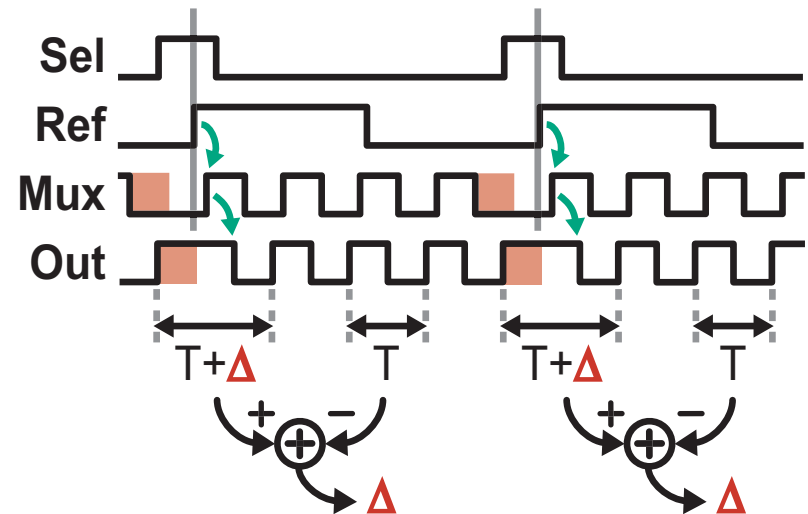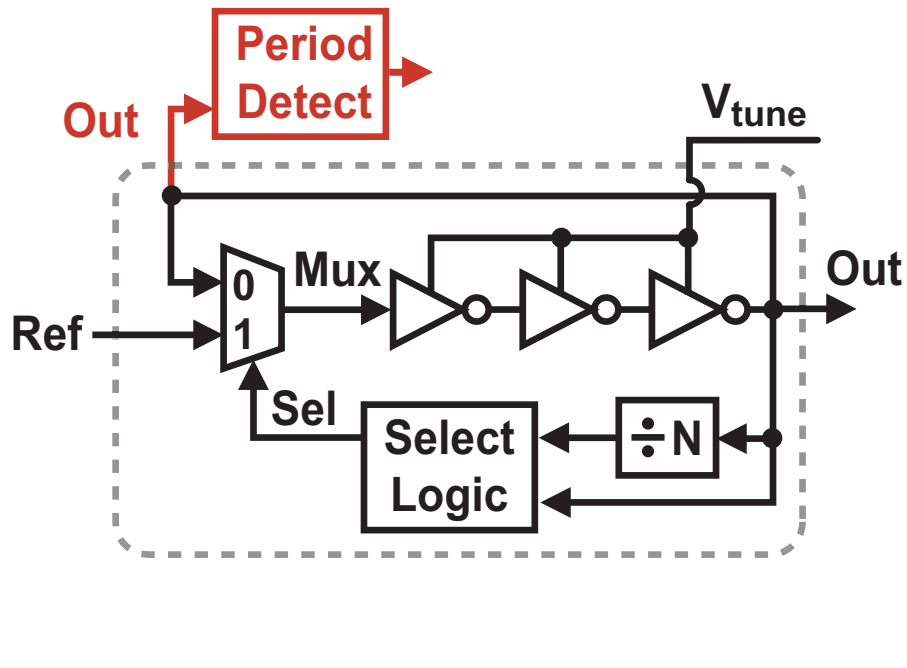
- **Compare cycle periods of MDLL output**
- **Infer error (Δ) *from difference* between cycle periods of the MDLL output**

Comparison of same signal eliminates path mismatch
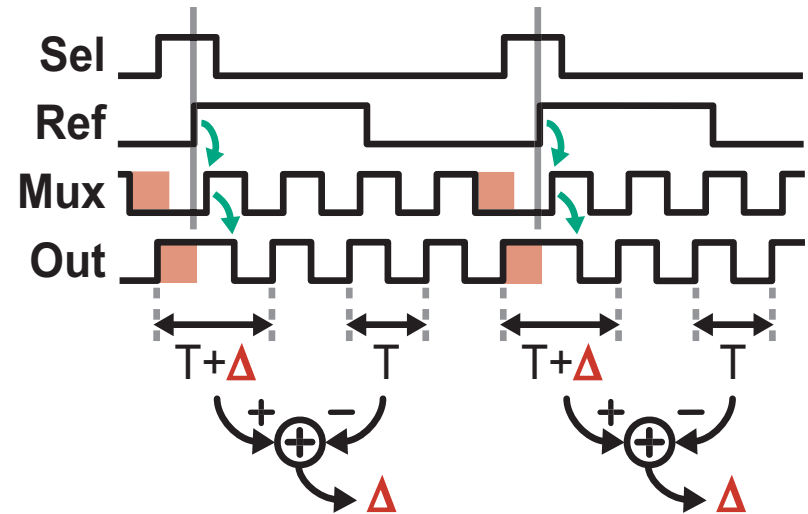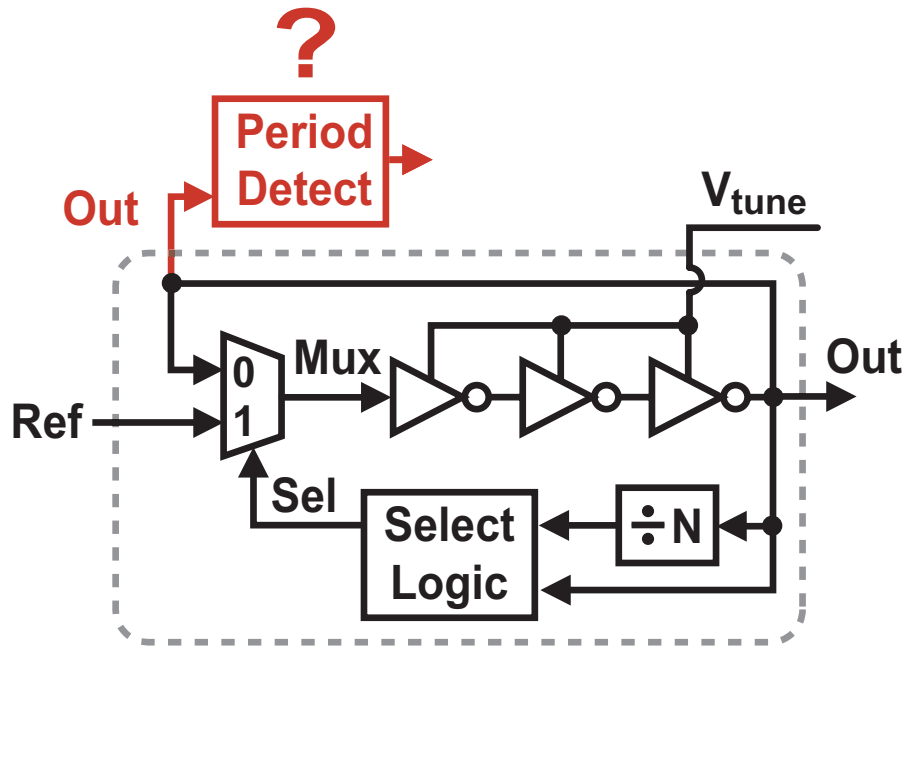
Detection of the Output Period

- **Need an accurate period detector**
  - Error removal is limited by the effective resolution of the detector
- **A digital detector has many advantages**
  - Time-to-digital converter (TDC)

Scrambling TDC (developed by Matt Straayer)
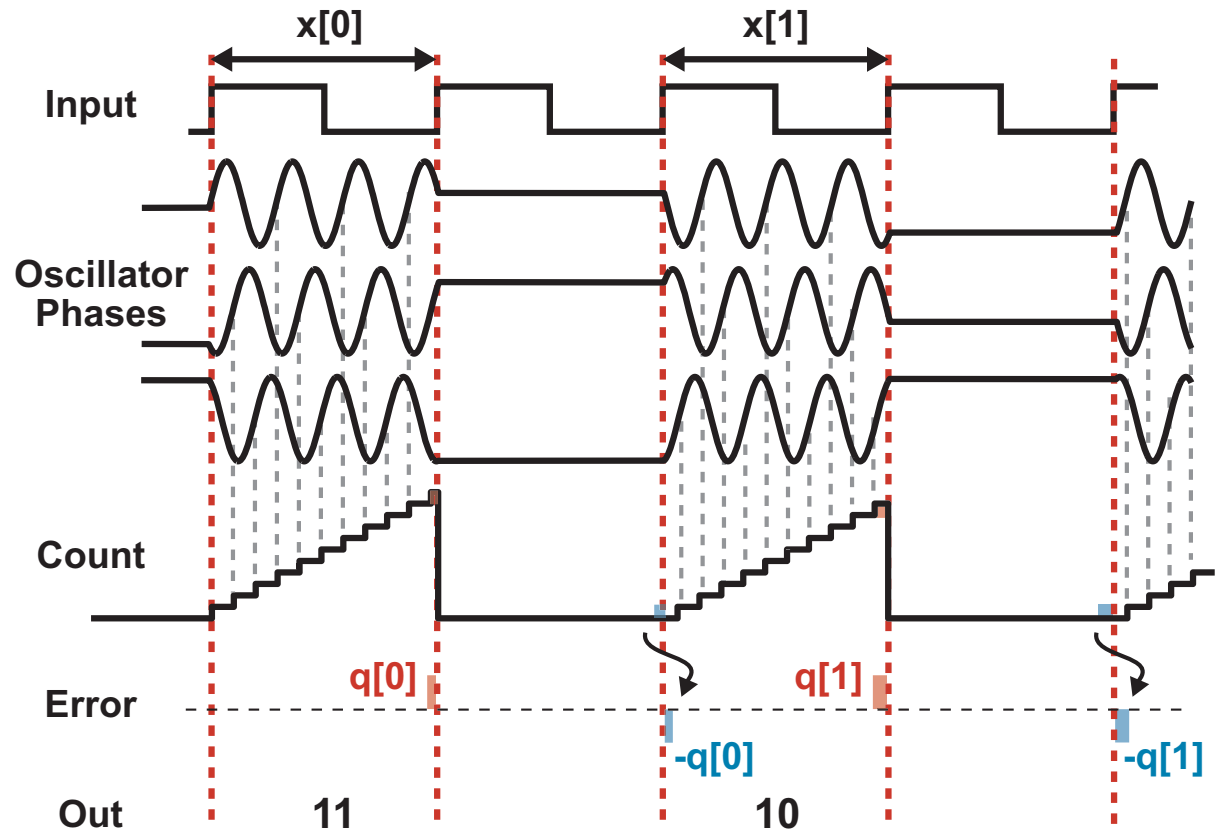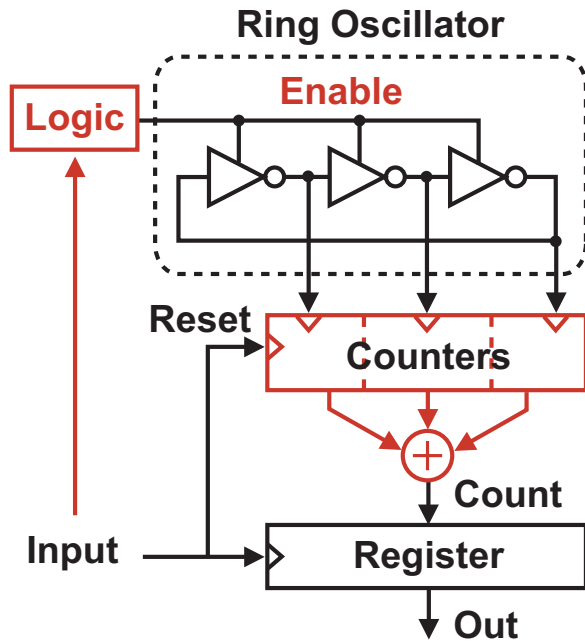
- **Gated Ring Oscillator (GRO) is ON during the measured period**
- **Raw resolution is one inverter delay**
- **Quantization noise is scrambled (and first order noise shaped)**
- **Effective resolution improved by averaging**

Using the GRO in the proposed MDLL Architecture
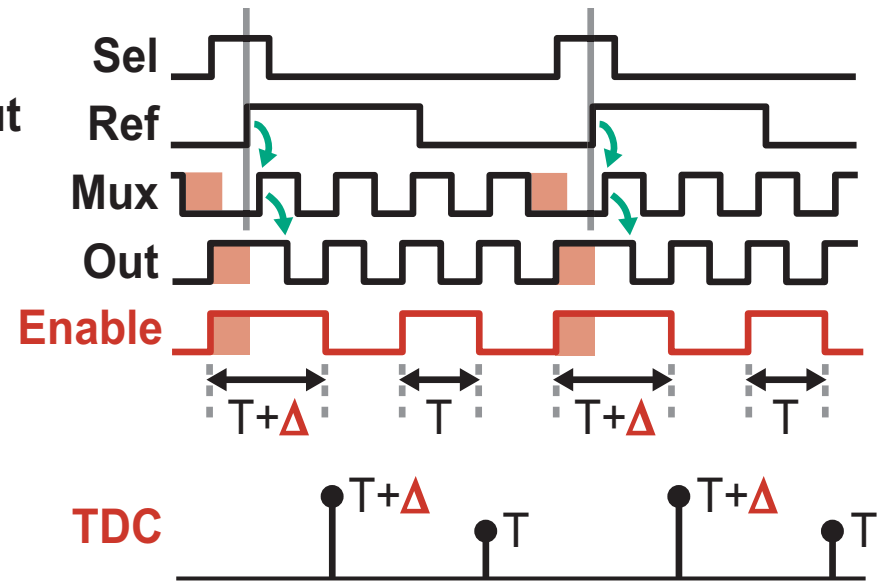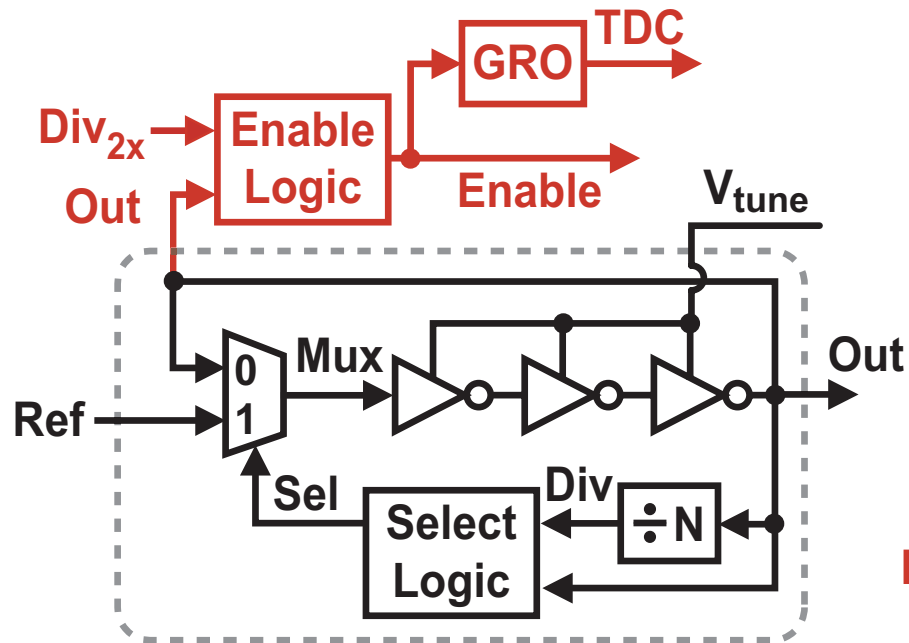
- **Div$_{2x}$ selects two output periods per reference cycle**
- **Sub-picosecond effective resolution is possible**
  - **T$_{gro}$ = 50 ps, Fs = 100 MHz, BW = 10 KHz → Eff. Res. ≈ 0.7 ps**

GRO Detects the Output Period Accurately

Digital Correlator Extracts the Error

- **Digital version of correlated double-sampling technique**

Close the Loop

- **Digital accumulator**
  - **Infinite DC gain**
  - **No DC offsets**
  - **Allows low bandwidth without leakage or large area**
- V_{tune} **adjustment only needs to track thermal variations**
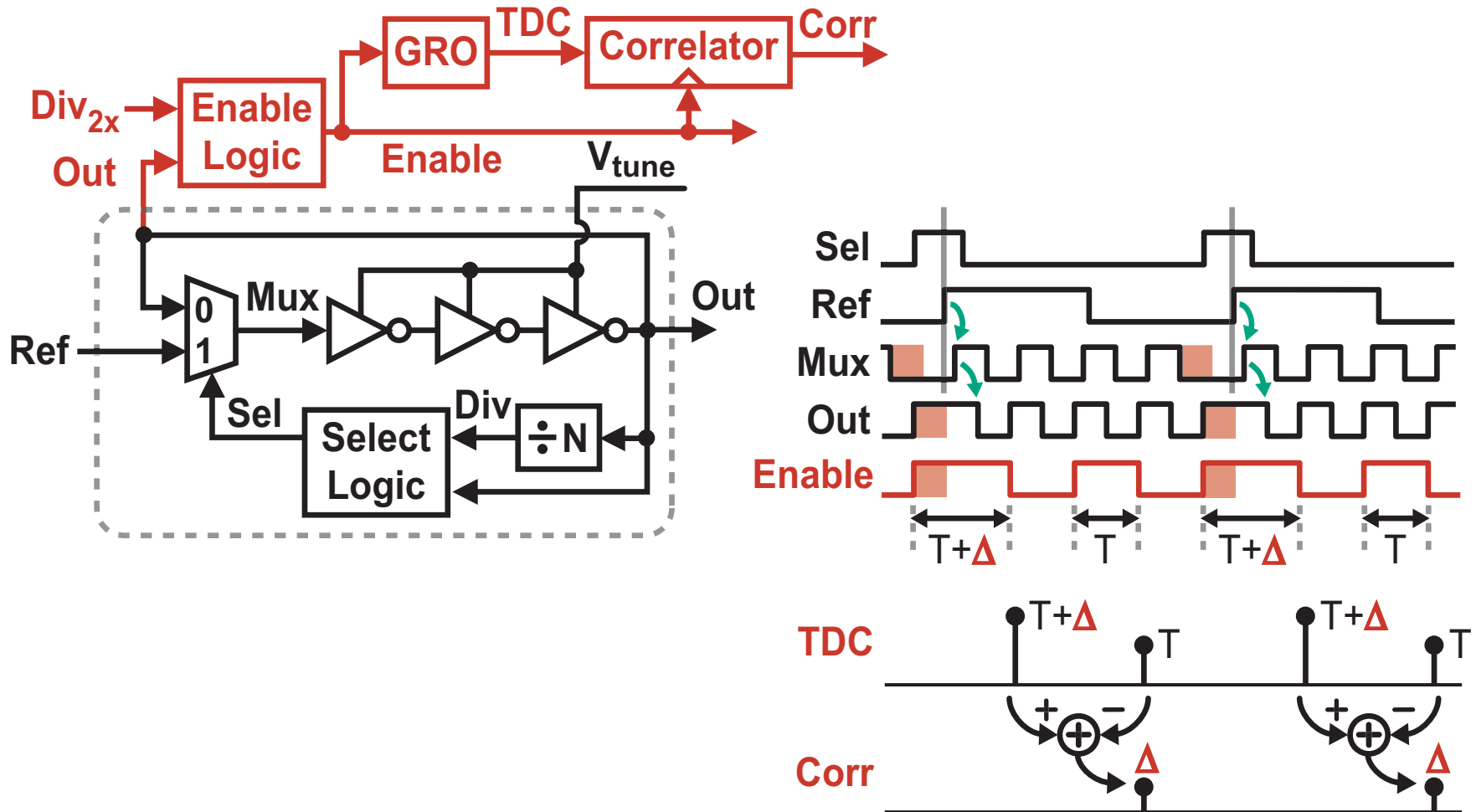
MDLL Prototype
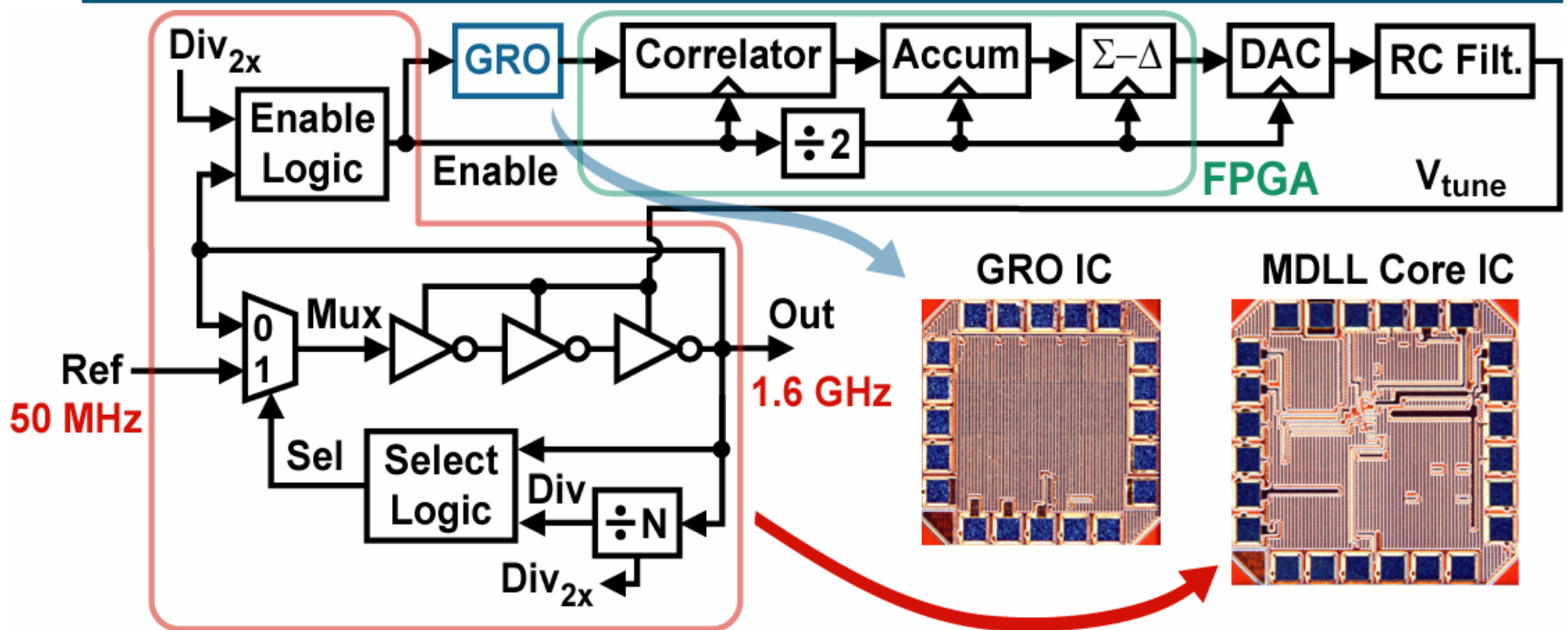
- ■ **Two custom 0.13μm CMOS ICs**
  - − **GRO (Matt Straayer) and core MDLL structures**
- ■ **FPGA**
  - − **Digital Correlator, Accumulator and digital $\Sigma\Delta$-modulator**
- ■ **Discrete 16-bit DAC and RC lowpass filter (3 MHz pole)**
  - − **DAC using 8 effective bits (by using the $\Sigma\Delta$-modulator)**

Power Consumption and Area
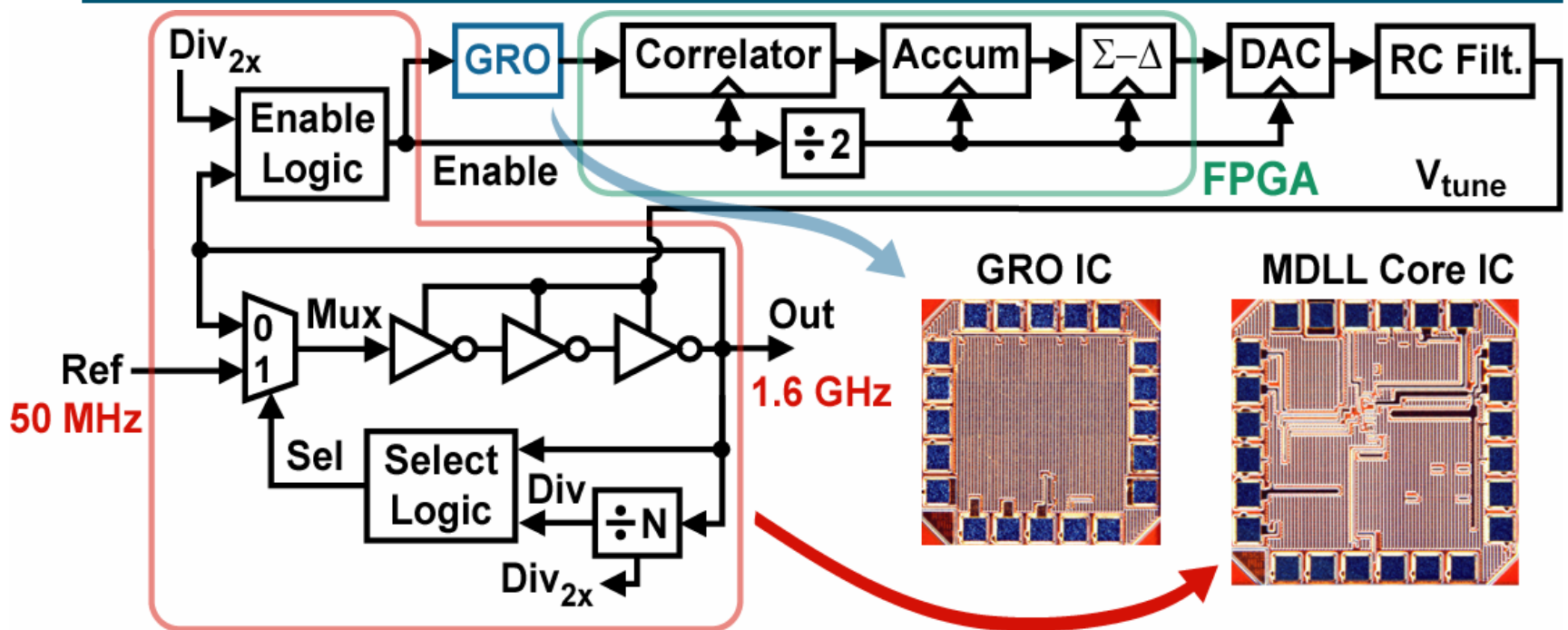
- **Core MDLL**
  - **Area: 0.04 mm^2**
  - **Power: 3.9 mW**

- **GRO-based TDC**
  - **Area: 0.02 mm^2**
  - **Power: 1.2 mW**

Circuit Details

Multiplexed Ring Oscillator
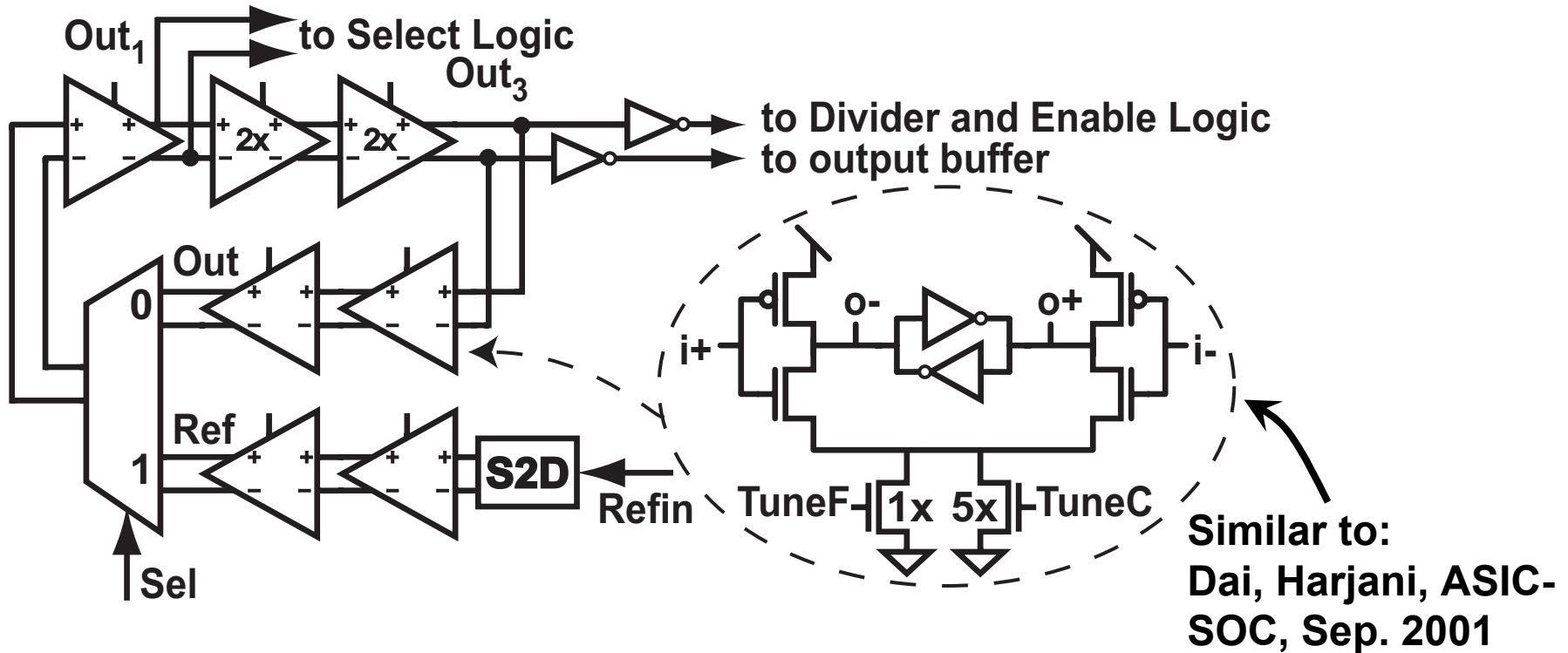
- **Balanced differential loading**
  - **→ Better PSRR and 1/f noise**
- **Five delay stages, no external connections to multiplexer**
  - **→ Faster edges → better multiplexing**

Select Logic and Enable Logic
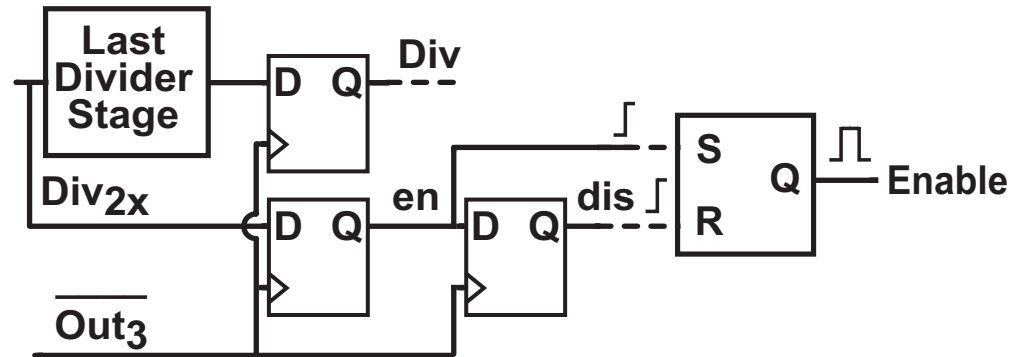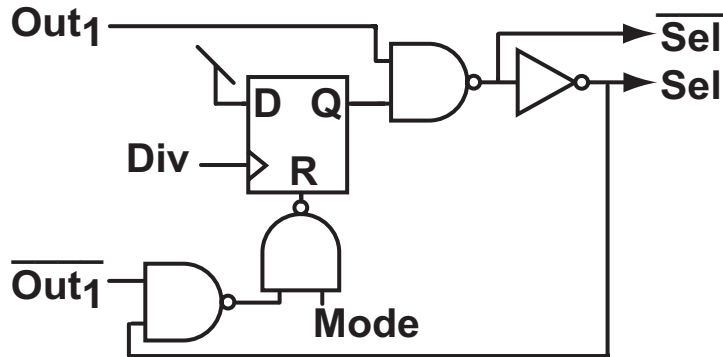
- **Select Logic**
  - **Mostly standard cells**
  - **Relaxed timing**
  - **Sel at middle of output transition**
    - **→ better multiplexing**

- **Enable Logic**
  - **Simple implementation**
  - **Single path detection**

Measured Overall Jitter
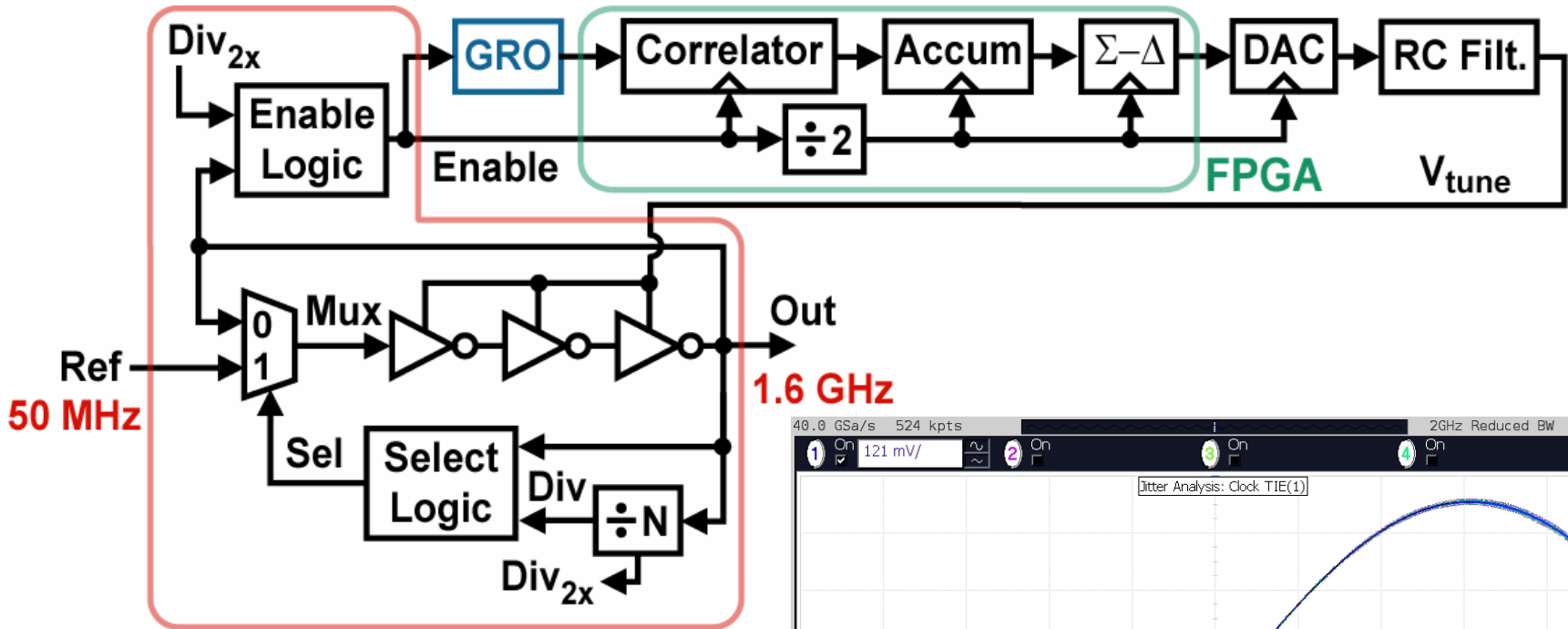
- **Measured overall jitter:**
  - **928 fs (rms)**
  - **11.1 ps (peak-to-peak)**

Sub-picosecond jitter
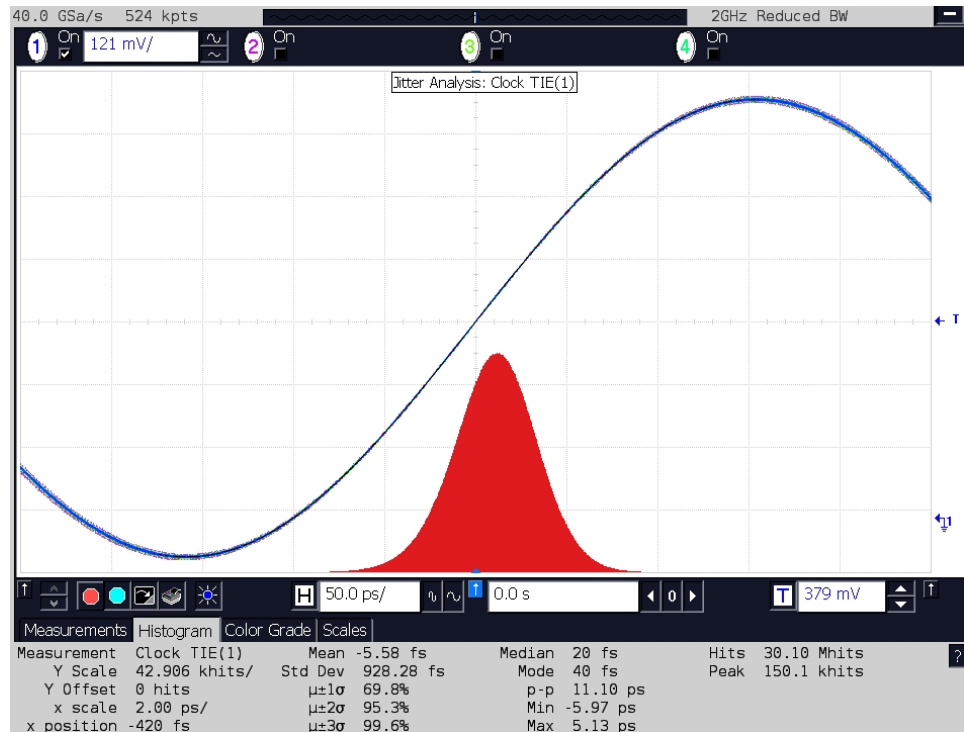
Jitter Estimation from Measured Ref. Spur and Ph. Noise
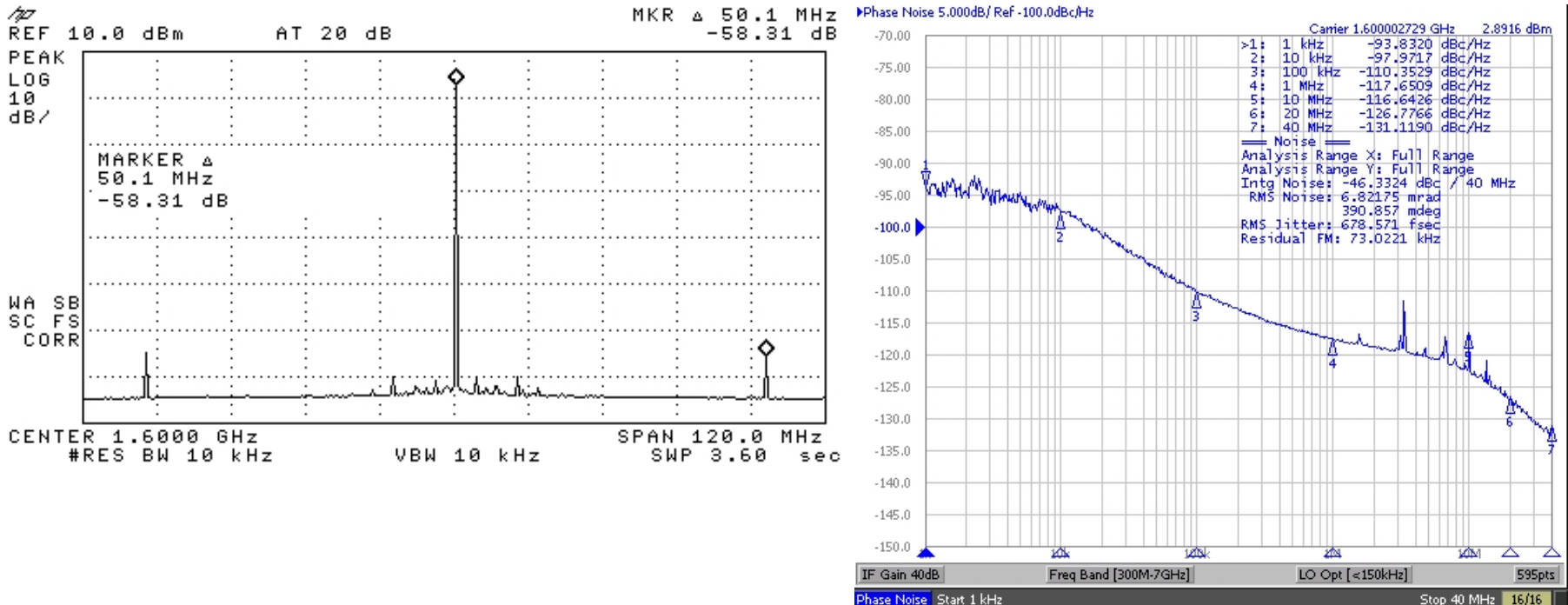
- ■ **Reference spur: -58.3 dBc**
- **→ Deterministic jitter: ≈ 760 fs (peak-to-peak)**
- ■ **Random jitter   :   679 fs (rms)**
  - **From integrated phase noise (1 kHz to 40 MHz)**

Sub-picosecond of estimated random and deterministic jitter

Performance Comparison

	[ISSCC 2002]	[CICC 2006]	[CICC 2006]	This work
Output Frequency (GHz)	2.0	1.216	0.176	1.6
Reference Frequency (MHz)	250	64	8	50
Reference Spur (dBc)	-37	-46.5	-70 (estimated)	-58.3
Deterministic Jitter (ps pp) estimated from meas. Spurs (Figure-of-merit)	7.06	3.89	1.80	0.76

Performance Comparison

	[ISSCC 2002]	[CICC 2006]	[CICC 2006]	This work
Output Frequency (GHz)	2.0	1.216	0.176	1.6
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Deterministic Jitter (ps pp) estimated from meas. Spurs (Figure-of-merit)	7.06 (reported DJ: 12)	3.89	1.80	0.76
Random Jitter (ps rms) from integrated phase noise	N/A	N/A	5 (1.8 simulated) (1 kHz to 10 MHz)	0.68 (1 kHz to 40 MHz)
Overall Jitter	1.62 ps (rms) 13.11 ps (p-p) 25 khits	(@2.16 GHz) 1.6 ps (rms) 12.9 ps (p-p) 12.2 khits	N/A	0.93 ps (rms) 11.1 ps (p-p) 30.1 Mhits
Technology (CMOS)	0.18 μm	0.18 μm	0.18 μm	0.13 μm

Conclusion

- **Digital Period Correlator**
  - Detects tuning error without path mismatch
  - Enables a digital loop filter

- **Highly-digital tuning technique**
  - Avoids analog non-idealities
  - Enables low bandwidth without leakage or large area

- **Highly digital MDLL**
  - 1.6 GHz from 50 MHz reference
  - Significantly-reduced deterministic jitter
  - Sub-picosecond jitter

A Low Noise Programmable Clock Multiplier based on a Pulse Injection-Locked Oscillator with a Highly-Digital Tuning Loop

Belal M. Helal, Chun-Ming Hsu, Kerwin Johnson, and Michael H. Perrott

Motivation
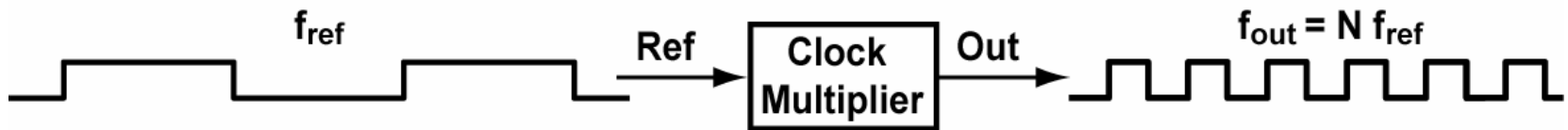
- **Goal: clock multiplication of a clean reference source**
  - **Applications: high performance data links, ADCs, processors, etc.**

- **Our approach: sub-harmonic injection-locking of an LC oscillator**
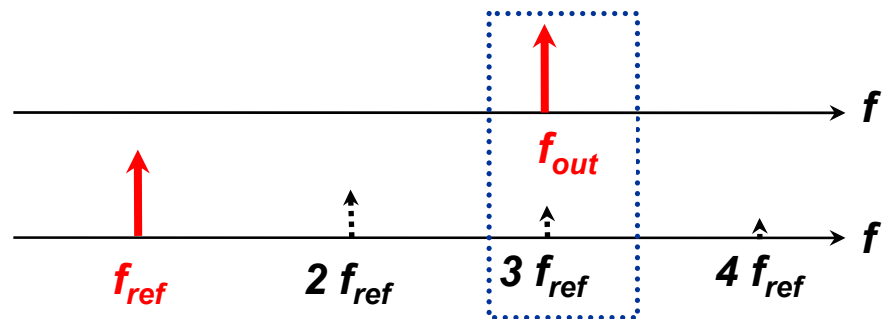
How do we achieve very low jitter levels?

Sub-Harmonic Injection-Locking of an LC Oscillator

[Toso et al., ISSCC 2008]

[Razavi, JSSC 2004]
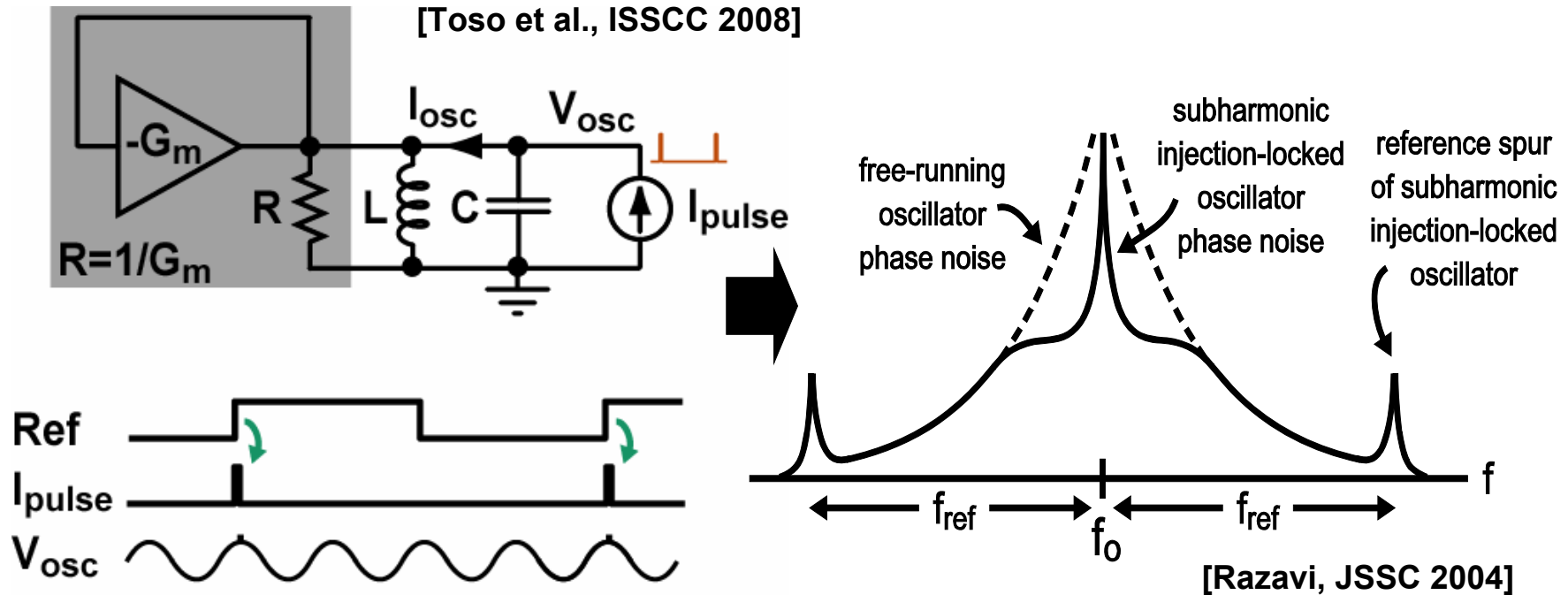
- **Sub-harmonic injection locking can be achieved with current pulses**
  - **Pulses have rich harmonic content to lock to**
  - **Oscillator locks its voltage peaks to the pulses**
  - **Locking bandwidth proportional to the injected charge**

Problems with Current Pulse Injection Locking

[Toso et al., ISSSC 2008]
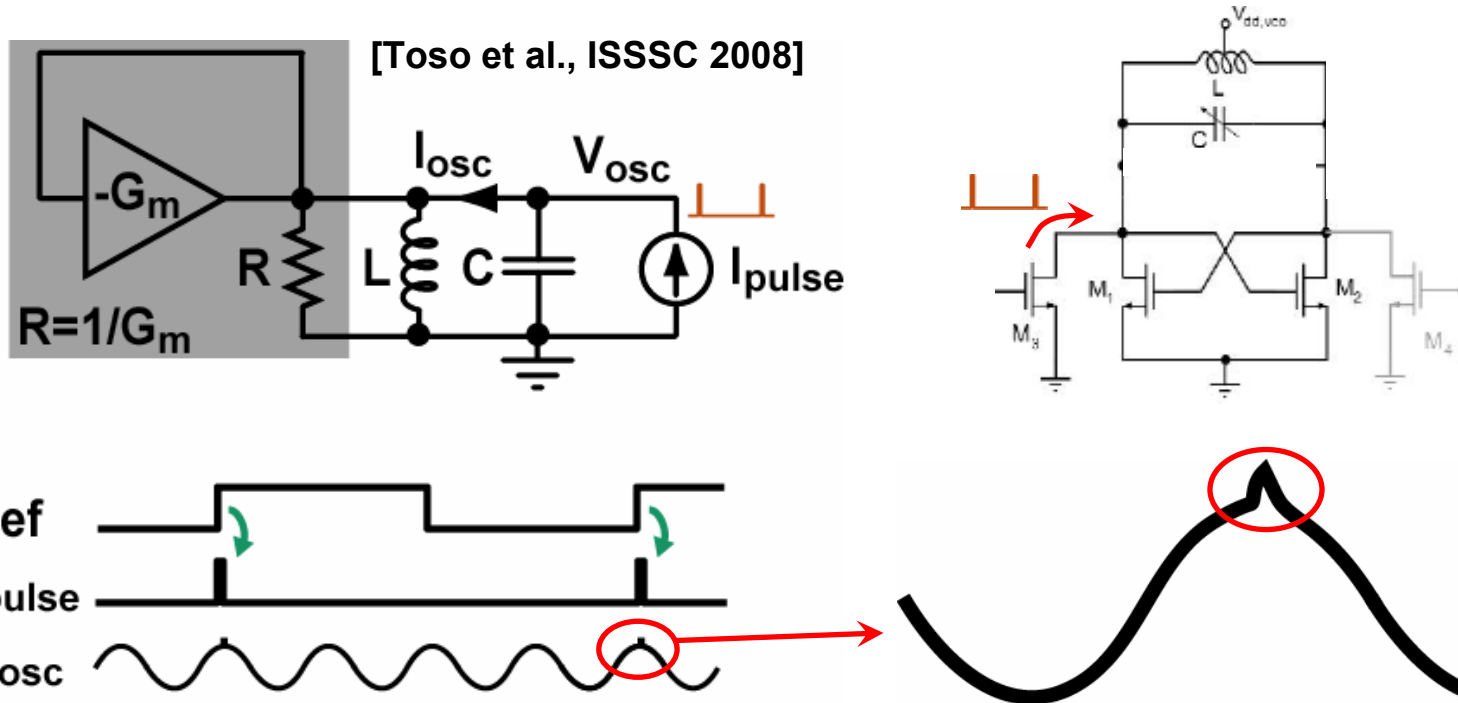
- **Asymmetric injections in differential oscillators**
  - → **large reference spurs**
- **Current pulses have constant level even at ideal tuning**
  - → **Oscillator amplitude is disturbed periodically**
  - → **increased reference spurs**

Proposed Pulse Injection-Locked Oscillator (PILO)
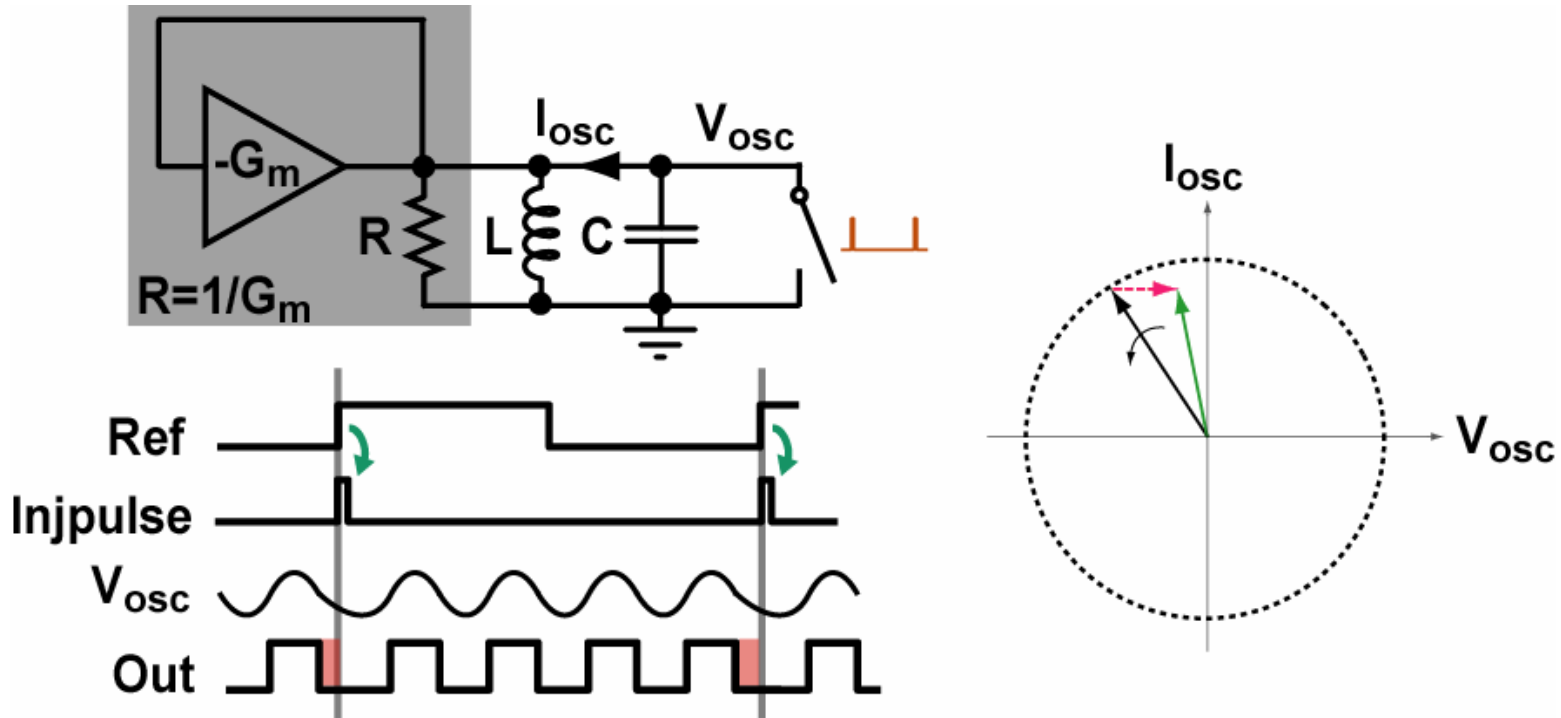
- **Injection lock by shorting the tank instead of using constant current pulses**

- **Injected pulse shifts phase towards zero crossing**

- **Minimal disturbance to oscillator amplitude when injected with narrow pulses and properly tuned**
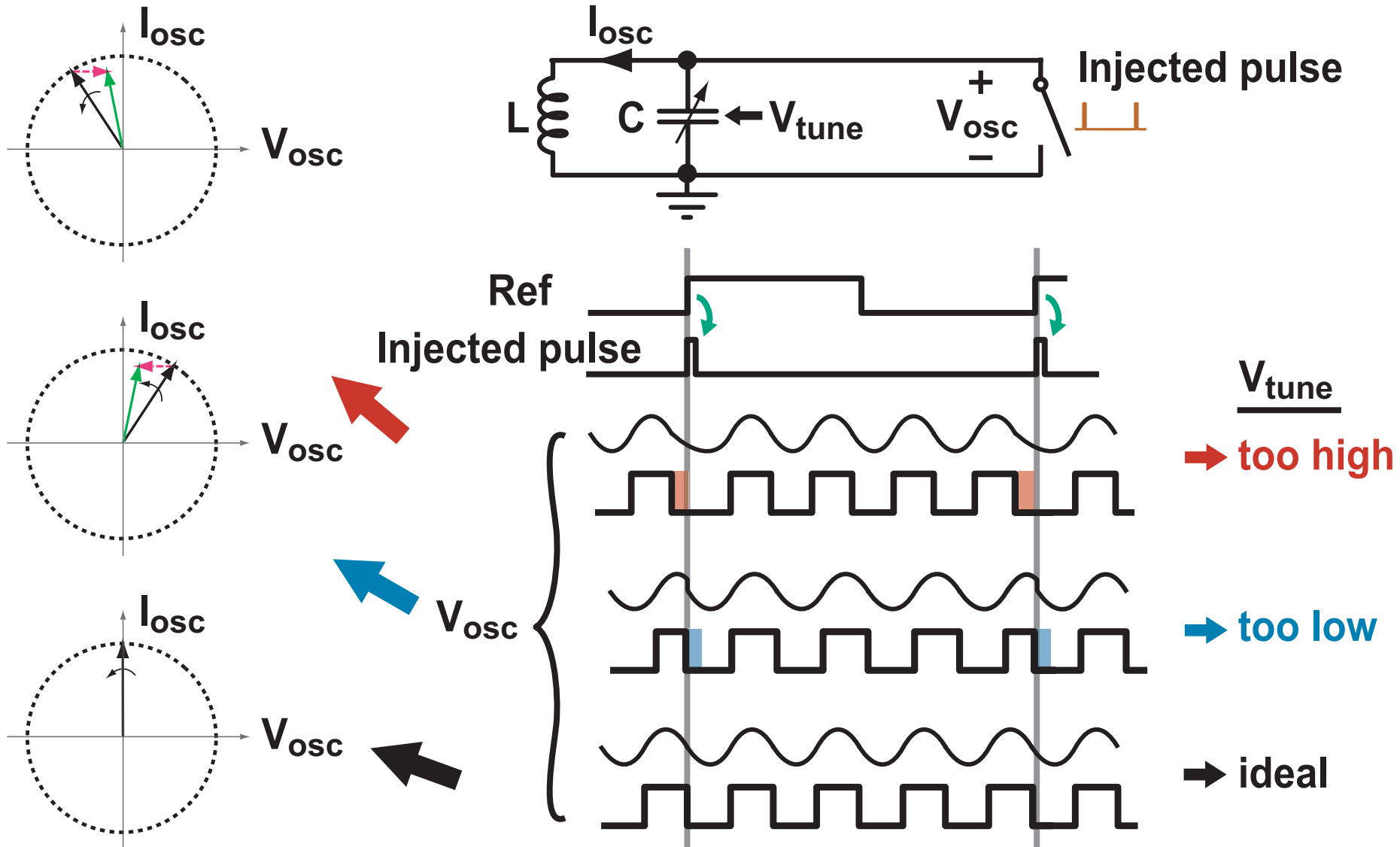
How do we achieve continuous tuning?

Proposed Tuning Approach

- **Leverage a tuning technique originally developed for Multiplying Delay-Locked Loops (MDLLs)**
  - **See Helal et al., JSSC, April 2008**

Output Period Detection
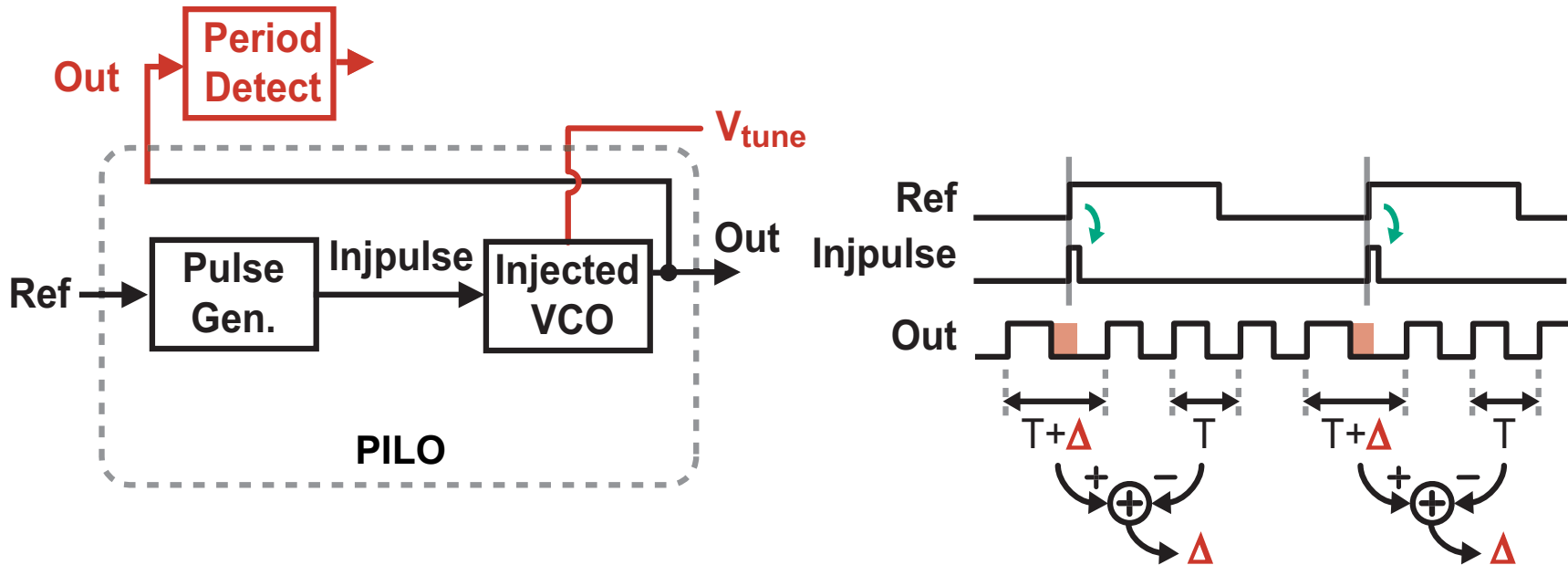
- **Compare cycle periods of PILO output**
- **Infer error (Δ) *from difference* between cycle periods of the PILO output**
- **Use this information to control V_{tune}**

Comparison of same signal eliminates path mismatch
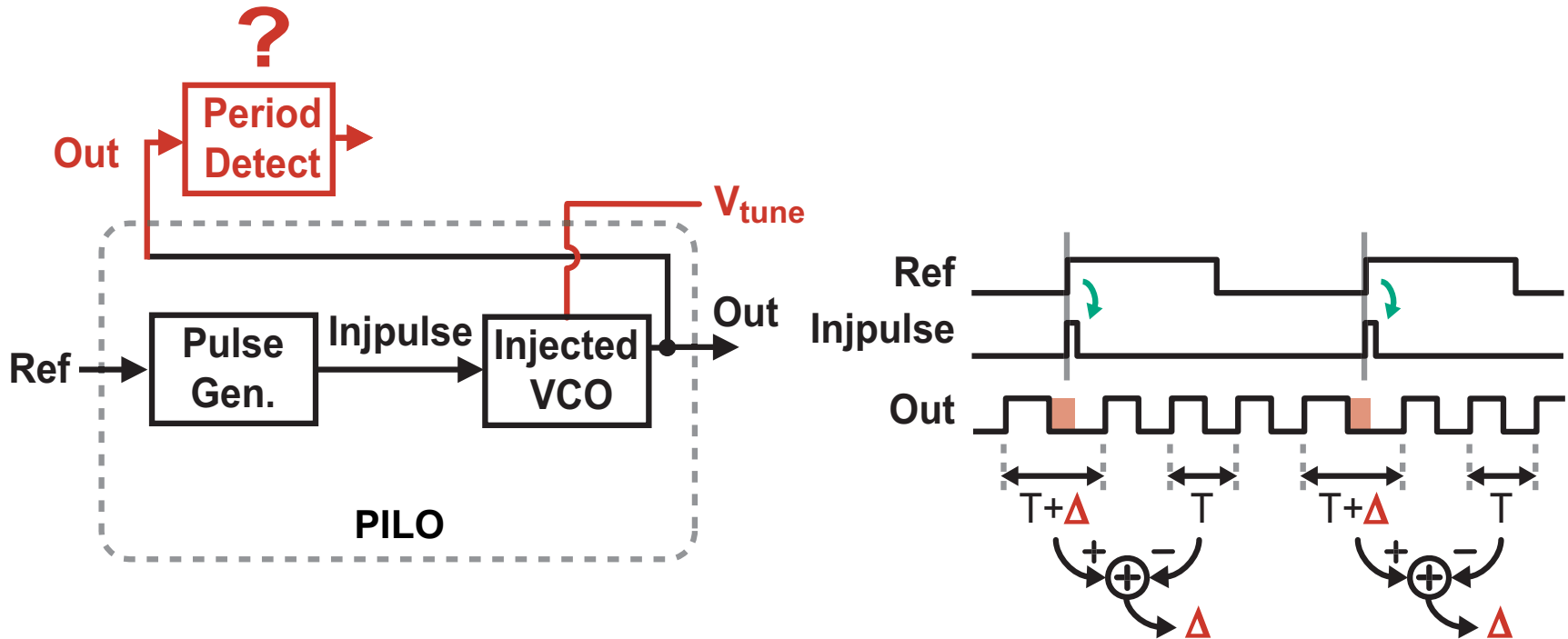
Detection of the Output Period

- **Need an accurate period detector**
  - Error removal is limited by the effective resolution of the detector
- **A digital detector has many advantages**
  - Time-to-digital converter (TDC)

Scrambling TDC

Gated Ring Oscillator

Enable

Reset

Counters

Count

Logic

Register

Enable

Out

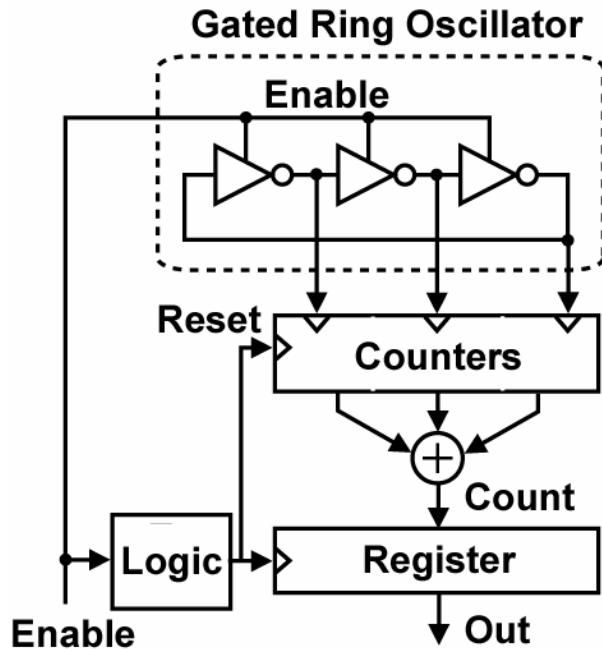[Helal, Straayer, *et al.*, JSSC 2008]

Enable

Oscillator
Phases

Count

Out

11   10
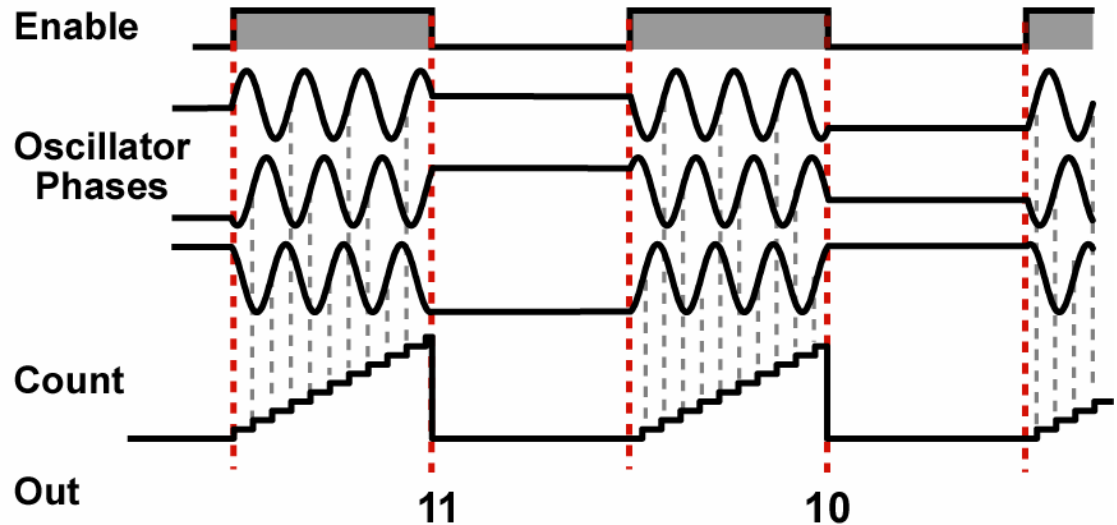
- **Gated Ring Oscillator (GRO) is ON during the measured period**
- **Quantization noise is scrambled (and first order noise shaped)**
  - **Effective resolution improved by averaging**
- **We are using a new version of the GRO**
  - **Details in Straayer, *et al.*, VLSI 2008**

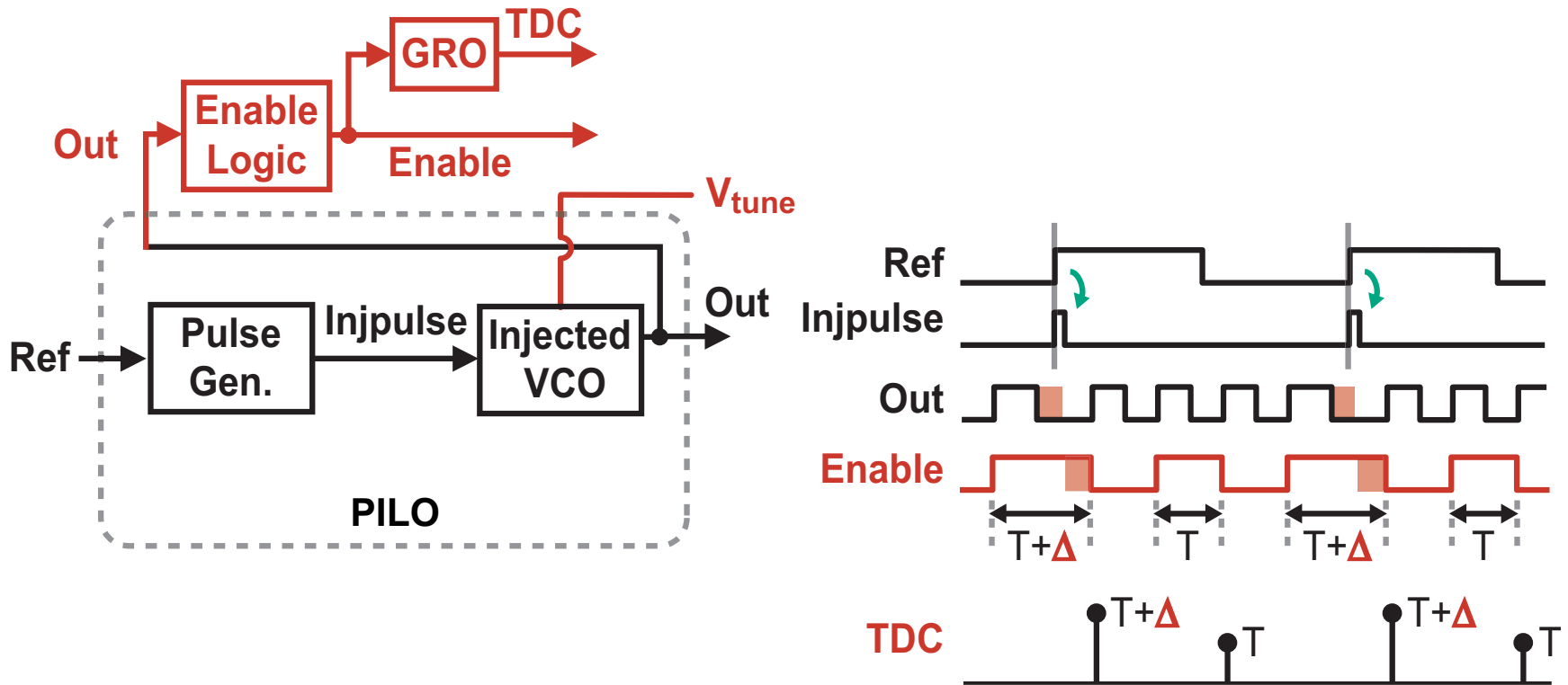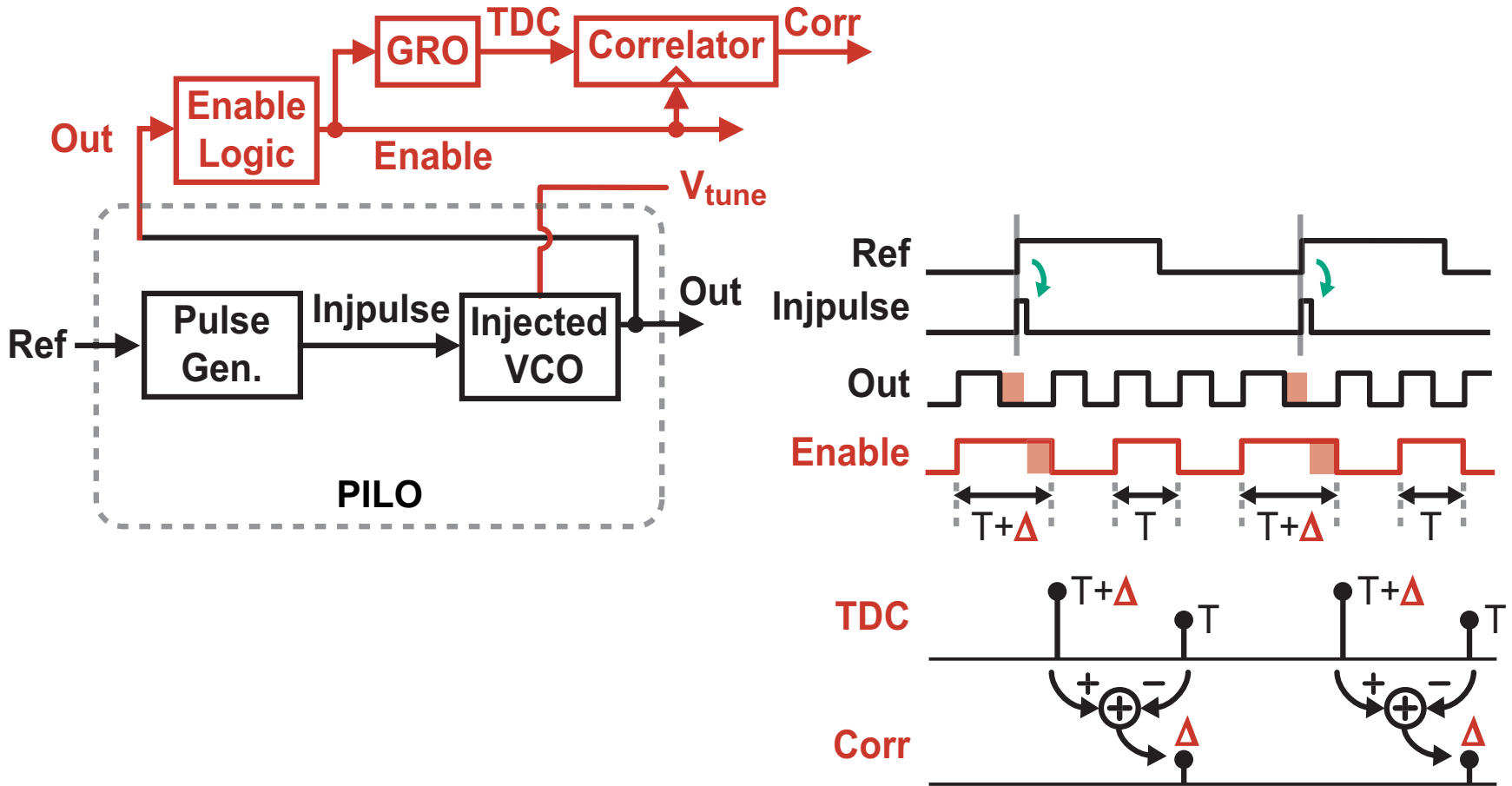# *Using the GRO in the proposed PILO Architecture*

- **Oversampling improves the effective resolution significantly**
  - T_{gro} = 20 ps, Fs = 100 MHz, BW = 1 kHz
    - → **Effective resolution ≈ 90 fs**
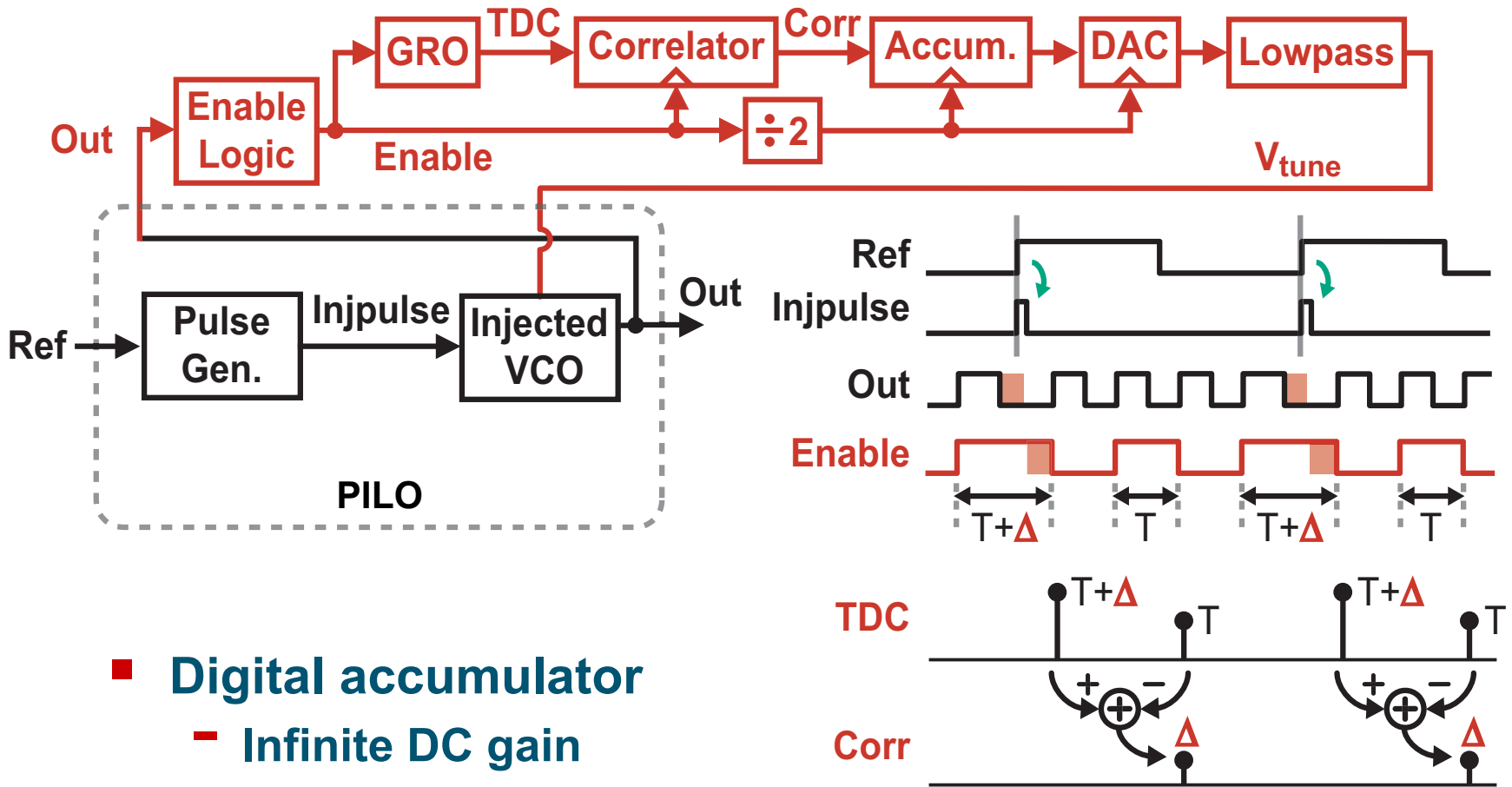
GRO detects the output period accurately

Digital Correlator Extracts the Error

- **Digital version of correlated double-sampling technique**

Close the Loop

- **Digital accumulator**
  - **Infinite DC gain**
  - **No DC offsets**
  - **Allows low bandwidth without leakage or large area**
- V_{tune} **adjustment only needs to track thermal variations**

PILO Prototype
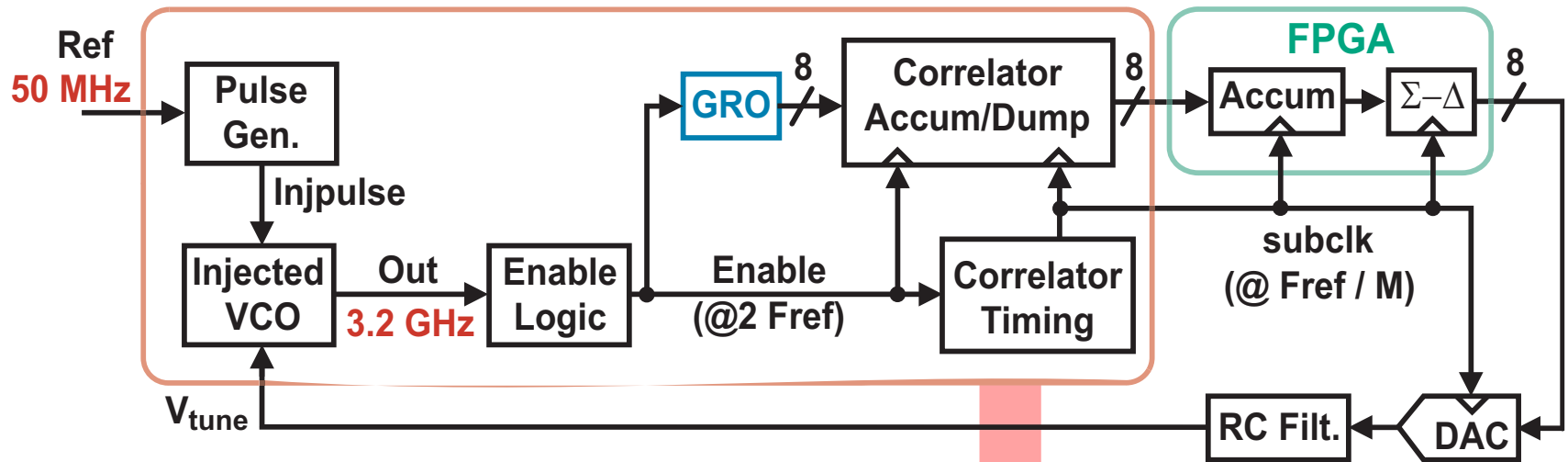
- **Custom 0.13μm CMOS IC**
  - **Active area: 0.4 mm²**
  - **Active Power: 28.6 mW**
- **FPGA**
  - **Accumulator and digital ΣΔ-modulator**
- **Discrete 16-bit DAC and RC lowpass filter (500 kHz pole)**
  - **DAC using 8 effective bits (by using the ΣΔ-modulator)**
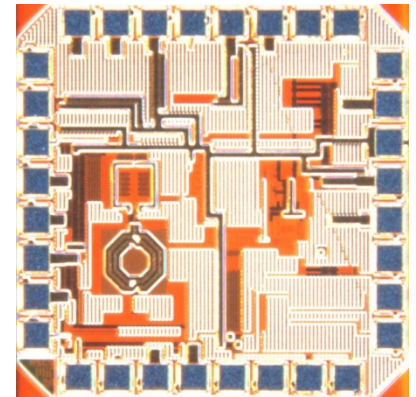
Circuit Details

Proposed PILO Implementation
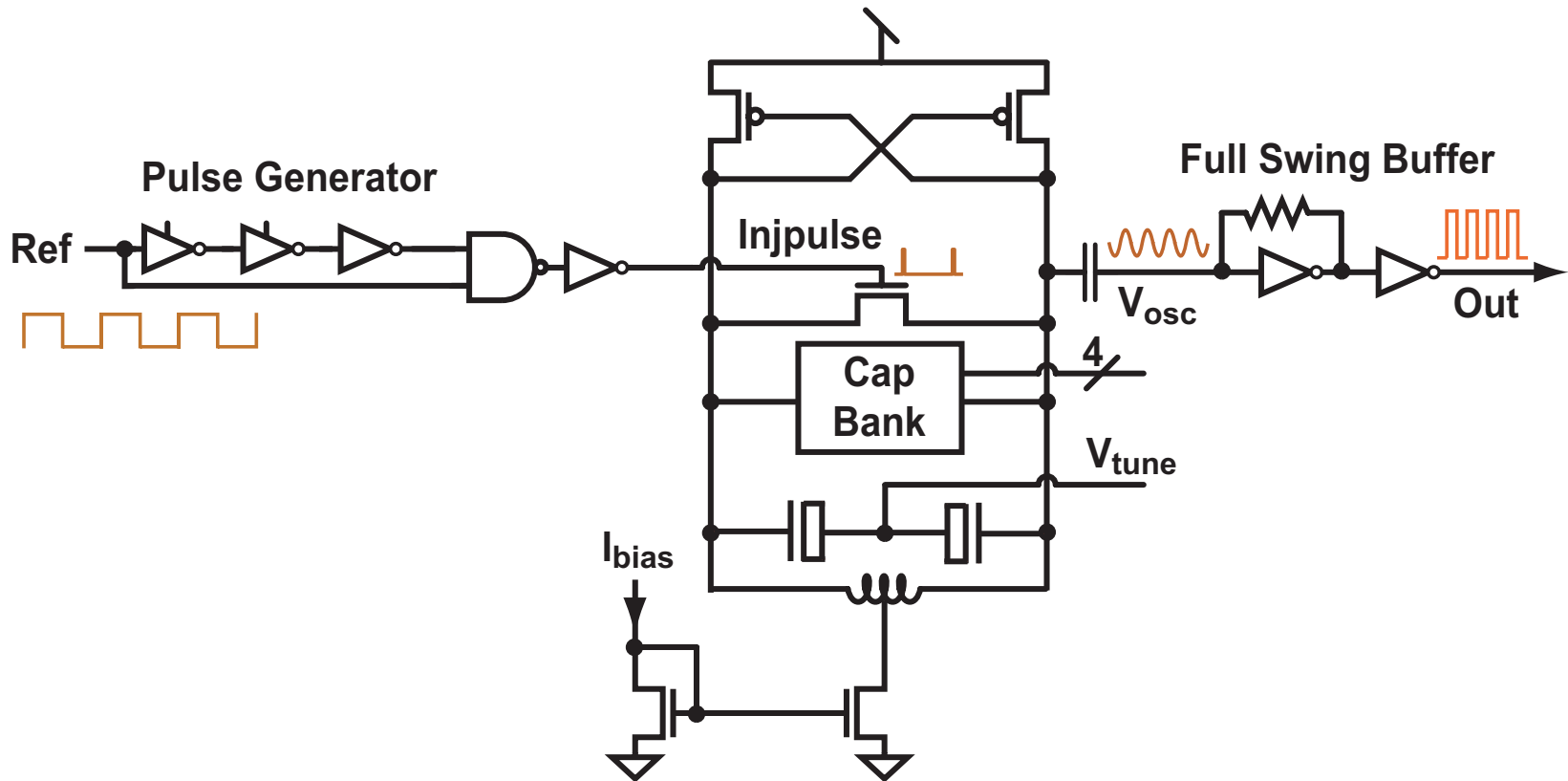
- **Differential Injection by shorting**
  - Minimizes deterministic jitter by preserving injection symmetry
- **Narrow pulses minimize effect on Q of the tank**
  - Minimal residual effect when tuned

Enable Logic

[similar to Voucher, et al, JSSC 2000]

- **Asynchronous Modular divider**
- **Pulse width of mod_x ≈ multiples of VCO periods**
    - → **Enable signal from any mod output (with reasonable width)**
- **Simple implementation and low power consumption**

Enable Logic: Divider Step Control
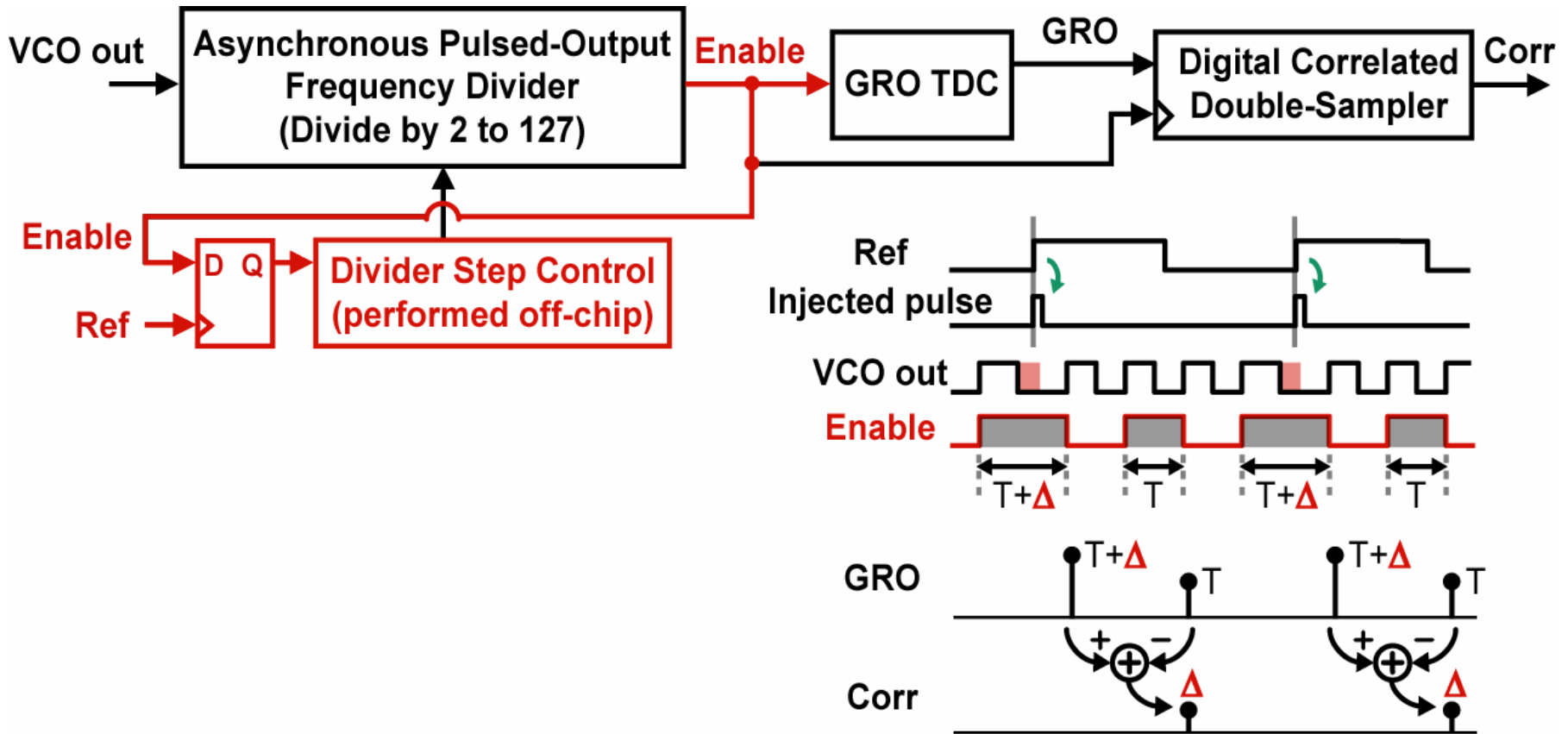
- **GRO TDC must capture periods that includes the injected pulse**
  → **Divider stepped until *Ref* rises during *Enable***

Measured Results

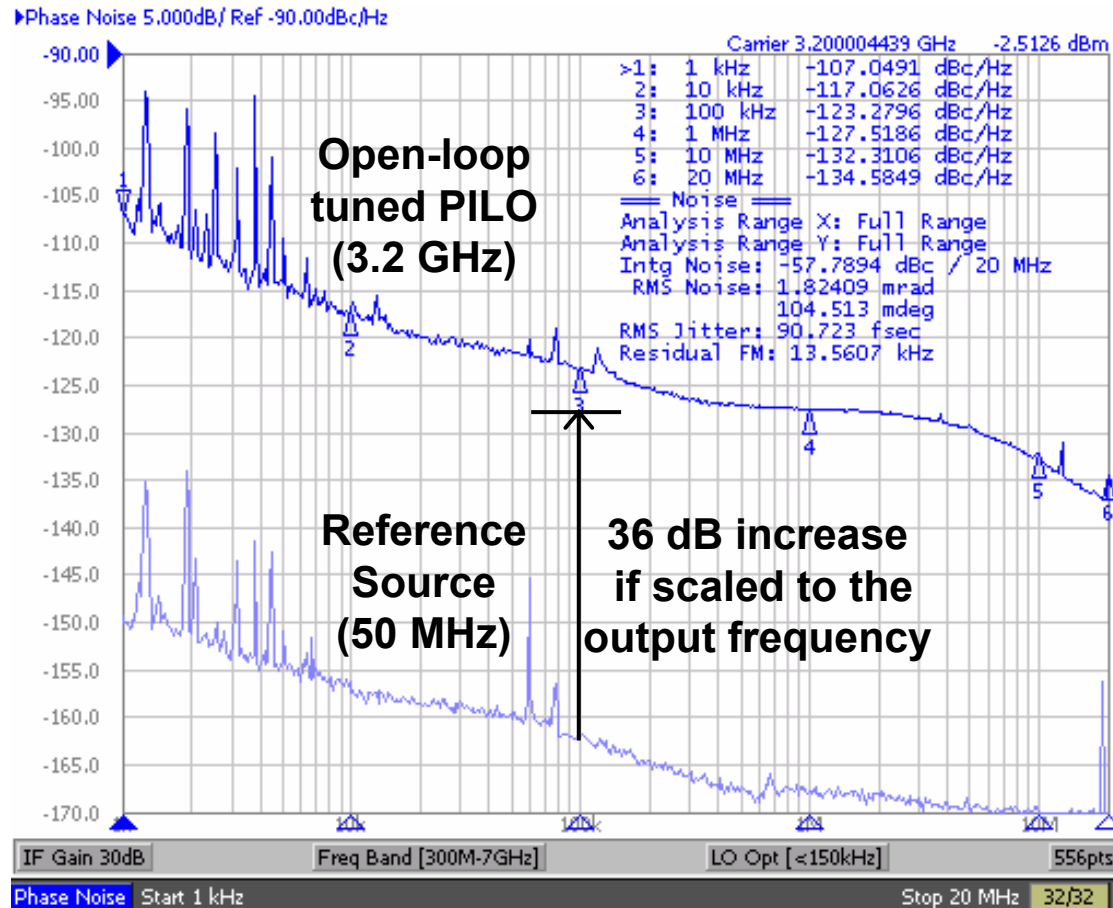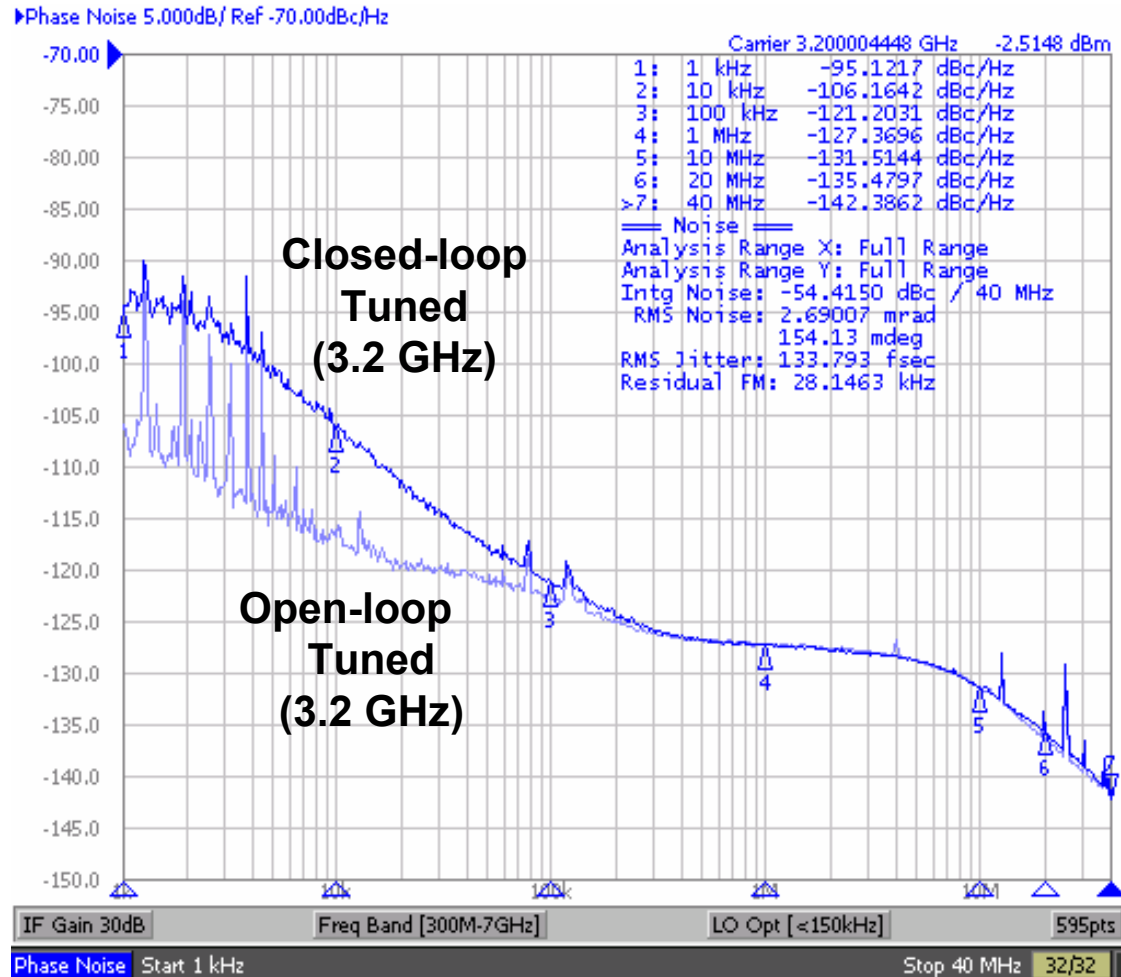# Measured Phase Noise (Open-loop tuned PILO)

- **Random jitter: 91 fs (rms)**
  - **From integrated phase noise (1 kHz to 20 MHz)**

Measured Phase Noise (close-loop tuned PILO)

- **Random jitter: 134 fs (rms)**
  - **From integrated phase noise (1 kHz to 40 MHz)**

Measured Reference Spurs and Est. Deterministic Jitter
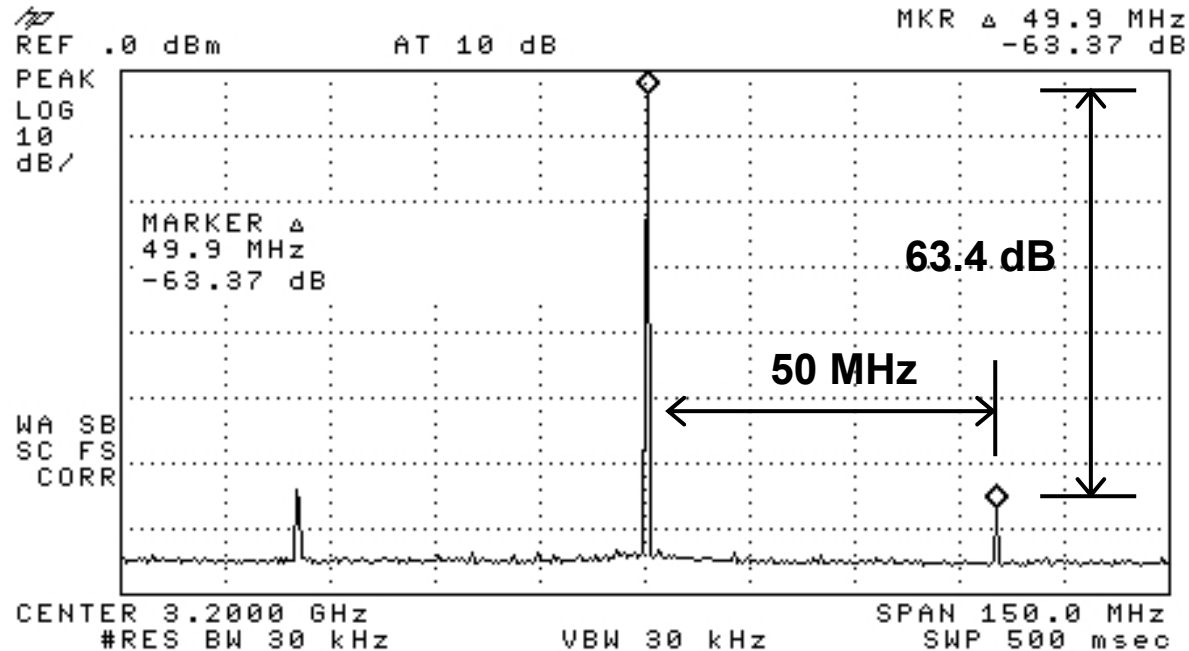

- **Reference Spur: -63.4 dBc**

- **From Fourier analysis:** $\Delta \approx T_{out} \times 10^{Spur(dBc)/20}$

  → **Estimated deterministic jitter ≈ 211 fs (peak-to-peak)**

Performance Summary

Process	**0.13 μm CMOS**
Core Area	**0.4 mm^2**
Core Power	**28.6 mW**
Output Frequency	**3.2 GHz (up to 4 GHz)**
Reference Frequency	**50 MHz**
Reference Spur	**-63.4 dBc**
Deterministic Jitter	**211 fs (peak-to-peak), estimated from measured reference spurs**
Random Jitter	**134 fs (rms), from integrated phase noise (1 kHz to 40 MHz)**

Future Research Area: Optical PILO

Ref_{optical}

Out
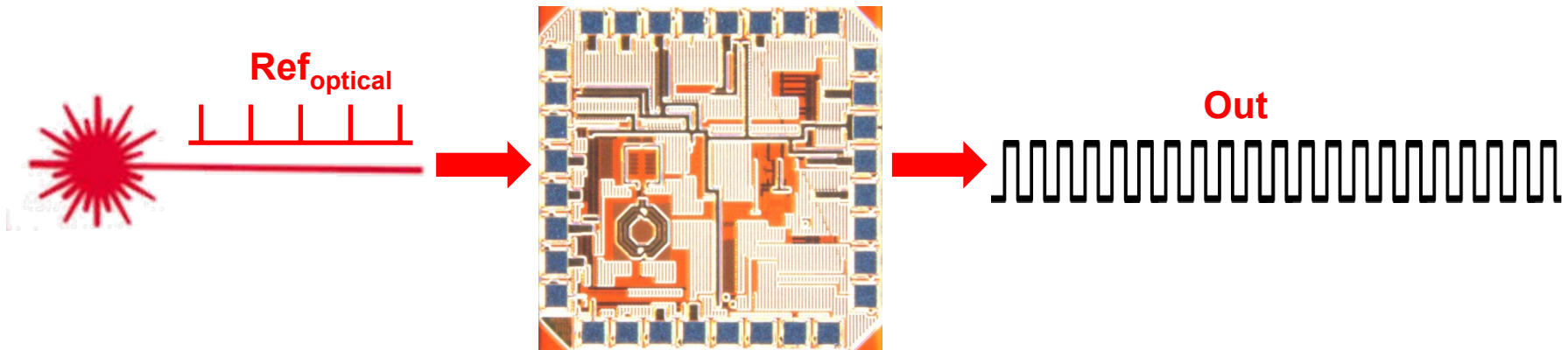
- **RF output from an optical reference input**
- **Leverage Mode-Locked lasers**
  - **Train of very short optical pulses**
  - **Ultra-low jitter in the range of 10's fs to sub-fs**

Conclusions

- **Clock multiplication by injection locking**
  - Lower jitter than typical PLLs
  - Achieved continuous tuning

- **Pulse Injection-Locked Oscillator (PILO)**
  - Injection by shorting minimizes deterministic jitter when tuned

- **PILO-based clock multiplier with highly-digital tuning**
  - 3.2 GHz from 50 MHz reference
  - Random jitter: 134 fs (rms)
  - Deterministic jitter: 211 fs (peak-to-peak)
  - Avoids analog non-idealities
  - Enables low bandwidth without leakage or large area