19.1 A Low-Noise, Wide-BW 3.6GHz Digital ΔΣ Fractional-N Frequency Synthesizer with a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation

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A digital fractional-N frequency synthesizer is presented that leverages a noise-shaping time-to-digital converter (TDC) and a simple quantization noise cancellation technique to achieve low phase noise with a wide PLL bandwidth of 500kHz. In contrast to previous cancellation techniques [1], this structure requires no analog components and is straightforward to implement with standard-cell digital logic. With the cancellation technique enabled, the synthesizer achieves phase noise of -131dBc/Hz at 3MHz offset, and an integrated phase noise from 1kHz to 40MHz of $<300\text{fs}_{rms}$ at 3.67GHz.

Figure 19.1.1 shows a block diagram of the synthesizer. High resolution digital phase detection is performed with an improved version of the gated ring oscillator (GRO) time-to-digital converter presented in [2]. Another interesting component of the architecture is an asynchronous frequency divider, which achieves low noise without re-timing of the divider output. In addition, in contrast to previous digital PLL implementations [3], the digitally-controlled oscillator (DCO) is implemented as a conventional LC voltage-controlled oscillator (VCO) with coarse and fine varactors, which are controlled by two passive 10b, 50MHz digital-to-analog converter (DAC) structures. An additional 4b MIM capacitor bank is included in the VCO to improve its tuning range.

The improved GRO structure (Fig. 19.1.2) greatly reduces the delay per stage by using a multipath ring oscillator [4], which has inputs for each stage that connect to a *combination* of previous delay stages. By optimizing the number, placement and weight of the connections, each stage begins to transition well before the full transition of the immediately preceding stage is completed; the resulting *effective* delay through the stage is reduced to 6ps. Although mismatch can cause each delay stage to vary from the nominal 6ps, a key attribute of the GRO structure is that both this delay mismatch and the overall quantization error will have 1st-order noise shaping [2]. Therefore, the multipath GRO achieves high linearity and resolution *without* the need for calibration.

Figure 19.1.3 displays the proposed divider structure, which leverages a common asynchronous divide-by-16-to-31 composed of cascaded divide-by-2/3 stages. As revealed by the figure, the divider structure realizes a given divide value as the addition of four values, three of which (i.e., N_0, N_1, and N_3) are always constant for a given frequency setting and one of which (i.e., N_2) is controlled by the 3rd-order ΔΣ modulator to achieve fractional values. Due to the re-timing of the reference edge by the flip-flop shown in the figure, only the N_3 edge impacts the GRO phase detector, so that the divide-by-16-to-31 is set to a constant divide-by value before its output directly impacts the phase detector. The divider structure therefore avoids divide-value dependent jitter due to the ΔΣ dithering without the use of re-timing of the divider output.

Figure 19.1.4 displays the quantization noise cancellation circuit, which is completely digital in its implementation. The goal of this circuit is to remove the noise introduced by the dithering action of the divider, which is manifested in the GRO phase error signal, $u[k]$, as a scaled version of the accumulated 3rd-order ΔΣ quantization noise, $x[k]$. Proper scaling of $x[k]$ must be performed before subtracting it from $u[k]$, and the scale factor is determined by a correlation circuit composed of a digital multiplier, accumulator and 1st-order IIR filter. Due to the high resolution of the GRO time-to-digital converter, the correlation feedback loop can be designed to have a reasonably fast settling time without introducing a sig-

nificant amount of additional noise into the synthesizer. As shown in the figure, the correlation feedback loop is enabled once the coarse-tune DAC path has settled; simulations indicate that this loop settles within ten microseconds.

To control both the coarse and fine varactors in the VCO, the loop filter consists of two paths, as shown in Fig. 19.1.5. The coarse-tune varactor, which has a K_v that is 16 times higher than the fine-tune varactor, is fed by a coarse-tune DAC with eight times less bandwidth than the fine-tune DAC to reduce the impact of its thermal noise. Further, the coarse-tune DAC is allowed to vary only when the frequency of the synthesizer is changed, and is fixed in value during steady-state lock conditions such that its quantization noise is not a concern. During a frequency acquisition cycle, the fine-tune DAC is held at its mid-point during coarse-tuning, and is then allowed to vary according to the Type-II settling characteristics of the overall PLL once the coarse-tune value is frozen. Note that a technique similar to that in [5] is used during coarse-tuning in order to allow the coarse-tune DAC to quickly settle to its proper value while simultaneously achieving a desired phase error of zero at the overall loop filter input. The overall settling time of the synthesizer (i.e., the sum of coarse and fine tune times) was measured to be less than 20μs for 10ppm accuracy.

As shown in Fig. 19.1.5, a passive 10b, 50MHz DAC structure is used in the prototype chip to achieve monotonicity with minimal active circuitry and no transistor bias currents. This topology essentially performs a two-step conversion, where the first step is performed by a 5b resistor ladder, and the second step is performed by a 5b zero-V_T NMOS capacitor array. The combination of these steps at 50MHz achieves 10b resolution as well as 1st-order filtering with a cutoff frequency set by a capacitor ratio. Therefore, the filtering bandwidth of each DAC is adjusted by proper selection of the value of C_{load}.

The chip is implemented in a 0.13μm CMOS process and has an active area of 0.95mm² (a micrograph is shown in Fig. 19.1.7). The prototype consumes 26mA from a 1.5V supply, excluding the VCO output buffer that consumes 7mA from a 1.1V supply. Figure 19.1.6 shows the measured phase noise at 3.67GHz where the results are shown with and without cancellation of the quantization noise. As the figure reveals, greater than 15dB noise cancellation is achieved such that out-of-band noise is dominated by the VCO. With noise cancellation enabled, the in-band noise is -108dBc/Hz at a 400kHz offset, and out-of-band noise is -132dBc/Hz and -150dBc/Hz at 3MHz and 20MHz offsets, respectively. The reference spur was measured to be -65dBc. Fractional spurs were measured at carrier frequencies spanning 3.620GHz to 3.670GHz in increments of 1 MHz. Worst case spurs were measured to be -53dBc at carrier frequencies of 3.649 and 3.651GHz, -64dBc at carrier frequencies of 3.648 and 3.652GHz, and were less than -65dBc at all the other carrier frequencies.

References:
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[4] S.-J. Lee, B. Kim and K. Lee, "A Novel High-speed Ring Oscillator for Multiphase Clock Generation Using Negative Skewed Delay Scheme," *IEEE J. Solid-State Circuits*, pp. 289-291, Feb. 1997.
[5] M. Ferriss and M.P. Flynn, "A 14mW Fractional-N PLL Modulator with an Enhanced Digital Phase Detector and Frequency Switching Scheme," *ISSCC Dig. Tech. Papers*, pp. 352-353, 2007.
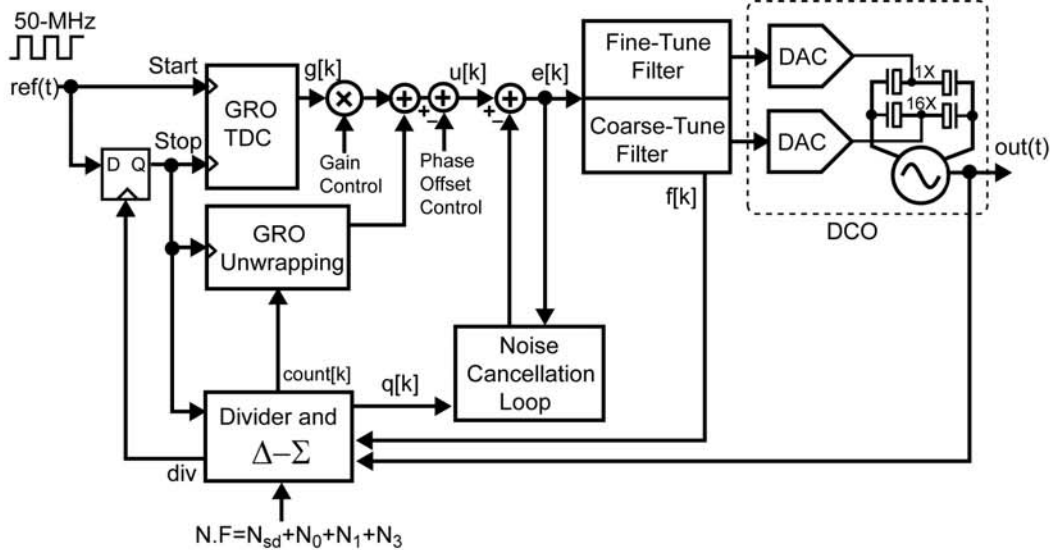
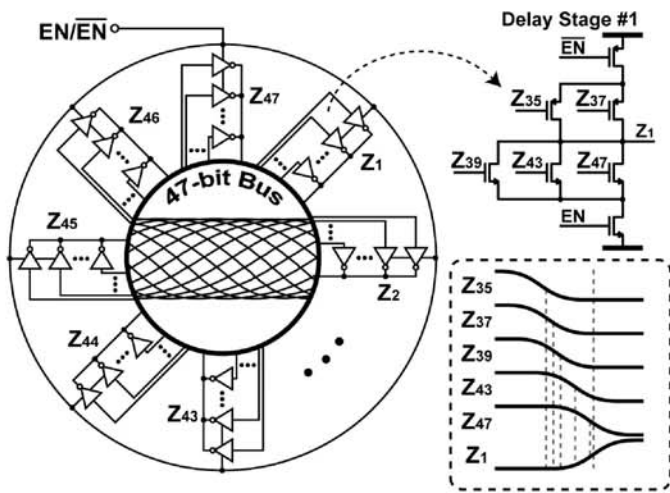Figure 19.1.1: Block diagram of the digital ΔΣ fractional-N frequency synthesizer.

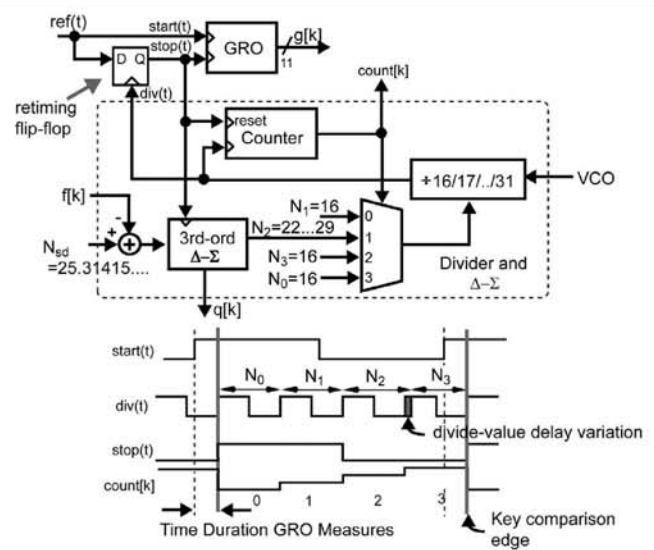Figure 19.1.2: Multipath GRO with 6ps of delay per stage.

Figure 19.1.3: Divider structure avoiding divide-value delay variation.
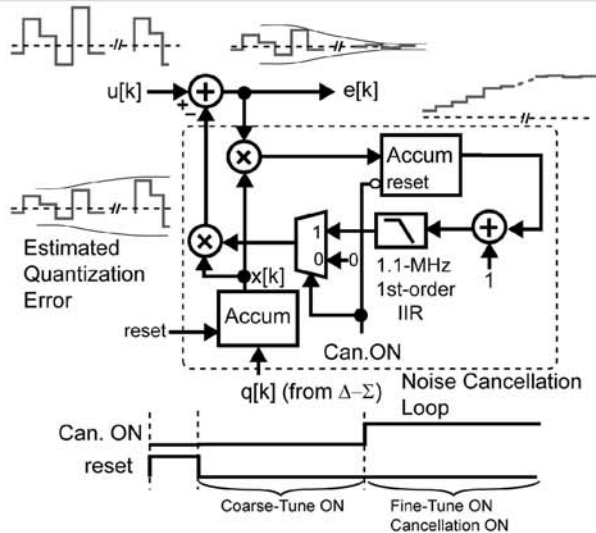

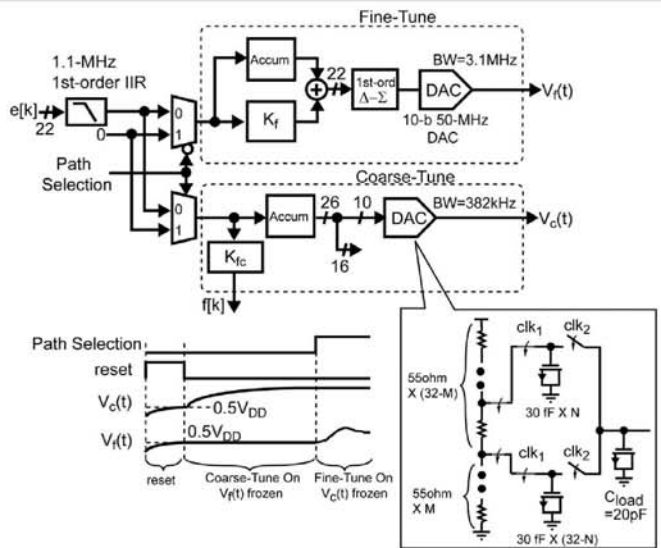Figure 19.1.4: Simplified view of the digital quantization noise cancellation circuit.

Figure 19.1.5: Digital coarse-tune and fine-tune loop filters.
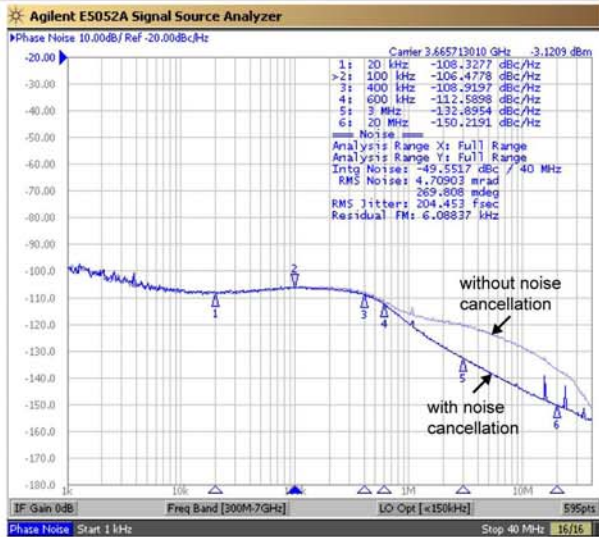
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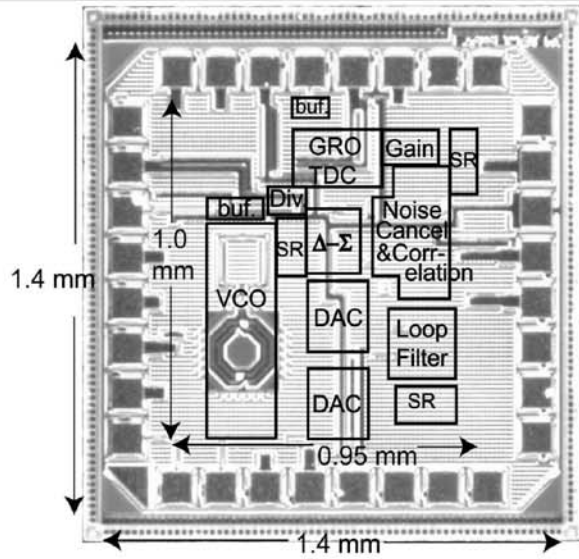
Figure 19.1.6: Measured phase noise with and without cancellation of quantization noise.

Figure 19.1.7: Micrograph.