A 27-mW CMOS Fractional-N Synthesizer Using Digital Compensation for 2.5-Mb/s GFSK Modulation

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***Abstract*— A digital compensation method and key circuits are presented that allow fractional-N synthesizers to be modulated at data rates greatly exceeding their bandwidth. Using this technique, a 1.8-GHz transmitter capable of digital frequency modulation at 2.5 Mb/s can be achieved with only two components: a frequency synthesizer and a digital transmit filter.**

A prototype transmitter was constructed to provide proof of concept of the method; its primary component is a custom fractional-N synthesizer fabricated in a 0.6-μm CMOS process that consumes 27 mW. Key circuits on the custom IC are an on-chip loop filter that requires no tuning or external components, a digital MASH Σ–Δ modulator that achieves low power operation through pipelining, and an asynchronous, 64-modulus divider (prescaler). Measurements from the prototype indicate that it meets performance requirements of the digital enhanced cordless telecommunications (DECT) standard.

***Index Terms*— Compensation, continuous phase modulation, digital radio, frequency modulation, frequency shift keying, frequency synthesizers, phase locked loops, sigma–delta modulation, transmitters.**

I. Introduction

THE use of wireless products has been rapidly increasing the last few years, and there has been worldwide development of new systems to meet the needs of this growing market. As a result, new radio architectures and circuit techniques are being actively sought that achieve high levels of integration and low power operation while still meeting the stringent performance requirements of today's radio systems. Our focus is on the transmitter portion of this effort, with the objective of achieving over 1-Mb/s data rate using frequency modulation.

To achieve the goals of low power and high integration, it seems appropriate to develop a transmitter architecture that consists of the minimal topology that accomplishes the required functionality. All digital, narrowband radio transmitters that are spectrally efficient require two operations to be performed. The baseband modulation data must be filtered to limit the extent of its spectrum, and the resulting signal must be translated to a desired RF band. This paper will focus on the issue of frequency translation, which can be accomplished in at least three different ways for frequency modulation. As illustrated in Fig. 1, the modulation signal can be (a) multiplied by a local oscillator (LO) frequency using a mixer, (b) fed into the input of a voltage controlled oscillator (VCO), or (c) fed into the input of a frequency synthesizer.

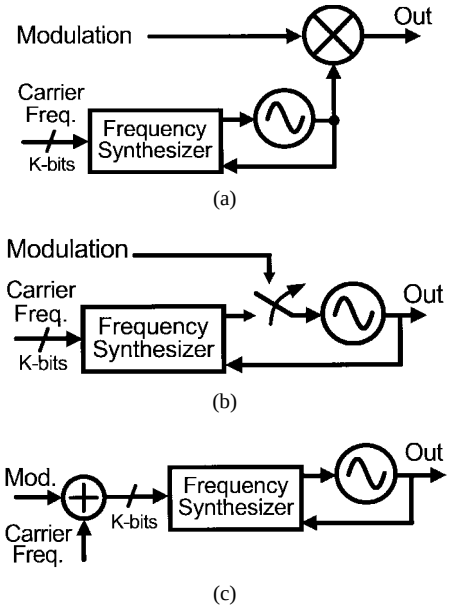

Fig. 1. Methods of frequency modulation upconversion: (a) mixer based, (b) direct modulation of VCO, and (c) indirect modulation of VCO.

Approach (a) can theoretically be accomplished with either a heterodyne or homodyne approach. The heterodyne approach offers excellent radio performance but carries a high cost in implementation due to the current inability to integrate the high-Q, low-noise, low-distortion bandpass filters required at intermediate frequencies (IF) [1]. As a result, the direct conversion approach has recently grown in popularity [2]–[4]. In this case, two mixers and baseband A/D converters are required to form in-phase/quadrature (I/Q) channels and a frequency synthesizer to obtain an accurate carrier frequency.

Approach (b) is referred to as direct modulation of a VCO and has appeared in designs for the digital enhanced cordless telecommunications (DECT) standard [5], [6]. A frequency synthesizer is used to achieve an accurate frequency setting and then disconnected so that modulation can be fed into the

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VCO unperturbed by its dynamics. This technique allows a significant reduction in components; no mixers are required since the VCO performs the frequency translation, and only one D/A converter is required to produce the modulation signal. Power savings are thus achieved, as demonstrated by the fact that the design in [5] appears to consume nearly half the power of the mixer based designs in [2]–[4]. Unfortunately, since the synthesizer is inactive during modulation, the nominal frequency setting of the VCO tends to drift as a result of leakage currents. In addition, undesired perturbations, such as the turn-on transient of the power amp, can dramatically shift the output frequency. As stated in [6], the isolation requirements for this method exclude the possibility of a one-chip solution. Therefore, while the approach offers a significant advantage in terms of power dissipation, the goal of high integration is lost.

Finally, approach (c) can be viewed as *indirect* modulation of the VCO through appropriate control of a frequency synthesizer that sets the VCO frequency and yields the simplest transmitter solution of those presented. The synthesizer has a digital input which allows elimination of the D/A converter that is required when directly modulating the VCO. Since the synthesizer controls the VCO during modulation, the problem of frequency drift during modulation is eliminated. Also, isolation requirements at the VCO input are greatly reduced at frequencies within the PLL bandwidth. The primary obstacle faced with this architecture is that a severe constraint is placed on the maximum achievable data rate due to the reliance on feedback dynamics to perform modulation.

This paper presents a compensation method and key circuits that allow modulation of a frequency synthesizer at rates that are over an order of magnitude faster than its bandwidth. Application of the technique allows a high data rate ($>$1 Mb/s) transmitter with good spectral efficiency to be realized with only two components: a frequency synthesizer and a digital transmit filter. By avoiding additional components such as mixers and D/A converters in the modulation path, a low power transmitter architecture is achieved. Since off-chip filters are not required, high integration is accomplished as well. The technique can be used in transmitter applications where frequency modulation is desired, and a moderate tolerance is allowed on the modulation index. (When using compensation, the accuracy of the modulation index, which is defined as the ratio of the peak-to-peak frequency deviation of the transmitter output to its data rate, is limited by variations in the open-loop gain of the PLL [7].) To provide proof of concept of the technique, we present results from a 1.8-GHz prototype that supports Gaussian frequency shift keying (GFSK) modulation, the same modulation method used in DECT, at data rates in excess of 2.5 Mb/s.

We begin by reviewing a fractional-N synthesizer method presented in [8]–[11] that provides a convenient structure with which to apply the technique. It is shown that high data rates and good noise performance are difficult to achieve with this topology. A method is proposed to overcome these problems, followed by discussion of issues that ensue from its use. A description of key circuits in the prototype is then given, which include an on-chip loop filter, a 64-modulus divider, and a pipelined, digital Σ–Δ modulator. Finally, experimental results are presented and conclusions made.

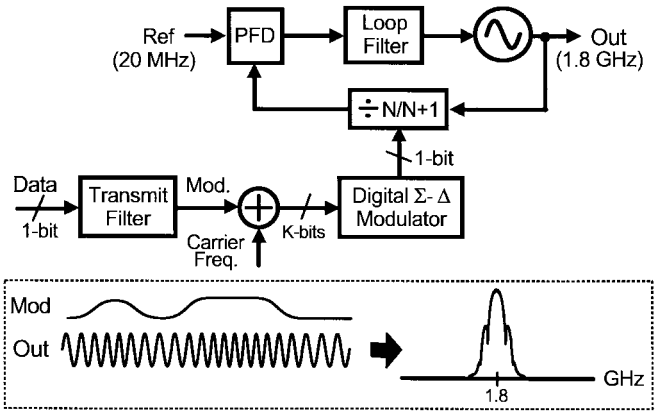


Fig. 2. A spectrally efficient, fractional-N modulator.

II. Background

The fractional-N approach to frequency synthesis enables fast dynamics to be achieved within the phase-locked loop (PLL) by allowing a high reference frequency [8]; a very useful benefit when attempting to modulate the synthesizer. High resolution is achieved with this approach by allowing noninteger divide values to be realized through dithering; it has been shown that low spurious noise can be obtained by using a high-order Σ–Δ modulator to perform this operation [8], [10], [11]. This approach leads to a simple synthesizer structure that is primarily digital in nature, and is referred to as a fractional-N synthesizer with noise shaping.

Using this fractional-N approach, it is straightforward to realize a transmitter that performs phase/frequency modulation in a continuous manner by direct modulation of the synthesizer. Fig. 2 illustrates a simple transmitter capable of Gaussian minimum shift keying (GMSK) modulation [9]. The binary data stream is first convolved with a digital finite impulse response (FIR) filter that has a Gaussian shape. (Physical implementation of this filter can be accomplished with a ROM whose address lines are controlled by consecutive samples of the data and time information generated by a counter.) The digital output of this filter is then summed with a nominal divide value and fed into the input of a digital Σ–Δ converter, the output of which controls the instantaneous divide value of the PLL. The nominal divide value sets the carrier frequency, and variation of the divide value causes the output frequency to be modulated according to the input data. Assuming that the PLL dynamics have sufficiently high bandwidth, the characteristics of the modulation waveform are determined primarily by the digital FIR filter and thus accurately set.

Fig. 3 depicts a linearized model of the synthesizer dynamics in the frequency domain. The digital transmit filter confines the modulation data to low frequencies, the Σ–Δ modulator adds quantization noise that is shaped to high frequencies, and the PLL acts as a low-pass filter that passes the input but attenuates the Σ–Δ quantization noise. In the figure, $G(f)$ is

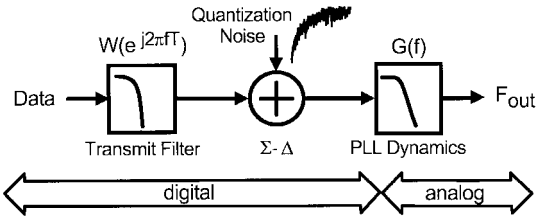


Fig. 3. Linearized model of fractional-N modulator.

calculated as

$$G(f) \equiv \frac{K_v H(f)/(\pi N_{\text{nom}})}{jf + K_v H(f)/(\pi N_{\text{nom}})} \tag{1}$$

where $H(f), K_v$, and N_{nom} are the loop filter transfer function, the VCO gain (in Hz/V), and the nominal divide value, respectively. (See [7] for modeling details.) An analogy between the fractional-N modulator and a Σ–Δ D/A converter can be made by treating the output frequency of the PLL as an analog voltage.

A key issue in the system is that the Σ–Δ modulator adds quantization noise at high frequency offsets from the carrier. In general, the noise requirements for a transmitter are very strict in this range to avoid interfering with users in adjacent channels. In the case of the DECT standard, the phase noise density can be no higher than -131 dBc/Hz at a 5-MHz offset [6]. Noise at low frequency offsets is less critical for a transmitter and need only be below the modulation signal by enough margin to insure an adequate signal-to-noise ratio.

Sufficient reduction of the Σ–Δ quantization noise can be accomplished through proper choice of the Σ–Δ sample rate, which is assumed to be equal to the reference frequency, and the PLL transfer function, $G(f)$. (Note that this problem is analogous to that encountered in the design of Σ–Δ D/A converters, except that the noise spectral density at high frequencies, rather than the overall signal-to-noise ratio, is the key parameter.) One way of achieving a low spectral density for the noise is to use a high sample rate for the Σ–Δ so that the quantization noise is distributed over a wide frequency range and its spectral density reduced. Alternatively, the attenuation offered by $G(f)$ can be increased; this is accomplished by decreasing its cutoff frequency, f_o, or increasing its order, n.

Unfortunately, a low value of f_o carries a penalty of lowering the achievable data rate of the transmitter. This fact can be observed from Fig. 3; the modulation data must pass through the dynamics of the PLL so that its bandwidth is restricted by that of $G(f)$. Given this constraint, the achievement of low noise must be achieved through proper setting of the Σ–Δ sample rate and PLL order.

It is worthwhile to quantify required values of these parameters for a given data rate and noise specification. To do so, we first choose $G(f)$ to be a Butterworth response of order n

$$G(f) = \frac{1}{1 + (jf/f_o)^n}.$$

The above expression is chosen for the sake of simplicity in calculations; other filter responses could certainly be implemented. The spectral density of the noise at the transmitter output due to quantization noise is expressed as

$$S_{\Phi_q}(f) = \left(T\frac{(2\pi)^2}{12}(2\sin(\pi fT))^{2(n-1)}\right)|G(f)|^2 \tag{2}$$

where T is the Σ–Δ sample period, and a multistage (MASH) structure [12] of order n is assumed for the modulator. By choosing the order of the MASH Σ–Δ to be the same as the order of $G(f)$, the rolloff of (2) and the VCO noise are matched at high frequencies (-20 dB/dec). Fig. 4 displays the resulting parameters at different data rates; these values were calculated by setting (2) to -136 dBc/Hz at 5 MHz and the ratio f_oT_d to 0.7, where $1/T_d$ is the data rate. (The noise specification was chosen to achieve less than -131 dBc/Hz at 5 MHz offset after adding in VCO phase noise.)

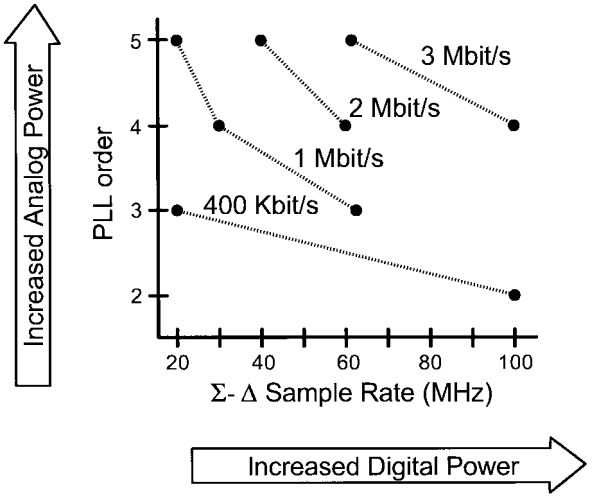


Fig. 4. Achievable data rates versus PLL order and Σ–Δ sample rate when noise from Σ–Δ is -136 dBc/Hz at 5 MHz offset.

The figure reveals that the achievement of high data rates and low noise must come at the cost of power dissipation and complexity when attempting direct modulation of the synthesizer. In particular, the power consumed by the digital circuitry is increased at a high Σ–Δ sample rate by virtue of the increased clock rate of the Σ–Δ modulator and the digital FIR filter, $W(e^{j2\pi fT})$. The power consumed by the analog section is increased for high values of PLL order since additional poles and zeros must be implemented. This issue is aggravated by the need to set these additional time constants with high accuracy in order to avoid stability problems in the PLL. If tuning circuits are used to achieve such accuracy [13], spurious noise problems can also be an issue.

III. Proposed Method

The obstacles of high data rate modulation discussed above are greatly mitigated if the modulation bandwidth is allowed to exceed that of the PLL. In this case, the bandwidth of $G(f)$ can be set sufficiently low that an excessively high PLL order or reference frequency is not necessary to achieve the required noise performance. Fig. 5 illustrates the proposed method that achieves this goal. By cascading a compensation filter, $C(f)$, with the digital FIR filter, the transfer function seen by the modulation data can be made flat by setting $C(f) = 1/G(f)$.

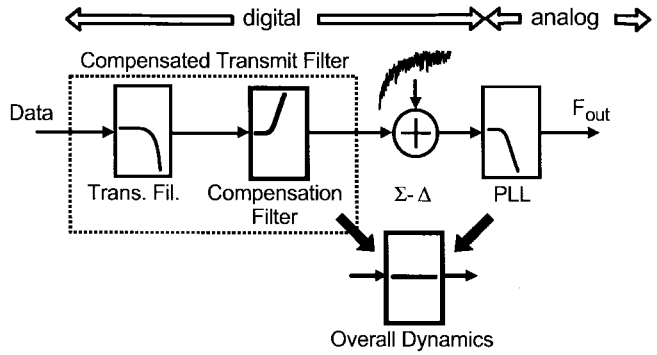


Fig. 5. Proposed compensation method.

This new filter is simple to implement in a digital manner—by combining it with the FIR filter, we need only alter the ROM storage values. In fact, savings in area and power of the ROM can be achieved over the uncompensated method since the number of time samples that need to be stored are dramatically reduced [7].

To illustrate the technique, we consider the case where $W(e^{j2\pi fT})$ is chosen to implement GFSK modulation with $BT_d = 0.5$, as used in the DECT standard, and $G(f)$ is second order. Under these assumptions, the time domain version of $W(e^{j2\pi fT})$ is described as samples of

$$w(t) = \mathrm{rect}(T_d, t) * \frac{T}{4\sqrt{1.66T_d}} e^{-(\pi t/(3.32T_d))^2} \quad (3)$$

where "$*$" is the convolution operator, T is the Σ–Δ sample period, T_d is the period of the data stream, and $\mathrm{rect}(T_d, t)$ equals $1/T_d$ for $-T_d/2 \le t < T_d/2$ and zero elsewhere. Since $C(f)$ is the inverse of $G(f)$, we write

$$C(f) = 1 + \frac{1}{f_o Q} jf + \frac{1}{f_o^2}(jf)^2. \quad (4)$$

In the time domain, the digital compensated FIR filter is then calculated by taking samples of the expression

$$w_c(t) \equiv w(t) * c(t) = w(t) + \frac{1}{2\pi f_o Q} w'(t) + \frac{1}{(2\pi f_o)^2} w''(t). \quad (5)$$

For $w(t)$ described in (3), these derivatives are well defined and can be calculated analytically. A final form is derived by substituting (3) into (5) to yield

$$w_c(t) = \left(1 - \frac{1}{1.66 Q f_o T_d}\left(\frac{t}{\sigma}\right) + \frac{1}{(1.66 f_o T_d)^2}\left(-1 + \left(\frac{t}{\sigma}\right)^2\right)\right) w(t). \quad (6)$$

A. Achievable Data Rates

Equation (6) reveals that the signal swing of $w_c(t)$ increases in proportion to $1/(f_o T_d)^2$ for large values of $1/(f_o T_d)$. Since $1/(f_o T_d)$ is the ratio of the modulation data rate to the bandwidth of the PLL, we see that high data rates lead to large signal swings of the modulation signal when using compensation. Intuitively, this behavior makes sense since the attenuation of $G(f)$ must be overcome by the compensated signal. If the order of $G(f)$ is increased to n, the resulting signal swings will be amplified according to $1/(f_o T_d)^n$.

TABLE I
THEORETICALLY ACHIEVABLE DATA RATES USING COMPENSATION FOR SECOND-ORDER PLL

Σ-Δ sample rate	20 MHz	40 MHz	80 MHz
Max. Data Rate	3.4 Mbit/s	4.8 Mbit/s	4.9 Mbit/s

The achievable data rates using compensation are limited by the ability of the PLL to accommodate this increased signal swing. PLL components that are particularly affected are the Σ–Δ modulator, the divider, and the charge pump. Assuming an appropriate multibit Σ–Δ structure and multimodulus divider topology are used, the bottleneck in dynamic range will be set by the limited duty cycle range of the charge pump.

Table I displays the achievable data rates at different Σ–Δ sample rates using compensation; the noise specification was identical to that used to generate Fig. 4. In light of the signal swing limitation and our goal of simplicity, we have restricted our attention to second-order PLL dynamics. Calculations were based on the assumption that the duty cycle of the charge pump is limited only by its transient response, which was assumed to be 5 ns. Comparison of this information with Fig. 4 reveals that compensation allows high data rates to be achieved with relatively low power and complexity. In the actual prototype, data rates as high as 2.85 Mb/s are achieved with a second-order PLL with $f_o = 84$ kHz, and a Σ–Δ sample rate of 20 MHz.

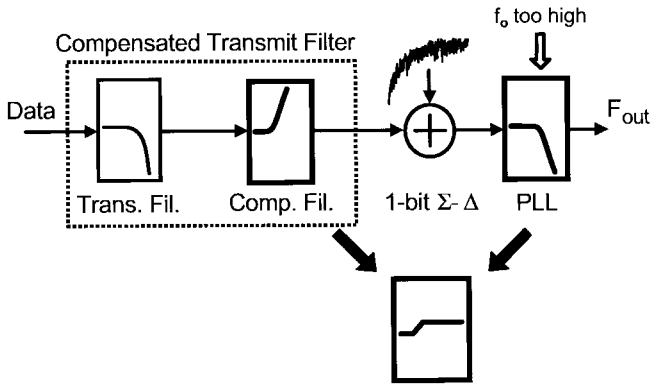


Fig. 6. The effect of mismatch.

B. Matching Issues

In practice, mismatch will occur between the compensation filter and PLL dynamics. While the compensation filter is digital and therefore fixed, the PLL dynamics are analog in nature and sensitive to process and temperature variations. Fig. 6 illustrates that a parasitic pole/zero pair occurs when the bandwidth of the PLL is too high; a similar situation occurs when its bandwidth is too low. As will be seen in the results sections, the parasitic pole/zero pair causes intersymbol interference (ISI) and modulation deviation error. To mitigate this problem in the prototype, an on-chip loop filter with accurate time constants was implemented, and open-loop gain

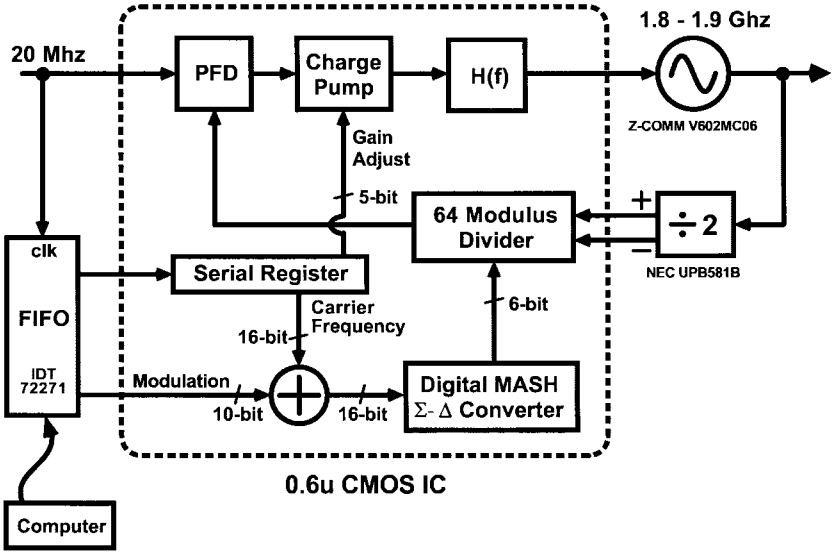


Fig. 7. Prototype system.

control was used to accurately place the overall pole and zero positions of the PLL transfer function.

An additional issue related to be mismatch arises from practical concerns in the PLL implementation. The achievement of a large dynamic range in the charge pump is aided by including an integrator in the loop filter (see Section IV-B2), which yields an overall PLL transfer function as

$$G(f) = \frac{1 + jf/f_z}{1 + jf/f_{cp}} \left(\frac{1}{1 + \frac{1}{f_o Q} jf + \frac{1}{f_o^2}(jf)^2} \right). \quad (7)$$

A parasitic pole/zero pair, f_z and f_{cp}, is now added that occurs well below f_o in frequency. Unfortunately, taking the inverse of (7) leads to a compensation filter that is IIR in nature and cannot be implemented with a ROM. To avoid such difficulties, we can ignore the parasitic pole/zero pair and use $C(f)$ as described in (4). The resulting ISI is negligible since f_z and f_{cp} are close to each other and low in value. However, the digital compensation filter must be modified to be samples of $(f_z/f_{cp})w_c(t)$ to accommodate the increased gain of $G(f)$ at frequencies greater than f_{cp}.

IV. Implementation

To show proof of concept of the proposed compensation method, the system depicted in Fig. 7 was built using a custom CMOS fractional-N synthesizer that contains several key circuits. Included are an on-chip, continuous-time filter that requires no tuning or external components, a digital MASH Σ–Δ modulator with six output bits that achieves low power operation through pipelining, and a 64-modulus divider that supports any divide value between 32 and 63.5 in half cycle increments. An external divide-by-two prescaler is used so that the CMOS divider input operates at half the VCO frequency, which modifies the range of divide values to include all integers between 64 and 127.

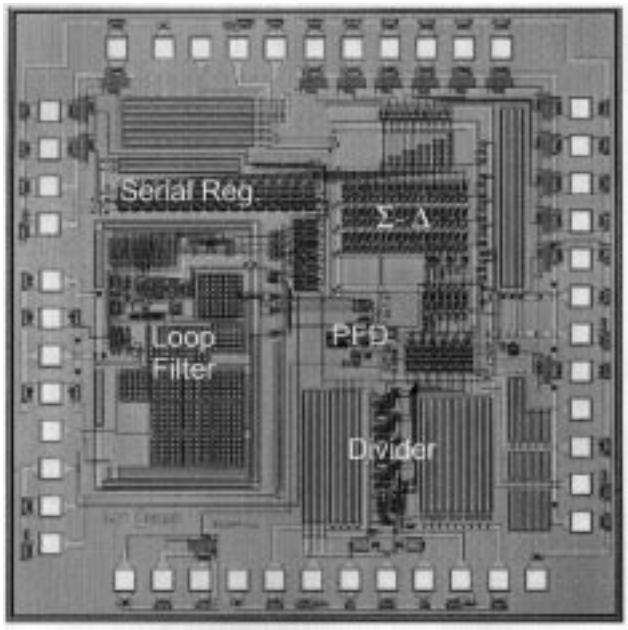


Fig. 8. Die photo.

TABLE II
Power Dissipation of IC Circuits

Component	Divider	Filter	Σ-Δ	Other
Power	22 mW	2.5 mW	0.33 mW	2.4 mW
Supply Voltage	3 V	3.3 V	1.25 V	3.3 V

Fig. 8 displays a die photograph of the custom IC, which was fabricated in a 0.6-μm, double-poly, double-metal, CMOS process with threshold voltages of $V_{tn} = 0.75$ V and $V_{tp} = -0.88$ V. The entire die is 3 mm by 3 mm, and its power dissipation is 27 mW. Table II lists the power consumed by individual circuits. The power supply values given in Table II were chosen to be as low as possible to minimize power dissipation; at the cost of higher power dissipation, all circuits could be powered by a single 3.3-V supply.

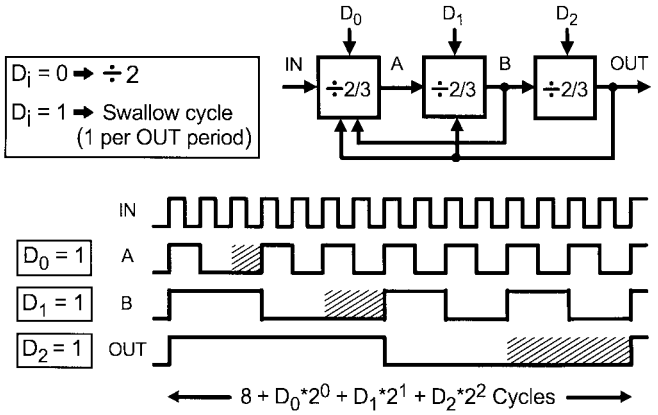


Fig. 9. An asynchronous, eight-modulus divider topology.

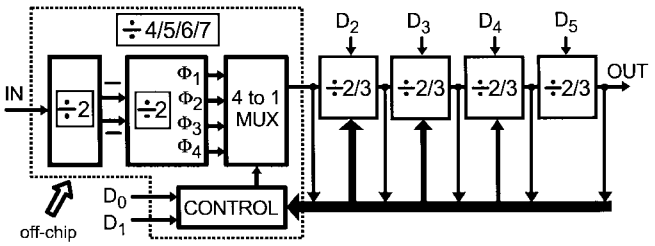


Fig. 10. An asynchronous, 64-modulus divider implementation.

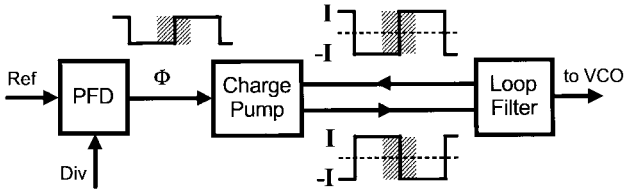


Fig. 11. PFD, charge pump, and loop filter.

The 64-modulus divider and six-output-bit Σ–Δ modulator provide a dynamic range for the compensated modulation data that is wide enough to support data rates in excess of 2.5 Mb/s. The on-chip loop filter allows an accurate PLL transfer function to be achieved by tuning just one PLL parameter—the open-loop gain. A brief overview of each of these components is now presented.

A. Divider

To achieve a low-power design, it is desirable to use an asynchronous divider structure to minimize the amount of circuitry operating at high frequencies. As such, a multimodulus divider structure was designed that consists of cascaded divide-by-2/3 sections [14]; this architecture is an extension of the common dual-modulus topology [15]. The eight-modulus example in Fig. 9 shows the proposed structure which allows a wide range of divide values to be achieved by allowing a variable number of input cycles to be "swallowed" per output cycle. Each divide-by-2/3 stage normally divides its input by two in frequency, but will swallow an extra cycle per *OUT* period when its control input, D_i, is set to one. As shown for the case where all control bits are set to one, the number of *IN* cycles swallowed per *OUT* period is binary weighted according to the stage position. For instance, setting $D_0 = 1$ causes one cycle of *IN* to be swallowed, while setting $D_2 = 1$ causes four cycles of *IN* to be swallowed. Proper selection of $\{D_2 D_1 D_0\}$ allows any integer divide value between 8 and 15 to be achieved.

The 64-modulus divider that was developed for the prototype system uses a similar principle to that discussed above, but has a modified first stage to achieve high-speed operation. Specifically, the implemented architecture consists of a high-speed divide-by-4/5/6/7 state machine followed by a cascaded chain of divide-by-2/3 state machines as illustrated in Fig. 10. The divide-by-4/5/6/7 stage accomplishes cycle swallowing by shifting between four phases of a divide-by-two circuit. Each of the four phases is staggered by one *IN* cycle, which allows single cycle pulse swallowing resolution despite the fact that two cascaded divide-by-two structures are used; details of this approach are discussed at length in [7]. The important point to make about the phase shifting approach, which is also advocated in [15], is that it allows a minimal number of components to operate at high frequencies—the first two stages are simply divide-by-two circuits, not state machines. Also, the fact that control signals are not fed into the first divide-by-two circuit allows it to be placed off-chip in the prototype.

B. Analog Section

The achievement of accurate PLL dynamics is accomplished in the prototype system with the variable gain loop filter topology depicted in Fig. 11. The input to the filter is the instantaneous phase error between the reference frequency and divider output and is manifested as the deviation of the phase frequency detector (PFD) output duty cycle from its nominal value of 50%. As modulation data is applied, the duty cycle is swept across a range of values; the shaded region in the figure corresponds to the deviation that occurs when GFSK modulation at 2.5 Mb/s is applied. A 50% nominal duty cycle is desired to avoid the dead-zone of the PFD and thus reduce distortion of the modulation signal. The prototype used a PFD design from [16] to achieve this characteristic.

To produce a signal that is a filtered version of the phase error, the output of the PFD is converted to complementary current waveforms by a charge pump before being sent into the inputs of an on-chip loop filter. The conversion to current allows the filtering operation to be performed without resistors and also provides a convenient means of performing gain control of the resulting transfer function. An integrator is included in the loop filter which forces the average current from the charge pump to be zero and the nominal duty cycle to be, ideally, 50% when the PLL is locked.

A PFD design with 50% nominal duty cycle is seldom used in PLL circuits due to power consumption and spurious noise issues—the charge pump is always driving current into the loop filter under such conditions, and spurs at multiples of the reference frequency are produced due to the square wave output of the PFD. Fortunately, these problems are greatly mitigated in the prototype transmitter since the charge pump

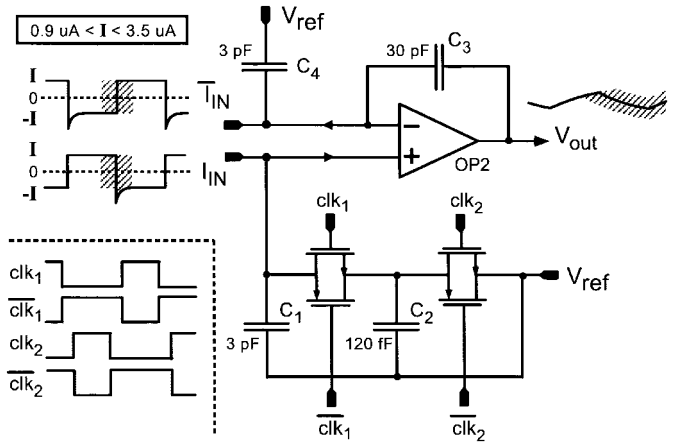


Fig. 12. Loop filter implementation.

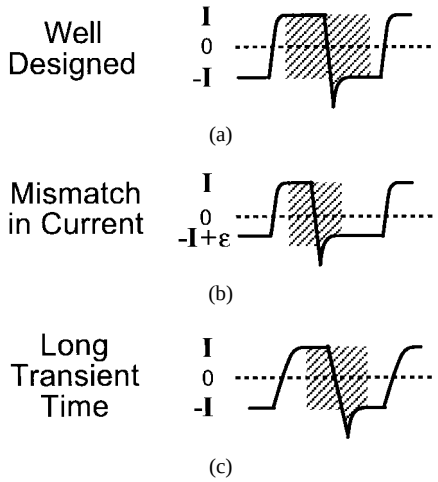


Fig. 13. Effect of transient time and mismatch on duty cycle range.

output current is very small (at its largest setting, it toggles between $+3.5$ and -3.5 μA), and the loop filter bandwidth is very low (84 kHz) in comparison to the reference frequency (20 MHz). The resulting spur at the transmitter output is less than -60 dBc at 20 MHz when measuring the transmitter in an unmodulated state without an RF bandpass filter at its output. When modulated, this spur is convolved with the modulation signal and thus turned into phase noise [7]; it is reasonable to assume that this noise is reduced to a negligible level when the RF bandpass filter is included due to its high frequency offset.

1) Loop Filter: The on-chip loop filter uses an opamp to integrate one of the currents and add it to a first-order filtered version of the other current. This topology, shown in Fig. 12, realizes the transfer function

$$H(f) = K_l \frac{1 + jf/f_z}{jf(1 + jf/f_p)}, \quad f_z = 11.6 \text{ kHz}, \quad f_p = 127 \text{ kHz}. \tag{8}$$

The open loop gain, K_l, is adjusted by varying the charge pump output current, I. The first-order pole f_p is created using a switched capacitor technique, which reduces its sensitivity to thermal and process variations and removes any need for tuning. Note that, although this time constant is formed through a sampling operation, the output of the switched capacitor filter is a continuous-time signal. Finally, the value of the zero, f_z, is determined primarily by the ratio of capacitors C_3 and C_2 under the assumption that the complementary charge pump currents are matched.

A particular advantage of the filter topology is that the rate of sampling C_1 and C_2 can be set high since it is independent of the settling dynamics of the opamp. As such, clk_1 and clk_2 are set to the PFD output frequency, 20 MHz, to avoid aliasing problems.

The opamp is realized with a single-ended, two-stage topology chosen for its simplicity and wide output swing. Its unity gain frequency was designed to be 6 MHz; this value is sufficiently higher than the bandwidth of the GFSK modulation signal at 2.5 Mb/s to avoid significantly affecting it. It is recognized that the single-ended structure has higher sensitivity to substrate noise than a differential counterpart. However, little would be gained in this case by making it fully differential since the output of the opamp is connected directly to the varactor of an *LC*-based VCO, which is inherently single ended. Fortunately, measured eye diagrams and spectral plots presented at the end of this paper conform to calculations that exclude substrate noise, thereby showing that it has negligible impact on the modulation and noise performance of the prototype system. However, as even higher levels of integration are sought in future radio systems, the impact of substrate noise will need to be carefully considered.

The limited dynamics of the opamp prevent it from following the fast transitions of its input current waveforms. To prevent these waveforms from adversely affecting the performance of the opamp, the voltage swing that appears at its input terminals is reduced to a low amplitude (less than 40 mV peak-to-peak) by capacitors C_1 and C_4. In the case of C_1, this capacitor also serves as part of the switched capacitor filter.

2) Charge Pump: Proper design of the charge pump is critical for the achievement of high data rates since it forms the bottleneck in dynamic range that is available to the modulation signal. Fig. 13 illustrates the fundamental issues that need to be considered in its design. To avoid distortion of the modulation signal, the variation in duty cycle should be limited to a range that allows the output of the charge pump to settle close to its final value following all positive and negative transitions. Fig. 13(a) shows the dynamic range available for a well-designed charge pump; the nominal duty cycle is 50% and the transition times are fast. Fig. 13(b) demonstrates the reduction in dynamic range that occurs when the nominal duty cycle is offset from 50%. This offset is caused by a mismatch between positive and negative currents produced by the charge pump. (The type II PLL dynamics force an average current of zero.) Finally, Fig. 13(c) illustrates a case in which the charge pump has slow transition times, the result again being a reduction in dynamic range.

The charge pump topology was designed with the above issues in mind and is illustrated in Fig. 14. The core component of the architecture is a differential pair (M_1 and M_2) that is fed from the top by two current sources, I_1 and I_2, and from the bottom by a tail current, I_{tail}. Ideally, I_1 and I_2 are equal to I and I_{tail} to $2I$, where I is adjusted by a 5-b D/A that

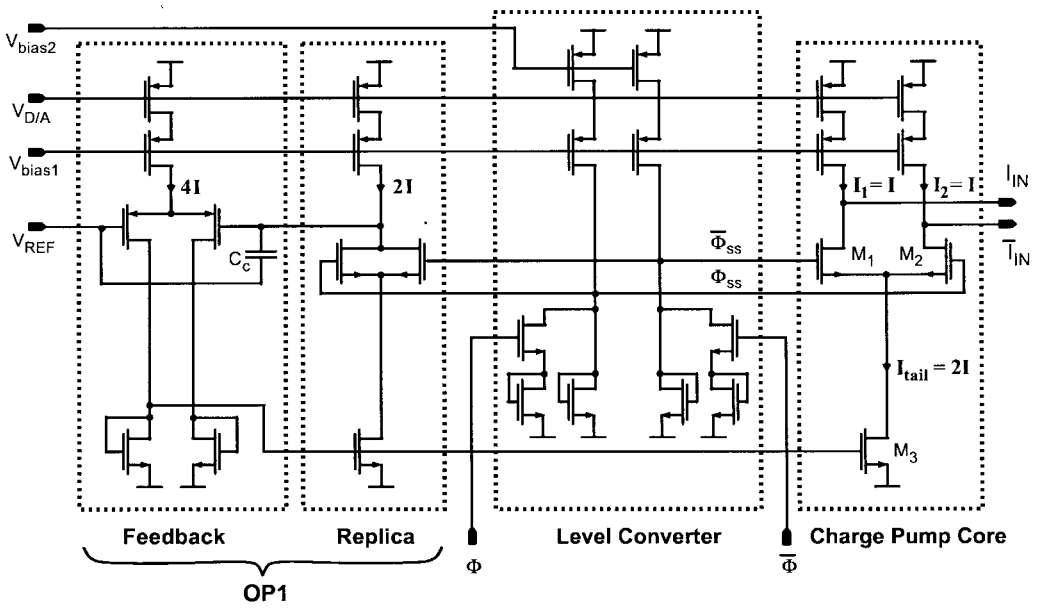


Fig. 14. Charge pump implementation.

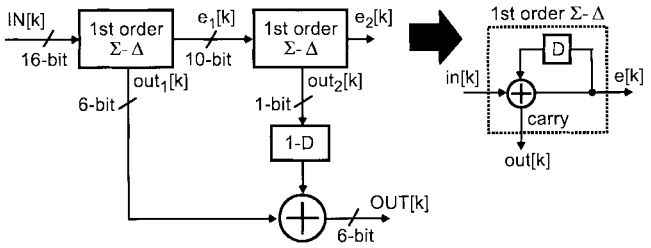


Fig. 15. A second-order, digital MASH structure.

controls the node $V_{D/A}$. Transistors M_1 and M_2 are switched on and off according to Φ, which ideally causes I_{in} and $\overline{I}_{\text{in}}$ to switch between I and $-I$.

To achieve a close match between the positive and negative currents of each charge pump output, the design strives to set $I_1 = I_2$ and $I_{\text{tail}} = I_1 + I_2$. In the first case, I_1 and I_2 are implemented as cascoded PMOS devices whose layout is optimized to achieve high levels of device matching. Unfortunately, device matching cannot be used to achieve a close match between I_{tail} and $I_1 + I_2$ since they are generated by different *types* of devices. To circumvent this obstacle, a feedback stage is used to adjust I_{tail} by comparing currents produced by a replica stage. This technique allows I_{tail} to be matched to $I_1 + I_2$ to the extent that the replica stage is matched to the core circuit.

A low transient time in the charge pump response is obtained by careful design of signal and device characteristics at the source nodes of M_1 and M_2. First, the parasitic capacitance at this node is minimized by using appropriate layout techniques to reduce the source capacitance of M_1 and M_2, the drain capacitance of M_3, and the interconnect capacitance between each of the devices. Second, the voltage deviation is minimized at this node that occurs when Φ switches. The level converter depicted in Fig. 14 accomplishes this task by reducing the voltage variation at nodes Φ_{ss} and $\overline{\Phi}_{ss}$ to less than 350 mV and setting an appropriate dc bias.

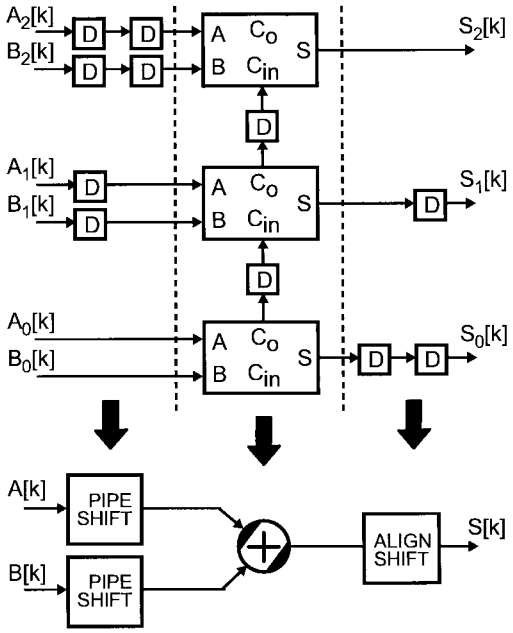


Fig. 16. A pipelined adder topology.

C. Σ–Δ Modulator

Fig. 15 shows the second-order MASH Σ–Δ topology used in the prototype. This structure is well known [12] and has properties that are well suited to our transmitter application. The MASH topology is unconditionally stable over its entire input range and is readily pipelined by using a technique described in this section.

The spectral density at the output of a second-order MASH Σ–Δ modulator is described by the equation

$$S_{\text{OUT}}(f) = S_{\text{IN}}(f) + \left|(e^{-j2\pi fT} - 1)^2\right|^2 S_E(f). \quad (9)$$

In the presence of a sufficiently active input, $S_E(f)$ can be considered a white noise source with spectral density

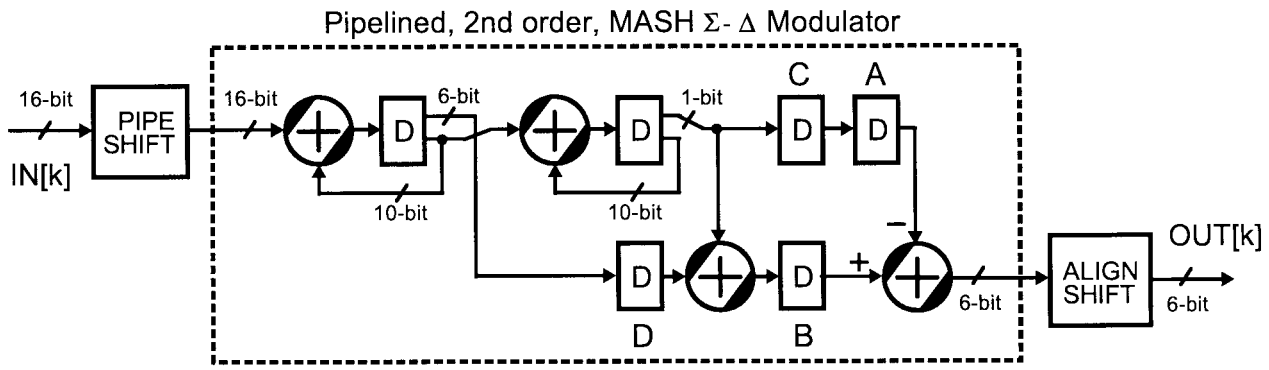


Fig. 17. A pipelined, second-order, digital MASH structure.

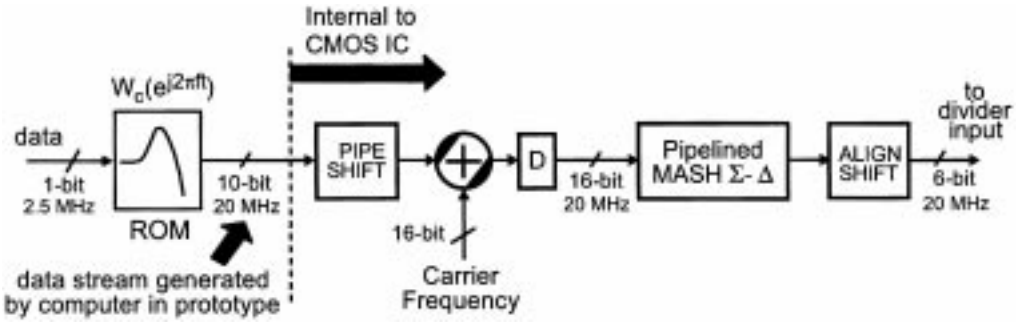


Fig. 18. Pipelined digital data path to divider input.

$S_E(f) = 1/12$. This assumption is reasonable while the modulation signal is applied; we have found that setting the least significant bit (LSB) of the modulator high also helps to achieve this condition by forcing the internal states of the MASH structure to constantly change.

A fact that does not appear to have been appreciated in the literature is that the digital MASH Σ–Δ structure is highly amenable to pipelining. This is a useful technique when seeking a low power implementation since it allows the supply voltage to be reduced by virtue of the fact that the required throughput can be achieved with lower circuit speed.

To pipeline the MASH structure, we apply a well-known technique that has been used for adders and accumulators [17], [18]. Fig. 16 illustrates a 3-b example. Since the critical path in these structures is their carry chain, registers are inserted in this path. To achieve time alignment between the input and the delayed carry information, registers are also used to skew the input bits. As indicated in the figure, we refer to this operation as "pipe shifting" the input. The adder output is realigned in time by performing an "align shift" of its bits as shown. (Note that shading is applied to the adder block in Fig. 16 as a reminder that its bits are skewed in time.) The same pipelining approach can be applied to digital accumulators since there is *no* feedback from higher to lower bits.

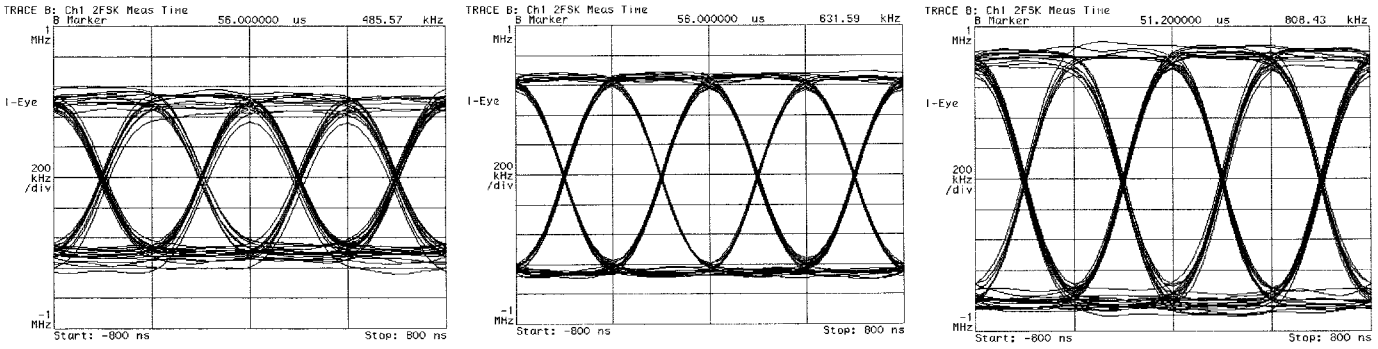
Since its basic building blocks are adders and accumulators, a MASH Σ–Δ modulator of *any order* can be pipelined using this technique. Using the symbols introduced in the previous two figures, Fig. 17 depicts a pipelined, second-order MASH topology. Each first-order Σ–Δ is realized as a pipelined accumulator with feedback removed from the most significant bits in its output. The output of the second stage is fed into the filter $1 - D$, which is implemented with two pipelined adders and a delay element, A. A delay B is inserted between these two adders in order to pipeline their sum path, which requires a matching delay C in the path above for time alignment. Also, a delay D must also be included in the output path of the first Σ–Δ stage to compensate for the time delay incurred through the second stage. Since a signal once placed in the "pipe shifted domain" can be sent through any number of cascaded, pipelined adders and/or integrators, only one pipe shift and align shift are needed in the entire structure.

Fig. 18 illustrates the implementation of the overall digital path using pipelining. To save area, the circuits were pipelined every two bits as opposed to one, and pipe shifting was not applied to the carrier frequency signal since it is constant during modulation. To achieve flexibility, the compensated digital transmit filter was implemented in software, as opposed to a ROM, and the resulting digital data stream fed into the custom CMOS IC.

V. Measured Performance

The primary performance criteria by which a transmitter is judged are its accuracy in modulation and its noise performance. We now describe the characterization of the prototype in relation to these issues.

Fig. 19 shows measured eye diagrams from the prototype using an HP 89441A modulation analyzer. To illustrate the impact of mismatch between the compensation filter and PLL dynamics, measurements were taken under three different values of open-loop gain. These results indicate that the modulation performance of the transmitter is quite good even when the open-loop gain is in error by $\pm 25\%$; the effects of



(a) (b) (c)

Fig. 19. Measured eye diagrams at 2.5 Mb/s for three different open-loop gain settings: (a) −25% gain error, (b) 0% gain error, and (c) 25% gain error.

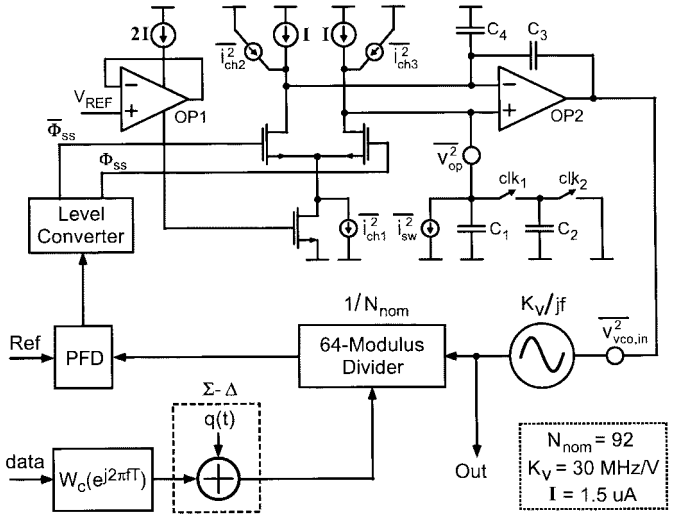


Fig. 20. Expanded view of PLL system.

this gain error are to produce a moderate amount of ISI and an error in the modulation deviation.

An explanation of the observed ISI and deviation error is given in [7]. In brief, the resulting mismatch creates a parasitic pole/zero pair that occurs near the cutoff frequency of the PLL (84 kHz in this case); the resulting transfer function seen by the data can be viewed as the sum of a low-pass and an all-pass filter. ISI is introduced as data excites the impulse response of the low-pass filter, and modulation deviation error occurs since the magnitude of the all-pass is changed according to the amount of mismatch present.

Fig. 20 displays the dominant sources of noise in the prototype; their values are displayed in Table III. Many of these values were obtained through ac simulation of the relevant circuits in HSPICE. Note that all noise sources other than $q(t)$ are assumed to be white, so that the values of their variance suffice for their description. This assumption is only approximate for the VCO noise in the prototype, as will be seen in the measured data.

Based on measurements, the input referred noise of the VCO was calculated in the table from the expression

$$10\ \log\left(\overline{v^2_{\rm vco,in}}|K_v/(jf)|^2\right) = -143\ \text{dBc/Hz at}\ f = 5\ \text{MHz} \tag{10}$$

TABLE III
VALUES OF NOISE SOURCES WITHIN PLL

Noise Source	Origin	Nature	Calculation	Value
$\overline{i^2_{ch1}}$	Ch. Pump, OP1	CT	Hspice	1.2E-24 A^2/Hz
$\overline{i^2_{ch2}}$, $\overline{i^2_{ch3}}$	Ch. Pump	CT	Hspice	1.8E-25 A^2/Hz
$\overline{i^2_{sw}}$	Switched Cap	DT	Equation 11	1.0E-26 A^2/Hz
$\overline{v^2_{op}}$	OP2	CT	Hspice	1.85E-16 V^2/Hz
$\overline{v^2_{vco,in}}$	VCO	CT	Equation 10	1.4E-16 V^2/Hz
$q(t)$	Σ-Δ	DT	—	—

where K_v is 30 MHz/V. The value of the kT/C noise current produced by the switched capacitor operation, $\overline{i^2_{sw}}$, is calculated as

$$\overline{i^2_{sw}} = (1/T)kT_KC_2 \tag{11}$$

where k is Boltzmann's constant, and T_K is temperature in degrees Kelvin.

Assuming that each of the noise sources in Fig. 20 are independent of each other, we can express the overall phase noise spectral density at the transmitter output $S_\Phi(f)$ as

$$S_\Phi(f) = S_{\Phi_v}(f) + S_{\Phi_i}(f) + S_{\Phi_q}(f) \tag{12}$$

where $S_{\Phi_v}(f), S_{\Phi_i}(f)$, and $S_{\Phi_q}(f)$ are the noise contributions from the dominant voltage, current, and quantization noise sources. Based on the values in Table III and the model in Fig. 20, we obtain

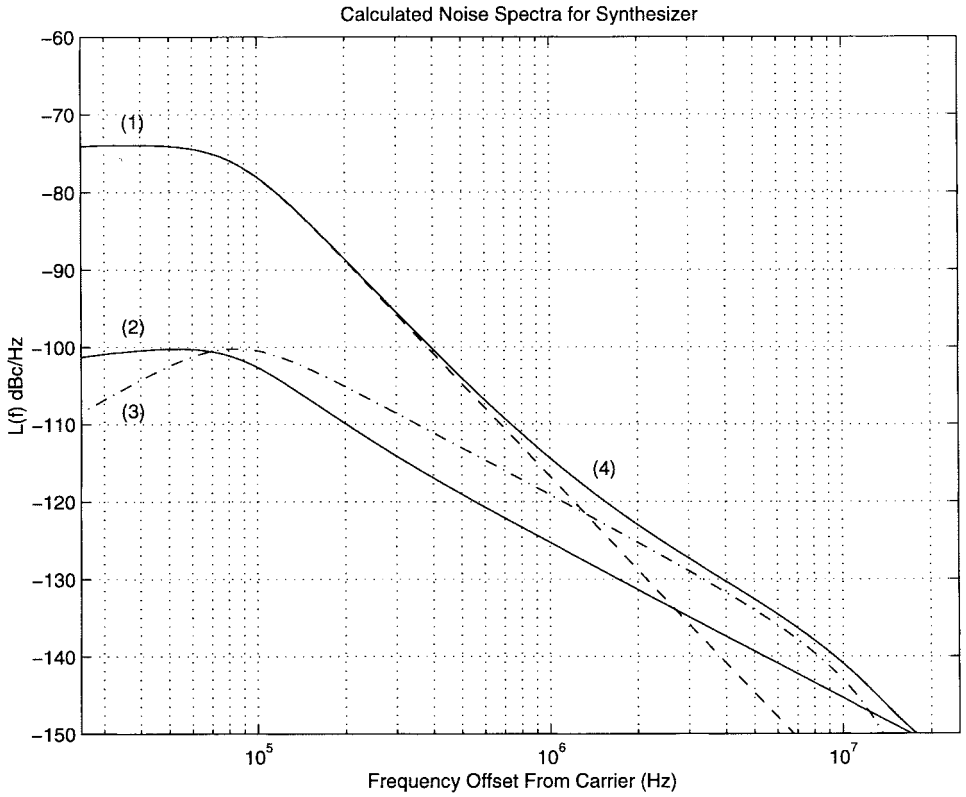
$$\begin{aligned} S_{\Phi_v}(f) &\approx \overline{v^2_{\rm sum}}|K_v/(jf)|^2|1-G(f)|^2 \\ S_{\Phi_i}(f) &\approx \overline{i^2_{\rm sum}}(\pi N_{\rm nom}/I)^2|G(f)|^2 \end{aligned} \tag{13}$$

where

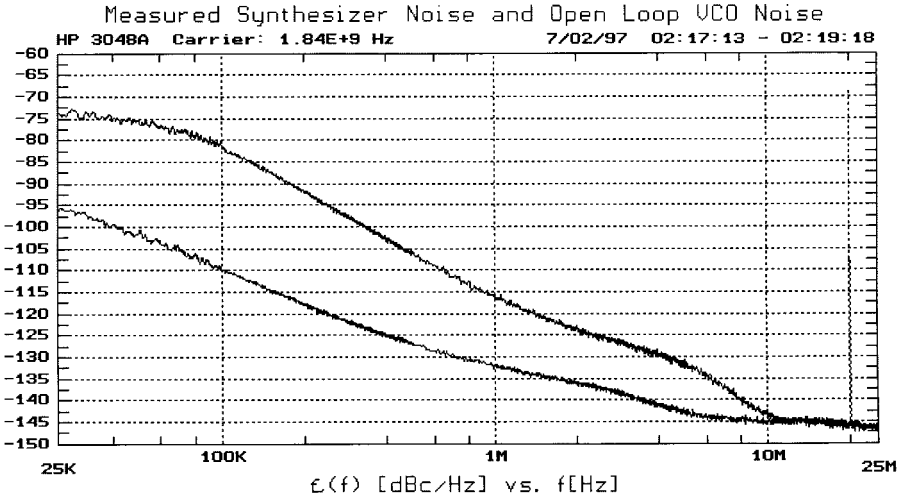
$$\overline{v^2_{\rm sum}} = \overline{v^2_{\rm vco,in}} + \overline{v^2_{\rm op}}, \quad \overline{i^2_{\rm sum}} \approx \overline{i^2_{\rm ch1}}/2.$$

In the case of $S_{\Phi_i}(f)$, the division of $\overline{i^2_{ch1}}$ by two is an approximation based on the fact that the dominant charge pump noise source is switched in and out at each opamp input with a nominal duty cycle of 50%. Note that $S_{\Phi_q}(f)$ is given by (2).

A plot of the spectra in (13) is shown in Fig. 21(a). Computation of these spectra assumed the parameter values



(a)



(b)

Fig. 21. Noise spectra of synthesizer: (a) calculated: (1) charge pump induced, $S_{\Phi_i}(f)$, (2) VCO and opamp induced, $S_{\Phi_v}(f)$, (3) Σ–Δ induced, $S_{\Phi_q}(f)$, (4) overall, $S_{\Phi}(f)$ and (b) measured synthesizer and open-loop VCO noise.

listed in Fig. 20 and Table III, and $G(f)$ described by (7) with

$$f_z = 11.6\ \text{kHz}, \quad f_{cp} = 14.2\ \text{kHz},$$
$$f_o = 84.3\ \text{kHz}, \quad Q = 0.75.$$

As seen in this diagram, the noise from the charge pump $\overline{i_{ch1}^2}$ dominates at low frequencies, and the influence of the Σ–Δ quantization noise dominates at high frequencies.

Fig. 21(b) shows measured noise results from the transmitter prototype taken with an HP 3048A phase noise measurement system. (The spurious content of the Σ–Δ modulator was reduced to negligible levels by feeding a binary data stream into the LSB of the modulation path so that the internal states of the Σ–Δ were randomized; the binary data stream was designed to have relatively flat spectral characteristics and negligible levels of spurious energy at frequencies greater than 10 kHz.) The resulting spectrum compares quite well with the calculated curve in Fig. 21(a), especially at high frequency offsets close to 5 MHz. At lower frequencies in the range of 100 kHz, the measured noise is within about 3 dB

of the predicted value; the higher discrepancy in this region might be attributed to the fact that $\overline{i_{ch1}^2}$ was calculated without considering the offset or transient response of the charge pump and/or the possible inaccuracy of the HSPICE device models at low currents. Note that the spur at 20-MHz offset (the reference frequency), which is due to the 50% nominal duty cycle of the PFD, is less than -60 dBc.

Fig. 21(b) demonstrates that the unmodulated transmitter has an output spectrum $S_\Phi(f)$ of -132 dBc/Hz at 5-MHz offset from the carrier. At this frequency offset, simulations reveal that the output spectrum of the *modulated* transmitter is equal to $S_\Phi(f)$ when its data rate is close to the DECT rate of 1 Mb/s [7]. This being the case, the transmitter satisfies the DECT noise specification of -131 dBc/Hz at 5-MHz offset; eye diagrams for data rates close to 1 Mb/s are found in [7].

VI. Conclusion

A digital compensation method and key circuits were presented that allow modulation of a frequency synthesizer at rates over an order of magnitude faster than its bandwidth. Using this technique, a transmitter prototype was built that achieves 2.5-Mb/s data rate modulation using GFSK modulation at a carrier frequency of 1.8 GHz. Measured results indicate that the architecture can achieve the modulation and noise performance required by the DECT standard with a structure that is highly integrated and has low power dissipation. In particular, the mostly digital design requires no off-chip filters, no mixers, and no D/A converters in the modulation path. Further, the structure contains only the core components required of a narrowband, spectrally efficient transmitter: a frequency synthesizer and a digital transmit filter.

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