A 4^{th} Order Continuous-Time $\Delta\Sigma$ ADC with VCO-Based Integrator and Quantizer

by

Matthew Jeremiah Park

B.S. in Electrical Engineering and Computer Science
Massachusetts Institute of Technology, 2004

M.Eng. in Electrical Engineering and Computer Science
Massachusetts Institute of Technology, 2005

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 2009

Author .....
Department of Electrical Engineering and Computer Science
February, 2009

Certified by .....
Michael H. Perrott
Visiting Associate Professor
Thesis Supervisor

Accepted by .....
Terry P. Orlando
Chairman, Department Committee on Graduate Students

A 4^{th} Order Continuous-Time $\Delta\Sigma$ ADC with VCO-Based Integrator and Quantizer

by

Matthew Jeremiah Park

Submitted to the Department of Electrical Engineering and Computer Science
on February, 2009, in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

Abstract

The use of a VCO-based integrator and quantizer within a continuous-time (CT) $\Delta\Sigma$ analog-to-digital converter (ADC) structure is explored, and a custom prototype in a 0.13 μm CMOS with a measured performance of 81.2/78.1 dB SNR/SNDR over a 20 MHz bandwidth while consuming 87 mW from a 1.5V supply and occupying an active area of 0.45 mm^2 demonstrated. A key innovation is the explicit use of the oscillator's output phase to avoid the signal distortion that had severely limited the performance of earlier VCO-based ADC's, which exclusively made use of the output frequency. Furthermore, the proposed architecture includes a scheme for performing fast dynamic element matching (DEM), enabling first-order shaping of unit-element mismatch in *all* feedback DAC's.

Thesis Supervisor: Michael H. Perrott
Title: Visiting Associate Professor

Acknowledgments

> But he said to me, 'My grace is sufficient for you, for power is made perfect in weakness.' So, I will boast all the more gladly of my weaknesses, so that the power of Christ may dwell in me.
>
> 2 Corinthians 12:9 NRSV

It is extremely difficult for me to describe my feelings about (finally) leaving MIT. This campus has been my home for more than 8 years, longer than I have ever lived in a single location in my lifetime. I've traversed its labyrinthine corridors at obscene hours, spent innumerable days and nights studying for exams and working on problem sets in its cavernous libraries and secluded reading rooms, and toiled in its soulless laboratories for many restless days and harrowing nights. To be honest, I'm amazed that I was able to endure it all with my sanity (relatively) intact.

But my experience at MIT was so much more than blood, sweat and tears. It was an honor to be here, especially because of the phenomenal people that I had the privilege to work with and meet. I owe my utmost thanks and gratitude to my advisor and friend, Mike Perrott, whom I have had the gift of knowing since my sophomore year. Mike has been not only a fantastic and patient teacher (from 6.003 recitations to advanced mixed-signal design), but also a dedicated mentor, an honest assessor of my work, and a committed advocate of my research. Mike's exemplary humility, integrity, and grace established a similar culture and spirit within the High Speed Circuits and Systems Group. Looking back, I marvel at how well the group worked together and supported each other, with its members volunteering their time and effort to help each other make a tapeout deadline. My association with this group is something that I am so proud of and will cherish forever.

I owe special thanks to two of the Perrott Group's earliest students, Ethan Crain and Scott Meninger. Ethan bravely accepted his role as my mentor when I first joined the group as a clueless M.Eng. student. He taught me the basics of chip design, simulation, and layout—all while raising three children, taping out, TA'ing a

class, preparing a talk for ISSCC, and writing a thesis and journal paper. Scott was another great mentor and confidant; his willingness to brainstorm ideas and review my designs helped me improve as a designer as well gain confidence in my abilities. At the same time, his thoroughness in his work was an amazing example that I still strive to replicate.

Matt Straayer and Kerwin Johnson also deserve special recognition for all the help they have given me over the years. Matt's early efforts in VCO-based ADC design laid a lot of the groundwork for my thesis project, and played a crucial role in making it a success. His deep and very intuitive grasp of circuit design helped me test out new ideas and explore different architectures, and his sheer efficiency and productivity when working were both a great inspiration and motivation. Kerwin was the Perrott group's CAD, Cadence and wirebonding wizard *par excellence*, and designed the pads and padframe for the entire IBM tapeout team. He generously and selflessly shared his encyclopedic knowledge about almost every conceivable topic with me on countless occasions, an experience that was not only enriching but also lots of fun!

The results presented in this thesis would also not be possible without the generous help of Charlotte Lau and Min Park. Charlotte assisted me during the tapeout crunch by laying out the high speed output buffers. She was also a calming voice of strength and support during all those days and nights when we were feverishly working to finish the tapeout on time. Min Park (along with Kerwin Johnson) graciously offered his deft fingers to wirebond a few of my chips on several of my trips to the Harvard labs. At the same time, his interminable optimism and fighting spirit toward research boosted my spirits on many occasions when I felt burnt out from work.

Chun-Ming Hsu and Belal Helal were an indispensable aid throughout the tapeout and testing process. Given the similarity of my project to a PLL, Chun-Ming offered a unique perspective on my work, and gave useful feedback on many of my crazy ideas. At the same time, he was great listener and an assuring presence whenever I talked to him about my thoughts and concerns about future careers and pursuits. Belal (along with Min Park) designed the serial interface used by almost all the chips in the IBM tapeout, and frequently demonstrated his sincere desire to expedite the

group's work by investigating and applying useful software and hardware tools. I know that my PCB-designing and chip testing experiences were that much easier to accomplish thanks to the detailed instructions and tutorials he wrote for the benefit of the entire group.

Professors Joel Dawson and Vladimir Stojanovic sat on my committee from the day I proposed my thesis, and have been such an awesome support throughout the entire process. In preparing this thesis, Joel encouraged me to emphasize the big picture behind this work, which helped me present the project in a manner that will excite and intrigue the unfamiliar reader. Vladimir helped me get access to the high speed pattern generator that I desperately needed during testing, and graciously offered his assistance with acquiring any other lab equipment that I might need.

I am indebted to our group secretary, Valerie DiNardo, for all the time and effort she put in on my behalf to navigate MIT's incredibly complicated accounting and treasury departments. Without her vast knowledge, I would not have been able to obtain crucial purchase orders and reimbursements, and would have had to fight unruly vendors on my own.

Two people who are unrelated to this thesis project, but nevertheless played a very important role in my graduate career are John Bulzacchelli and Jungwon Kim. John was my mentor during my internship at IBM research, and was an incredible teacher and friend. His passion and dedication for engineering and research were truly an inspiration for me, and his selfless devotion to my project and my education is something that I will always remember with profound gratitude. Jungwon was my partner in my master's project, and together we traveled the long road (4 years, phew!) to demonstrating a working optical-electrical 40 GHz sub-sampling receiver and ADC. He is an optics guru extraordinaire, an incredibly talented scientist and engineer, and an all-around awesome person who will undoubtedly become a giant in his field.

Sungah Lee deserves very special words of acknowledgement and thanks. She was a constant companion, supporter and friend, and faithfully stayed at my side during the bulk of my Ph.D. When times were tough, she was always there to give me a

warm hug and to offer encouraging words. Without her comforting presence, this Ph.D. probably would not have been possible, and I am extremely grateful to her for all the loving care and support she gave me.

It almost goes without saying that my family has been a source of unflagging support and guidance for me during my many years at MIT. I know my parents and my grandmother have been praying for me everyday throughout my life, and the very fact that I am where I am at this moment in my life is largely a reflection of their constant and fervent requests on my behalf for God's blessing, protection and guidance. My mother, father and grandmother have also been my role models, and their examples of love, humility, integrity, leadership and professionalism have always served as a guiding light to me throughout my education. My sister Cathy and my brother-in-law George have been my cheerleaders for as long as I can remember, and always believed in my abilities whenever I was in doubt. At the same time, they generously cared for and lavished me with me so many gifts, yet never asked for anything in return other than my well being and happiness. I can't express how indebted I am to their tremendous loving support. My love and gratitude to everyone in my family is so enormous that it is ineffable; I only hope that I can make them proud in everything that I do.

I chose the passage from 2 Corinthians because of something very similar that my father told me when I was going through an extremely difficult time in graduate school: "In all things, God's grace is sufficient." This thesis, my graduate training, my education at MIT, and every blessing and hardship I've experienced in life are due to God's infinite grace and love. Through *all* times, good and bad, God never abandoned me but used the circumstances to make me stronger and shape me into the person I am today. If MIT has taught me anything, it is that I always need to have faith in His plan for my life.

Biography

Matt Park, American, b. 1981
A Portrait of the Artist as a Young Man
2000-2008
Oil on canvas
Museum of Questionable Art, Cambridge: Park Collection

Matthew Jeremiah Park was born in Rochester, New York, on September 4, 1981. He attended Masuk High School in Monroe, Connecticut from 1996 to 1998, and then Northern Valley Regional High School in Old Tappan, New Jersey from 1998 to 2000. He entered the Massaschusetts Institute of Technology (M.I.T.) in September 2000. As a member of M.I.T.'s VI-A co-op program, he was an internship student at M.I.T. Lincoln Laboratories, Lexington, Massachusetts in the summer of 2002, and at Linear Technology, New Chelmsford, Massachusetts in the summer of 2003. In January 2004, he began an undergraduate research study (UROP) in the M.I.T. Microsystems Technology Laboratory as part of the High Speed Circuit and Systems (HSCS) Group under the supervision of Professor Michael Perrott. During this time, he worked on a circuit implemention of the Dynamic Weighted Averaging (DWA) algorithm for use in a high bandwidth fractional-N frequency synthesizer. He received the B.S. degree from the Department of Electrical Engineering and Computer Science (EECS) at M.I.T. in June 2004.

From September 2004 until May 2005, he was a Research Assistant in the HSCS Group. His research in new opto-electronic receiver and analog-to-digital converter (ADC) architectures formed the basis of his M.Eng. thesis entitled *An Optical Electrical Sub-Sampling Down-Conversion Receiver with Continuous-Time* $\Sigma\Delta$ *Modulation.*

He received the M.Eng. degree in EECS in June 2005.

From June 2005 until August 2005, he was a Graduate Research Scientist at the IBM T.J. Watson Research Center, Yorktown Heights, New York, where he investigated low-power decision-feedback equalizer (DFE) architectures leveraging current integration. He returned to the HSCS Group in September 2005 to begin his doctoral research on high-resolution VCO-based ADC's. He successfully defended his dissertation entitled *A* 4^{th} *Order Continuous-Time* $\Delta\Sigma$ *ADC with VCO-Based Integrator and Quantizer* in November 2008, and received his Ph.D. degree in EECS in February 2009. His present research interests include mixed-signal circuit and systems design and opto-electronic systems.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Thanks to the speed enhancements accompanying scaling in CMOS, as well as continued innovations in mixed-signal circuit design, the past decade has seen dramatic changes in the applications of traditional analog-to-digital converter (ADC) topologies. Figure 1-1 plots the resolution versus input bandwidth of popular ADC topologies presented at ISSCC and VLSI from 1997-2008 [38]. As can be seen, the boundaries that had once distinctly separated specific architectures from each other have become quite blurred.

One of the most notable examples of this trend is the $\Delta\Sigma$ ADC, which has evolved from primarily serving niche applications requiring very high resolution at low speeds (16-24 bits, $<$ 500 kS/s [28, 58]), to becoming a formidable competitor to the pipeline ADC in high performance communication systems requiring high resolution and moderate bandwidths (10-12 ENOB, 10-100 MS/s) [36, 61, 52, 9, 65]. Interestingly, the scatter plot of Figure 1-1 also illustrates another major developing trend in the research of these $\Delta\Sigma$ ADC's—the move from discrete-time (DT) toward continuous-time (CT) architectures.

1.1 A Brief Overview of CT $\Delta\Sigma$ ADC's

The recent popularity of the CT $\Delta\Sigma$ ADC largely stems from its inherent anti-alias filtering ability [64, 41]. Such inherent anti-alias filtering is possible since the input

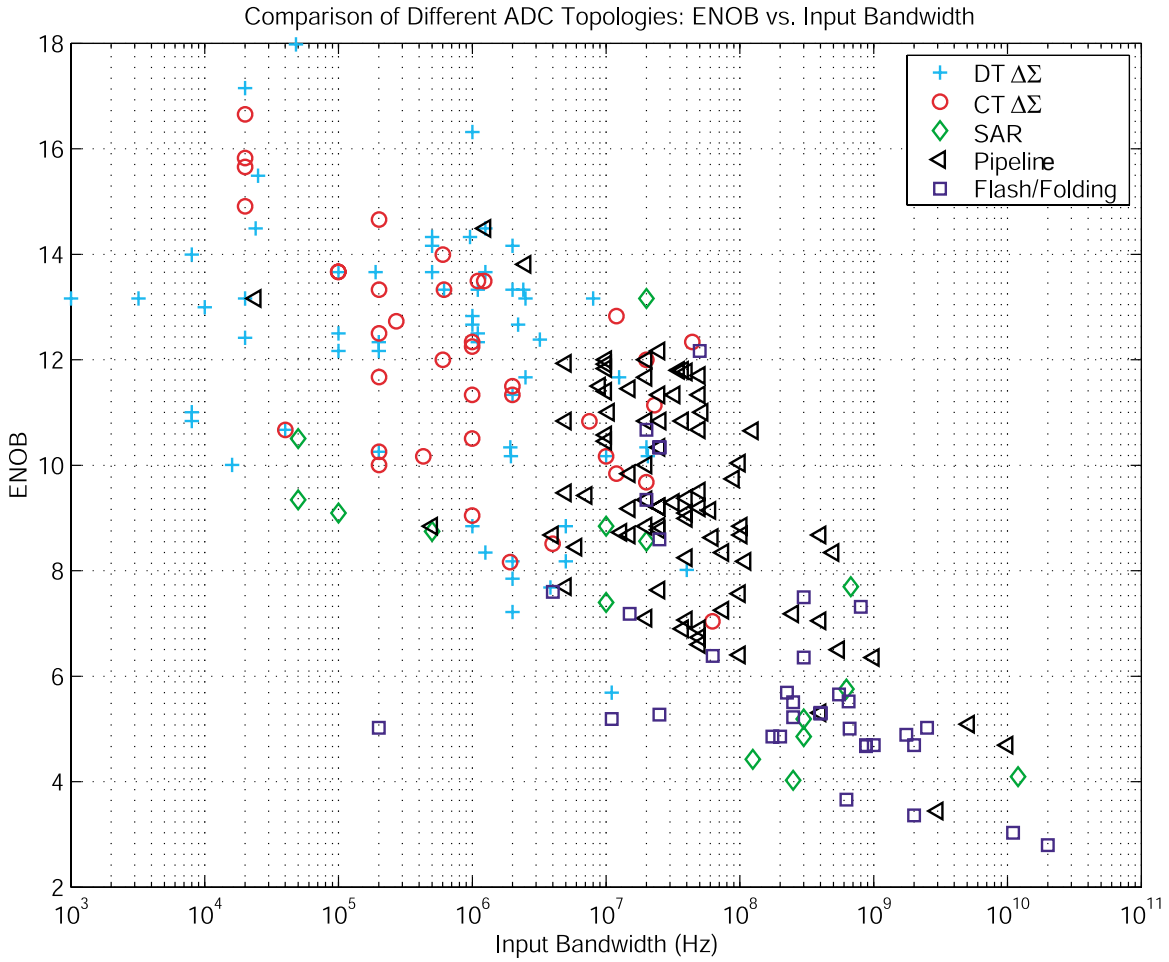
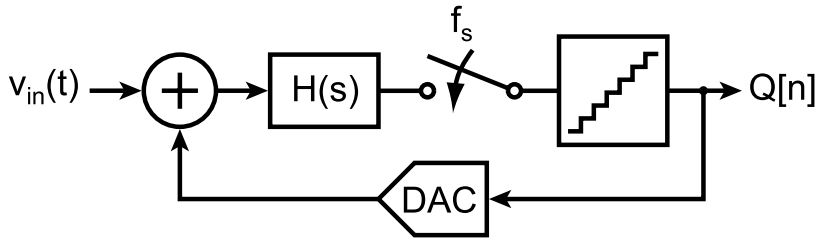
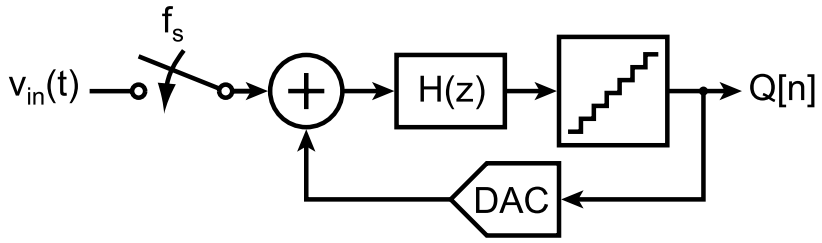


Figure 1-1: survey of the resolution and bandwidth of popular ADC topologies presented at ISSCC and VLSI from 1997-2008 [38].



(a)



(b)

Figure 1-2: (a) inherent anti-alias filtering due to location of sampler after loop filter in a CT $\Delta\Sigma$ ADC, and (b) risk of aliasing due to sampling of input-signal without any filtering in a DT $\Delta\Sigma$ ADC.

analog signal is first processed by the CT loop filter before being sampled by the quantizer (see Figure 1-2(a)). In contrast, the DT $\Delta\Sigma$ samples the input analog signal before it is applied to the loop filter, and therefore requires an explicit anti-alias filter preceding the ADC (see Figure 1-2(b)) [41]. The same is also true for any other DT ADC architecture (SAR, pipeline, flash, etc.), as sampling always occurs prior to the ADC input.

The CT $\Delta\Sigma$ ADC's inherent anti-alias filtering ability has also been widely touted in the literature as an elegant architectural means to simplify baseband filtering and digitization in wireless systems [10, 30, 16]. As shown in Figure 1-3(a), a conventional RF receiver would require an explicit low-pass filter prior to the DT ADC (pipeline, DT $\Delta\Sigma$, SAR, flash, etc.) to eliminate out-of-band interferers that would otherwise alias in-band. However, a properly designed CT $\Delta\Sigma$ ADC can leverage its inherent anti-aliasing ability to eliminate this low-pass filter, as shown Figure 1-3(b) [10]. Moreover, as scaling yields faster devices, there is even an effort to eliminate the IF

mixer and band-pass (BP) filter by leveraging a BP CT $\Delta\Sigma$ ADC to perform filtering and digitization, while performing the final down-conversion in the digital domain with a DSP [16, 30] (see Figure 1-3(c)).

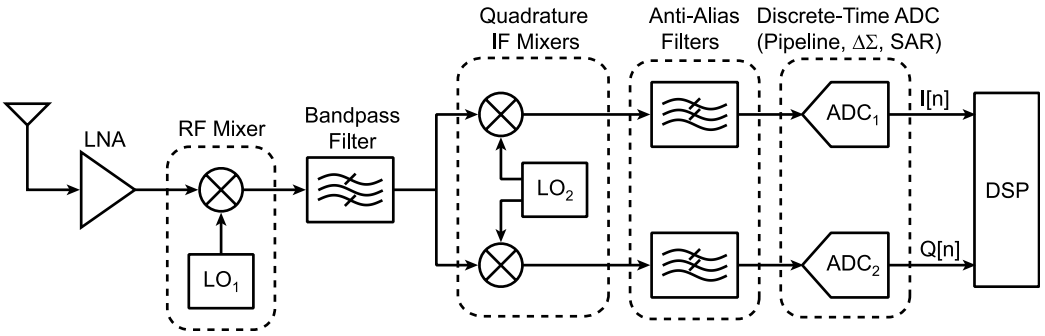
While anti-alias filtering can be performed using off-chip passives, doing so increases the system cost and consumes precious real estate on the PCB—an unacceptable tradeoff in many high volume, ultra-competitive commercial wireless applications where cost and form factor are paramount. Consequently, most recent wireless receiver architectures employing DT ADC's with wide input bandwidths (100 kHz-100 MHz) have opted to perform filtering on chip using active filters [32, 15, 37, 60, 34].

Unfortunately, designing an anti-alias active filter that introduces minimal noise and distortion has the drawback of high power dissipation and area consumption [57]. Indeed, a survey of recently published CT filters (see Table 1.1) has found that the power dissipation can vary from 10 mW to more than 100 mW depending on the desired noise, linearity and bandwidth. At the same time, the active filter's area can vary widely (from 0.1 mm^2 to more than 1 mm^2) depending on the filter order (with greater than 5th order typical) and the amount of on-chip capacitance ($>$ 100 pF common). Given the considerable power and area overhead involved with designing an explicit anti-alias filter, the inherent filtering ability of the CT $\Delta\Sigma$ is very attractive.

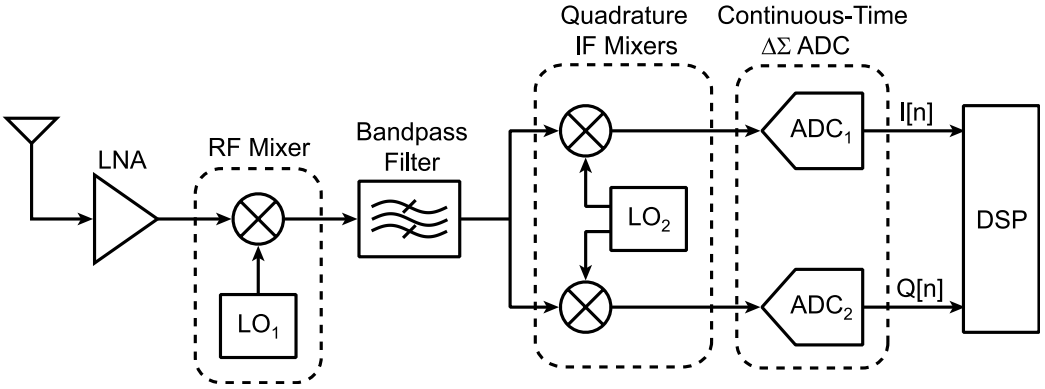
Reference	Order	Bandwidth (MHz)	Power (mW)	Area (mm^2)
[46]	4	60-350	70	0.15
[20]	7	30-100	210	3
[62]	16	0.45	12	2.5
[33]	3	0.93	26	0.5
[44]	10	19	22.5	0.7
[66]	7	1.92	11.6	2.86
[27]	5	2.1	11.6	1.35
[6]	8	15	11.9	Not Reported
[4]	6	0.005-5	6.1	1.25
[25]	5	2	10	Not Reported
[31]	5	19.7	18	0.32

Table 1.1: brief survey of recently published CT anti-alias filters.

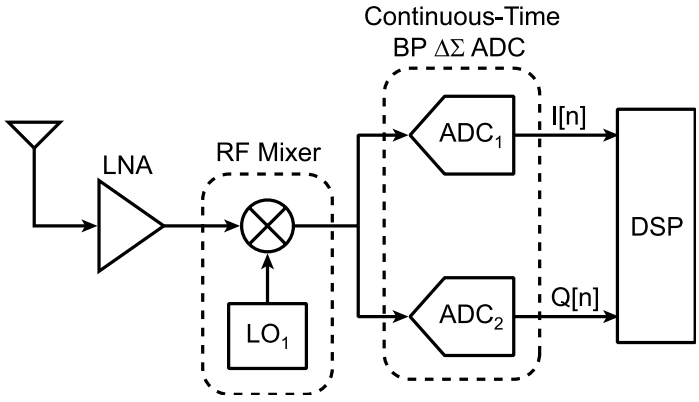
Despite its signal processing advantages, application of CT $\Delta\Sigma$ ADC's in such



(a)



(b)



(c)

Figure 1-3: prototypical receiver architectures assuming (a) an arbitrary DT ADC preceded by an explicit anti-alias filter (b) a CT $\Delta\Sigma$ ADC providing inherent anti-alias filtering, and (c) a bandpass CT $\Delta\Sigma$ ADC that eliminates the IF mixer, performs anti-alias filtering at the IF frequency, and downcoverters the IF signal in the digital domain using a DSP.

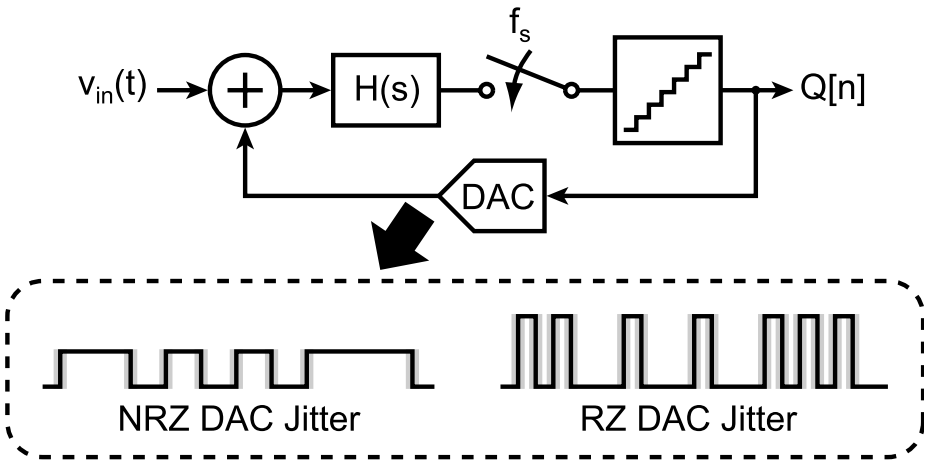


Figure 1-4: clock jitter appearing at ADC input due to modulation of charge in a 1-bit NRZ and RZ feedback DAC.

high performance applications was initially met with some skepticism due to concerns over the architecture's sensitivity to clock jitter. Indeed, early work on a CT $\Delta\Sigma$ ADC's with single-bit quantizers and DAC's [13, 42, 63] showed that such CT architectures were highly sensitive to clock jitter due to the modulation of DAC signal charge appearing directly at the ADC input (see Figure 1-4). In particular, the return-to-zero (RZ) DAC was demonstrated to have far greater jitter sensitivity compared to the non-return-to-zero (NRZ) DAC due to its modulation of more than *twice* the DAC charge at *every* sample [63]. Consequently, the SNR of these single-bit modulators decreased steadily with increasing clock jitter, typically limiting the converter resolution to no more than 10-11 bits.

Fortunately, recent work has shown that the SNR degradation due to clock jitter can be significantly reduced by pursuing a multibit quantizer and NRZ feedback DAC implementation [64, 36, 50, 65]. As shown in Figure 1-5, jitter now only modulates the DAC charge of the LSB's that change from sample-to-sample. Increasing the number of DAC bits causes jitter to affect a smaller fraction of the DAC full-scale signal, significantly reducing the error charge it introduces. At the same time, improved phase-locked-loop (PLL) design techniques applied to more modern fine line-width technologies have enabled high output clock frequencies with low-jitter performance (< 1 ps,RMS). Indeed, simple PLL architectures achieving GHz output frequencies

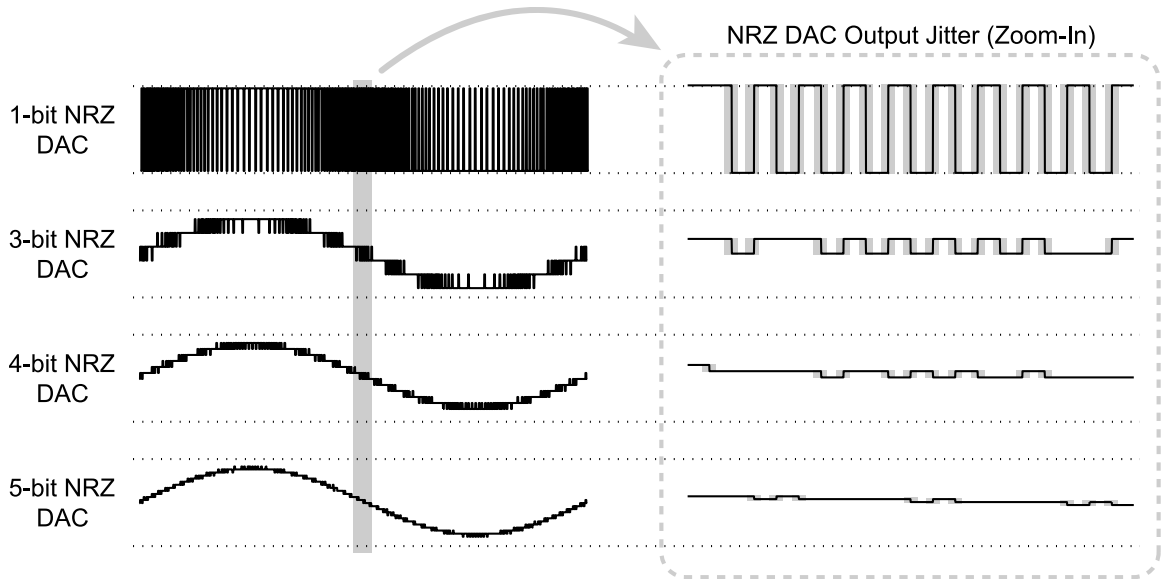


Figure 1-5: reducing the amount of charge modulation by clock jitter by increasing the number of bits in a multibit NRZ DAC.

with less than 1 ps,RMS jitter have become quite common in the recent literature [14, 56, 11, 21, 23].

Note, however, that the RZ DAC does have one advantage over its NRZ counterpart. As will be analyzed in greater detail later in this thesis, NRZ multibit DAC's have increased sensitivity to transient mismatches (ISI) but reduced sensitivity to clock jitter, while the opposite is true of RZ structures. It turns out that a dual RZ structure can also be employed to minimize sensitivity to both of these issues. While not implemented in the prototype, we will discuss the dual RZ structure in more detail in Chapter 5.

Given these advancements, modern multibit CT $\Delta\Sigma$ ADC implementations with dedicated on-chip PLL's have regularly achieved resolutions rivaling DT equivalents, while avoiding any significant performance limitation due to clock jitter [64, 36, 52, 65]. Indeed, as the industry's interests in CT $\Delta\Sigma$ ADC's and greater system integration continues to grow, the emphasis in research has shifted toward exploring new architectures that can continue to deliver high resolution, bandwidth and power efficiency in some the of the latest, deeply sub-micron technologies [9, 59, 54, 43]. In these highly digital environments, mixed-signal designers of CT $\Delta\Sigma$ ADC's (or of

any ADC topology, for that matter) will face new challenges as they strive to build high performance analog circuits while attempting to fully leverage the speed benefits accompanying device scaling.

1.2 Motivations for Investigating VCO-Based ADC's

Voltage controlled oscillator (VCO) based analog-to-digital converters (ADC's) have recently become a topic of great interest in the mixed-signal community [22, 26, 39, 29, 55]. In addition to having a very digital structure that benefits from technology scaling, the VCO presents a host of unique signal processing properties that are especially attractive in the design of oversampling converters. However, certain non-idealities—namely, non-linearity in the VCO's voltage-to-frequency translation—have limited the resolution of the VCO-based ADC to less than 8 effective number of bits (ENOB), pigeon-holing the architecture to niche low-power applications where such resolution is adequate [22, 3]. Indeed, only recently has the mixed-signal community demonstrated that feedback techniques could linearize the VCO-based ADC further, with the work in [55] demonstrating an SNDR of 67 dB in a 20 MHz bandwidth.

To that end, this thesis proposes a new 4th order CT $\Delta\Sigma$ ADC architecture that leverages a VCO-based quantizer to achieve 78 dB SNDR in a 20 MHz input signal bandwidth. The ADC has an over-sampling ratio (OSR) of 22.5, a 4-bit quantizer/DAC, consumes approximately 87 mW from a 1.5V supply (FOM = 330 fJ/conv), and is fabricated in a 0.13 μm CMOS process. The primary contributions of this thesis are (1) an architecture that overcomes the severe signal distortion caused by VCO Kv non-linearity, and (2) a methodology for performing first-order dynamic weighted averaging (DWA) on all feedback DAC's. Both of these contributions are essential in order to achieve a resolution $>$ 12 ENOB in a 20 MHz bandwidth.

As a motivation for pursuing a multi-bit VCO-based ADC architecture, this chapter will begin by highlighting the unique signal processing properties of VCO's that can be exploited in CT $\Delta\Sigma$ ADC design. An overview of prior VCO-based ADC architectures will then be provided, followed by a discussion of non-idealities that limited

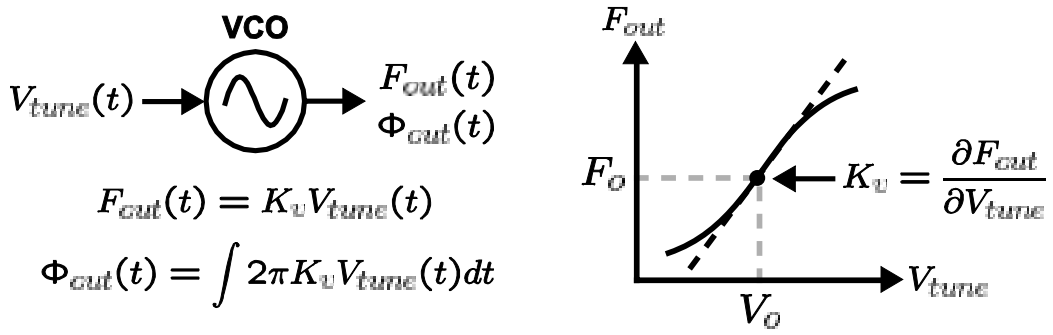


Figure 1-6: the VCO voltage-to-frequency and voltage-to-phase relationships.

performance. The proposed ADC architecture is then introduced through an example of a 1^{st} order CT $\Delta\Sigma$ ADC, which illustrates the significant improvement in linearity attained by directly leveraging the quantized VCO phase. The simple 1^{st} order case is then expanded to the proposed 4^{th} order CT $\Delta\Sigma$ ADC architecture. Finally, the high-speed digital architecture that performs dynamic element matching (DEM) using the DWA technique on all feedback DAC's is presented, with the VCO's unique structure that enables this high-speed technique highlighted. The chapter closes with an outline for the remainder of this thesis.

1.3 Benefits of a VCO-based ADC architecture

While a VCO has a variety of unusual and interesting properties, it has two traits that are especially attractive and relevant in the design of CT $\Delta\Sigma$ ADC's. First, the VCO behaves as a CT voltage-to-phase integrator. As shown in Figure 1-6, the instantaneous VCO output frequency $F_{out}(t)$ is proportional to the applied input voltage $V_{tune}(t)$ according to the voltage-to-frequency gain K_v [Hz/V]. The resulting VCO output phase $\Phi_{out}(t)$ is proportional to the time integral of the applied input voltage. Note that as long as the VCO oscillates, the VCO output phase will accumulate endlessly, even for a DC input. This implies that the VCO behaves as a CT integrator with infinite DC gain.

The value of a simple integrator structure that provides infinite DC gain cannot be emphasized enough. Indeed, with transistor intrinsic gains dropping rapidly at

each technology node, even the ability to achieve modest gains (> 40 dB) with a conventional amplifier topology is far from a trivial exercise, as will be discussed later in this thesis. Note, however, that the VCO integrator is not an ideal integrator even though it has infinite DC gain. Figure 1-6 again illustrates this point by indicating that the VCO output frequency is a non-linear function of the applied input voltage. Consequently, an input voltage signal that modulates the VCO control node will incur potentially high harmonic distortion, degrading the effective dynamic range of the VCO-based integrator.

A second property of interest is the digital nature of a ring-VCO's outputs. Note that while the VCO output phase and frequency are continuously varying, the VCO output itself toggles between two discrete levels, V_{DD} and GND, much like a CMOS digital gate (see Figure 1-7). Multi-phase (or equivalently, multi-bit) quantization can be accomplished by sampling the output phases of a ring oscillator with an array of D-flip-flops. Note that since the VCO phases are full-swing logic signals, the quantizer is robust to voltage offsets in the flip-flops. At the same time, only one VCO edge transitions at a given sampling instant, while the rest of the VCO phases saturate to either V_{DD} or GND. Consequently, the quantizer not only is less prone to generate metastable outputs, but also has guaranteed monotonicity without requiring any calibration.

The ease with which the VCO's digital output phases can be quantized can be better appreciated when the design of a conventional voltage flash ADC is considered. In the case of a voltage flash, the input signal applied to an array of comparators is typically restricted to be within an operating range, V_{HI} to V_{LO}. This range is usually less than the power supply range, V_{DD} to V_{SS}, and is further subdivided according to the number of quantization levels (see Figure 1-8) via a reference ladder. The voltage comparators must then sample and regenerate the resulting signal, which can be on the order of tens of millivolts, and therefore must not only be designed to have high gain and high bandwidth, but also must operate over a wide input common-mode range. To reduce the probability of generating metastable outputs, high-bandwidth preamplifiers typically precede the voltage comparators, consuming additional power.

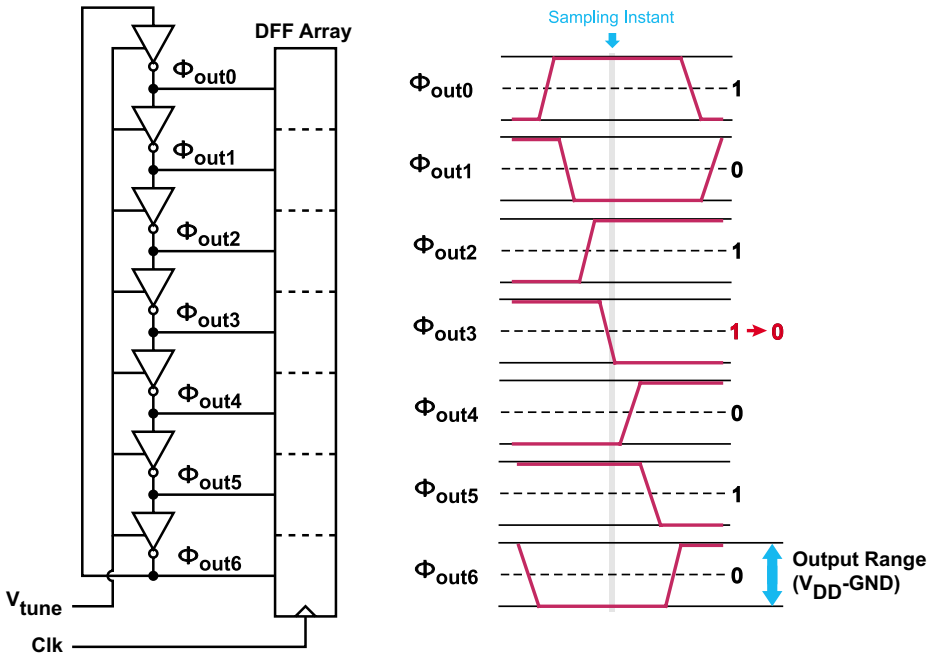


Figure 1-7: multibit quantization with a ring oscillator structure.

Finally, since the comparators/preamplifiers can have offset voltages in excess of one or more LSB's, large device sizes must be used to reduce these random offsets to ensure monotonicity. This in turn will also require proportionately larger bias currents in order to maintain the circuit's speed, resulting in both an area and power penalty. While the aforementioned list of design considerations is by no means exhaustive, it is clear that the design of conventional voltage flash quantizers is far from trivial.

1.4 Prior VCO-Based ADC Architectures

The earliest VCO-based ADC was proposed more than thirty years ago for use in a digitally controlled switching regulator [7], and a similar topology was later rediscovered in the superconductivity community five years later [24]. While the exact implementation of the converters differed due to the choice of technology (i.e., semiconductor vs. superconductor), the overall architecture for each was essentially the same, and is shown in Figure 1-9(a). Here, the ADC comprises a single-phase output VCO, a counter, and sampling register. As the analog input signal modulates the VCO frequency via the tuning node, the counter continuously accumulates the num-

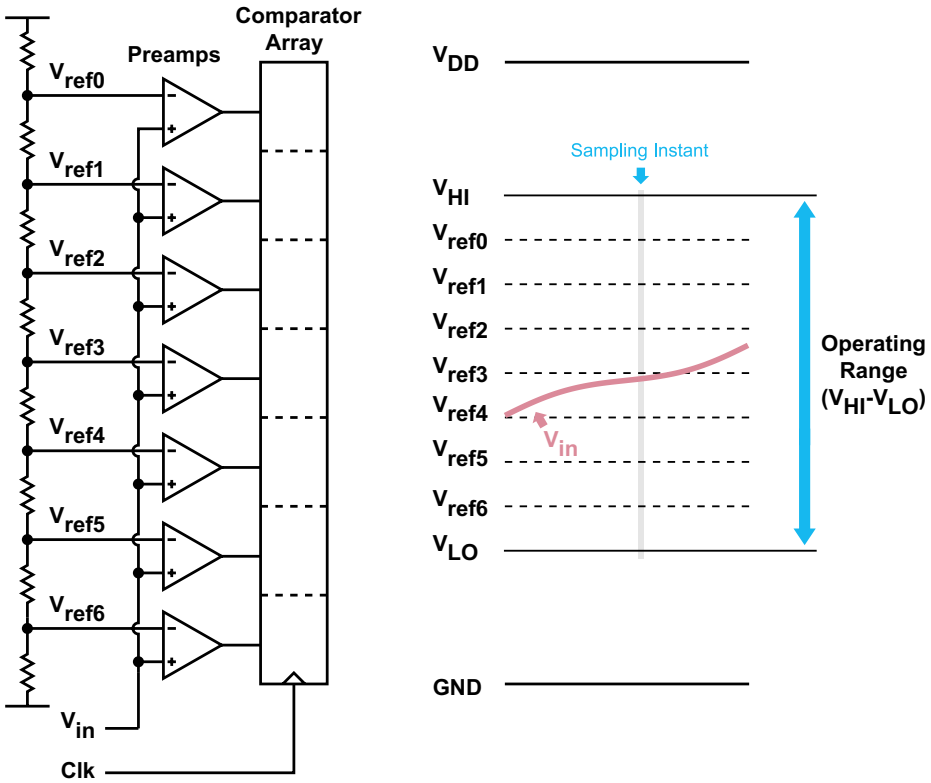
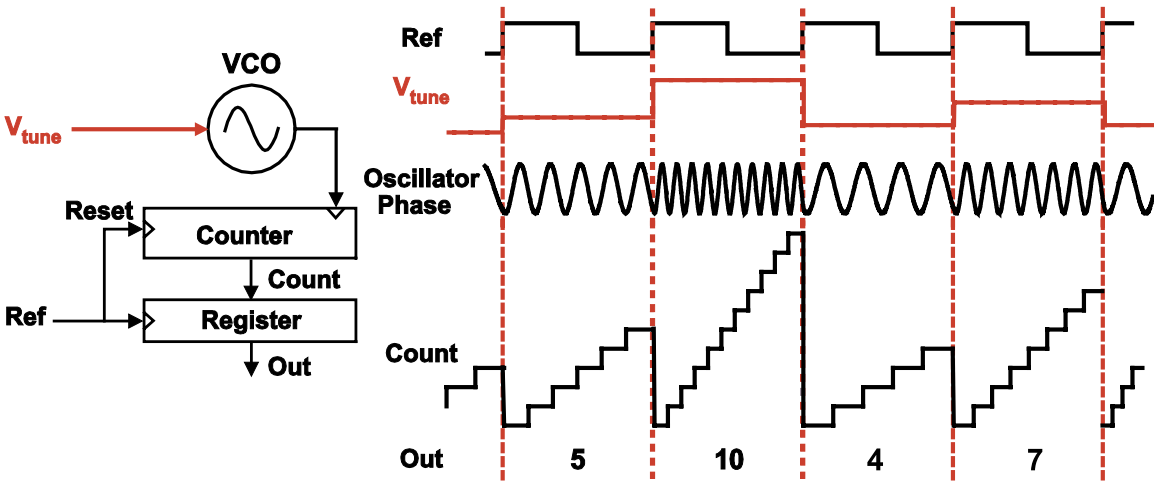


Figure 1-8: multibit quantization using a conventional voltage flash architecture.

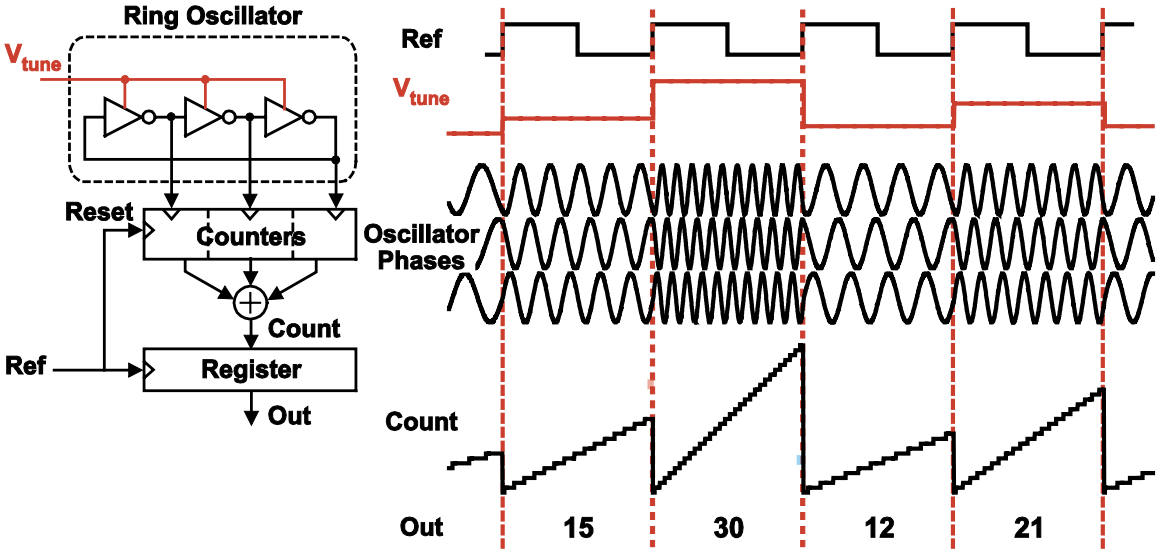
ber of transitioning edges during the sample period. At the end of the period, the resulting count is sampled by a register, the counter reset to zero, and the process repeated. As can be seen from the figure, the sampled count is proportional to the oscillation frequency of the VCO, and therefore the input signal level.

To improve the resolution of the ADC, a ring-oscillator structure was adopted in [22] to generate multiple VCO output phases (see Figure 1-9(b)). Here, each phase output from the ring-VCO drives a counter input, producing a total count with higher resolution than the single-phase VCO-based ADC of [7] and [24]. A serious drawback of this multi-phase approach, however, is that the counter becomes proportionately more complicated to design, and typically consumes greater power and area in order to meet timing and data throughput constraints. At the same time, both the single-phase and multi-phase VCO-based ADC must contend with error incurred when the counter misses a VCO edge during reset.

Fortunately, it is possible to eliminate the counters entirely under certain operat-



(a)



(b)

Figure 1-9: (a) single-phase and (b) multiple-phase counting ADC architectures.

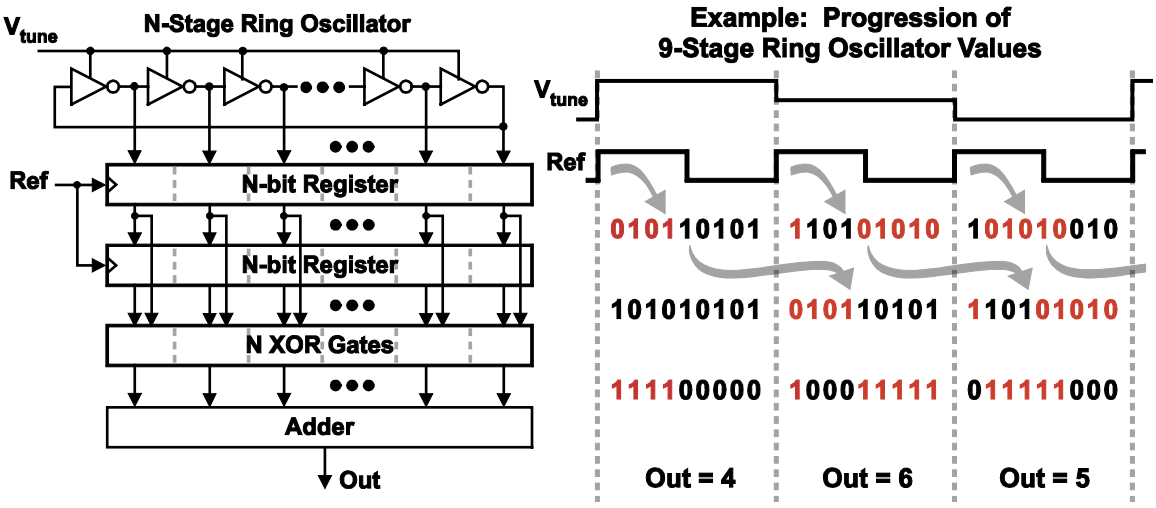


Figure 1-10: a multi-phase VCO-based ADC that eliminates the counter by oversampling the VCO phase.

ing conditions [22]. In particular, when the sample rate is chosen such that the VCO elements do not transition more than once in a given sample period, the counters can be replaced with registers and XOR gates (see Figure 1-10). These gates process the sampled VCO phases, and generate a thermometer code that, when summed, is equivalent to the output count of the counter-based VCO-based ADC. This equivalence is possible because the register-XOR combination effectively performs a first-order difference, or discrete-time differentiation, of the sampled/quantized VCO phases. Since frequency is the derivative of phase, the resulting outputs will be proportional to the input voltage applied to the VCO control node. Note that the counter-based VCO ADC's of Figures 1-9(a) and 1-9(b) also performs a first-order difference during reset by effectively subtracting out the previously quantized VCO phase. Consequently, the output count is also proportional to the VCO frequency and to the applied input voltage signal.

A general model for the counter-based and XOR-based VCO-based ADC architectures is shown in the top-half of Figure 1-11. A subtle benefit of this voltage-to-frequency ADC is that the quantization noise will be first-order noise shaped due to the post-quantization differentiation, as illustrated in Figure 1-11 [22]. Furthermore, the architecture precludes the feedback DAC needed in a classical first-order $\Delta\Sigma$

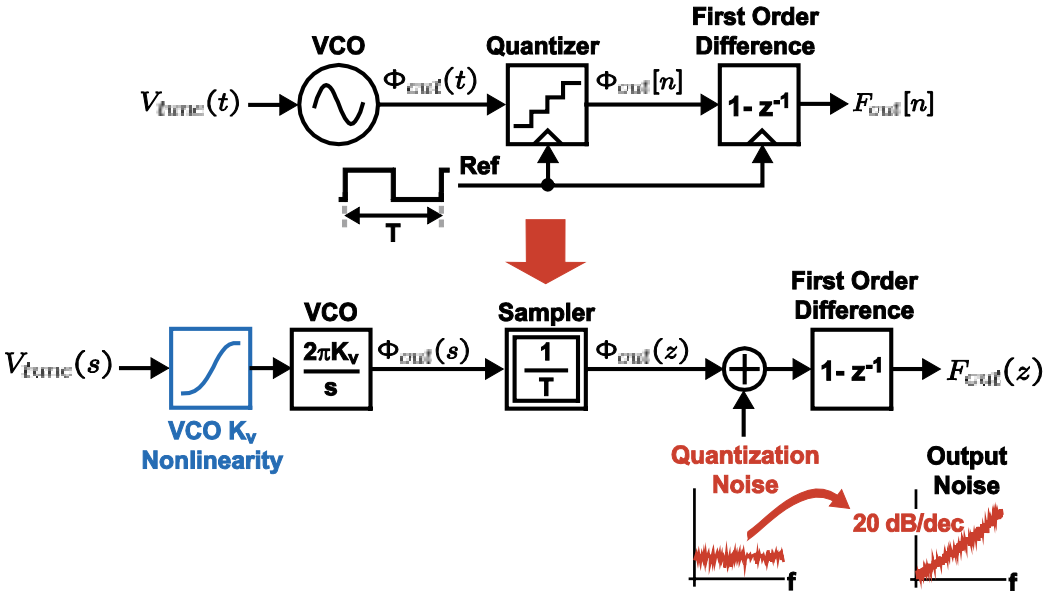


Figure 1-11: analytical model of the voltage-to-frequency VCO ADC, and the equivalent frequency domain block diagram.

ADC, greatly simplifying design. While the earlier works in [7] and [24] apparently did not recognize the inherent noise-shaping of the voltage-to-frequency VCO ADC, the architecture and its noise-shaping ability was analyzed and tested thoroughly in [22]. As will be discussed next, the non-linearity of the VCO's voltage-to-frequency gain, K_v, severely limits the resolution of this open loop architecture.

For an over-sampling ratio (OSR) of 2000, the $\Delta\Sigma$ ADC in [22] achieved a peak SNDR of 71 dB in a 500 Hz bandwidth when the input signal was approximately -36 dBFS. But when the input was increased to -2 dBFS, harmonic distortion arising from K_v non-linearity caused the SNDR to drop down to 44 dB. To mitigate the impact of this non-linearity, the authors in [22] suggested reducing the maximum allowable input signal such that distortion arising from the K_v non-linearity can be minimized. Unfortunately, this solution not only sacrifices a significant amount of DR, but also is not feasible when the desired bandwidth approaches the Megahertz range since such a high OSR is impractical.

Subsequent work sought to suppress the K_v non-linearity by embedding the VCO ADC from [22] in the loop filter of a classical $\Delta\Sigma$ ADC. A CT $\Delta\Sigma$ architecture proposed in [26] achieved second-order noise-shaping by preceding the multi-phase VCO

quantizer with an opamp-based integrator, and using a multi-bit feedback DAC. The DT $\Delta\Sigma$ architecture in [39] tried to bypass a multi-bit DAC implementation and the required dynamic element matching (DEM) overhead by using a frequency difference detector that pulse-width modulated a one-bit DAC. However, this approach had additional complexities in the frequency difference detector design, and lost the inherent first-order noise-shaping provided by the VCO quantizer. While both of these architectures intuitively should improve linearity, only behavioral simulation results that tended to downplay or ignore the impact of the K_v non-linearity were presented. Consequently, a fair comparison to the work in [22] cannot be made.

Fortunately, a modified version of the ADC in [26] was actually implemented and provided measured results in [55]. As shown in Figure 1-12, this third-order CT $\Delta\Sigma$ ADC achieved an extra order of noise shaping without a second op-amp integrator by creating a passive pole with a large on-chip capacitor. At the same time, the architecture in [55] leveraged the algorithm patented in [35] to automatically shape the feedback DAC mismatch by directly connecting the VCO quantizer output bits to the unit elements. As illustrated in Figure 1-12, the scheme leveraged the periodic cycling of ring-VCO delay elements and the inherent VCO integration such that the first-order difference generated the equivalent dynamic weighted averaging (DWA) sequence.

The measured results presented in [55] demonstrated the benefits of using negative feedback with a high gain loop filter to reduce the impact of VCO K_v non-linearity. For a signal bandwidth of 20 MHz and an OSR of 25, the CT $\Delta\Sigma$ ADC was able to achieve a peak SNDR of 65.7 dB for a -15 dBFS input signal. This represents a 20 dB improvement compared to the open loop voltage-to-frequency VCO-based ADC from [22]. However, when the signal power was increased to -3 dBFS, distortion tones from K_v non-linearity caused the SNDR to drop below 50 dB.

While the brute-force application of higher loop filter gain could help reduce the signal distortion further, a more elegant architecture that can directly address the source of non-linearity is desirable. As will be seen in the next section, simply changing the output variable of interest—from frequency to phase—can effectively eliminate

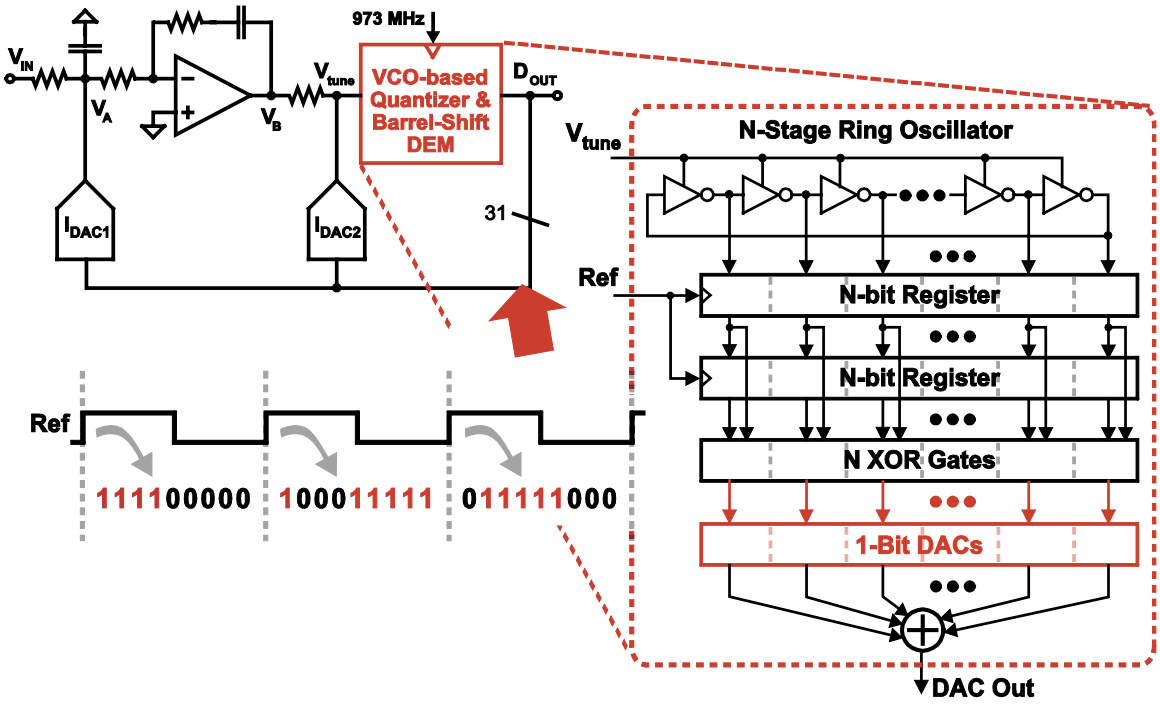


Figure 1-12: VCO-based ADC that achieved third-order shaping with feedback and an additional passive and active integrator [55].

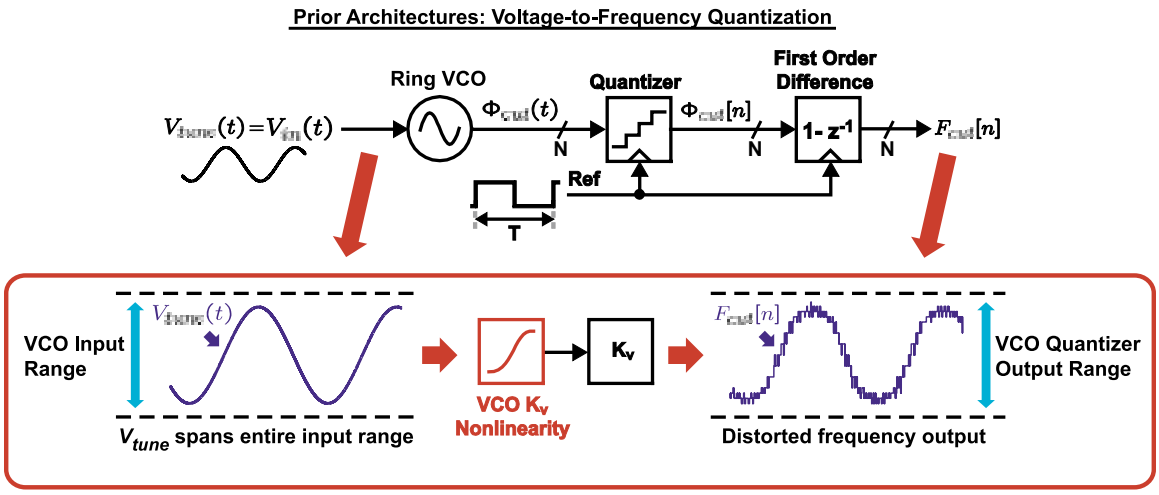
the impact of signal distortion arising from K_v non-linearity.

1.5 Proposed Continuous-Time $\Delta\Sigma$ ADC Architecture

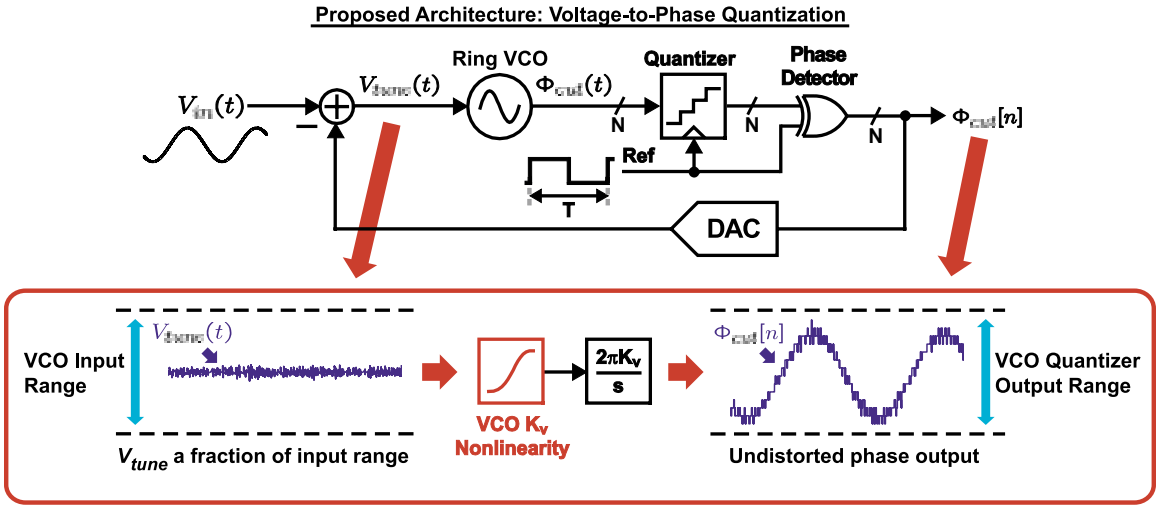
1.5.1 Voltage-to-phase quantization

The previous section revealed that the resolution of prior VCO-based ADC's was primarily limited by distortion arising from the VCO K_v non-linearity. While negative feedback techniques did manage to suppress the distortion by more than an order of magnitude, non-linearity still prevented the ADC from achieving its full dynamic range. Consequently, it is clear that a more robust linearization technique is needed in order to extend the performance and utility of VCO-based quantization.

To that end, this thesis proposes a new VCO-based ADC architecture that overcomes the SNDR limitation imposed by the VCO's non-linear K_v characteristic. The



(a)



(b)

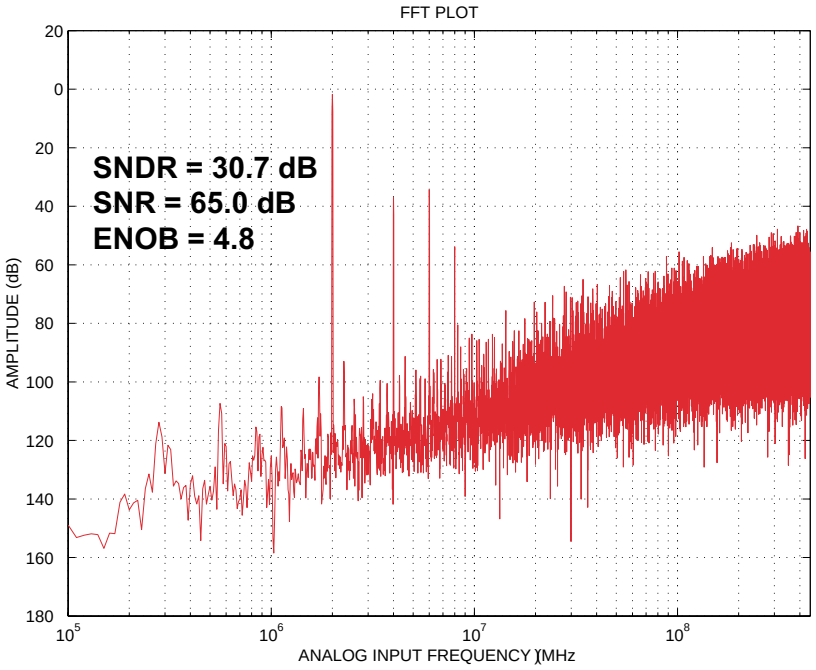
Figure 1-13: (a) prior voltage-to-frequency VCO-based ADC architecture that suffered from distortion due to K_v non-linearity, and (b) proposed voltage-to-phase VCO-based ADC that is immune to distortion caused by K_v non-linearity.

basis for the architecture can be understood by first considering the example of the open-loop first-order CT $\Delta\Sigma$ from [22] (see Figure 1-13(a). Here, and in all subsequently published architectures [26, 55, 3], the VCO output frequency is the desired output variable due to its proportional relationship with the input signal. Therefore, to exercise the full DR of the VCO quantizer, the input signal to the VCO must span the entire non-linear transfer characteristic, and incur harmonic distortion. However, if it were possible to leverage the VCO output phase, then it would not be necessary to span this non-linear transfer characteristic. Since the VCO behaves as an ideal voltage-to-phase integrator and typically has a large K_v, small perturbations at the tuning node on the order of tens of mV are sufficient to shift the VCO phase by a substantial amount.

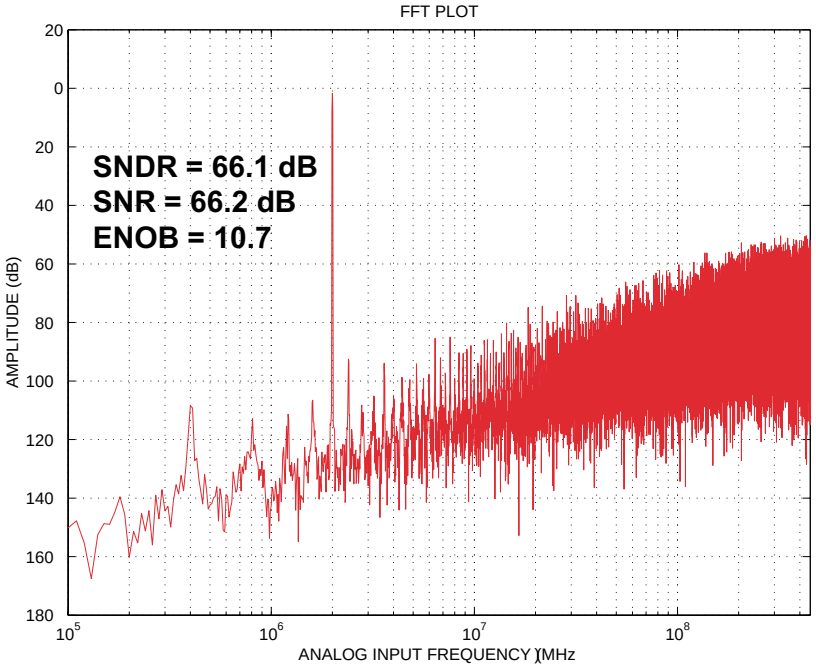
Of course, it is not feasible to use an open-loop integrator with infinite DC gain since frequency offsets, drifts, and temperature variations will cause the VCO output phase to saturate the phase detector that follows. At the same time, the input signal level is restricted to being no more than a few tens of mV, which is a severe restriction on the dynamic range of the ADC. Negative feedback offers a simple solution to this problem, as illustrated in Figure 1-13(b). Here, the VCO phase is sampled and quantized by registers, and compared to a reference phase via a phase detector. The output of the detector then drives a multibit DAC, which subtracts the previously quantized value from the input signal applied to the VCO. The resulting residue is then applied to the control node of the VCO, and integrated during the next cycle.

Note that the feedback loop shown in Figure 1-13(b) is in fact a first-order CT $\Delta\Sigma$ ADC loop, and will therefore first-order shape the VCO quantization noise. While this noise-shaping does require a feedback DAC (as opposed to the open-loop noise-shaping achieved in [22]), such a DAC would nonetheless be required in any architecture that embedded the VCO in a higher order $\Delta\Sigma$ loop filter, as was done in [26, 55]. As will be explained later in this section, the primary disadvantage of using the VCO output phase instead of frequency is the loss of automatic DWA sequence generation.

As shown in Figures 1-14(a) and 1-14(b), the VCO voltage-to-phase quantizer improves the SNDR of the converter significantly. Here, the ADC's of Figures 1-



(a)



(b)

Figure 1-14: FFT's generated from the behavioral simulation of the 5-bit (31-stage) VCO-based quantizer assuming (a) the prior voltage-to-frequency and (b) the proposed voltage-to-phase architectures. SNDR is calculated over a 20 MHz bandwidth, a -1 dBFS input signal, and a sample rate of 1 GHz.

13(a) and 1-13(b) are modeled and simulated using the CppSim behavioral simulator [48] (a tool that will be described in greater detail in the next chapter), and the corresponding FFT's plotted assuming a -1 dBFS input signal and 1 GHz sample rate. Note that in both cases, VCO non-linearity similar to that in [55] is included in the model by describing the voltage-to-frequency transfer characteristic with a fourth-order polynomial. All other circuit non-idealities are excluded. From Figure 1-14(a), it is obvious that the harmonic distortion in the voltage-to-frequency VCO quantizer of [22, 55] is also present here, limiting the SNDR to roughly 30 dB in a 20 MHz bandwidth. But for the voltage-to-phase VCO quantizer of Figure 1-14(b), the distortion tones are almost completely eliminated. Indeed, the SNDR is limited primarily by the quantization noise, to approximately 66 dB in a 20 MHz bandwidth.

1.5.2 Proposed 4^{th}-order CT $\Delta\Sigma$ Loop Filter

The simulation results from the previous section clearly showed the improved linearity that can be obtained when using a VCO voltage-to-phase quantizer. In reality, thermal noise, DAC mismatch, and other noise and error terms will add on top of the quantization noise floor, further degrading SNDR. To ensure high resolution, it is necessary to expand the loop filter and go beyond first-order noise shaping so that quantization noise can be further suppressed. Ultimately, the converter SNDR should be limited by thermal noise sources, and not by in-band quantization noise.

A fourth-order loop filter was chosen for this thesis due to its high quantization noise shaping ability (SQNR $>$ 95 dB in 20 MHz BW). Traditionally, such a high-order loop filter would be implemented using a cascade of integrators and feed-forward paths, with summation of all signals occurring at the input of the quantizer (see Figure 1-15). This architecture also has the advantage of enabling easy compensation of feedback loop delay by using an additional feedback DAC (labeled DAC_B in Figure 1-15) around the quantizer to obtain the desired loop filter impulse response [64].

In the proposed architecture, the quantizer is preceded by the VCO voltage-to-phase integrator, precluding the implementation shown in Figure 1-15. Fortunately, the filter can still be realized by replacing one of the feed-forward paths with an

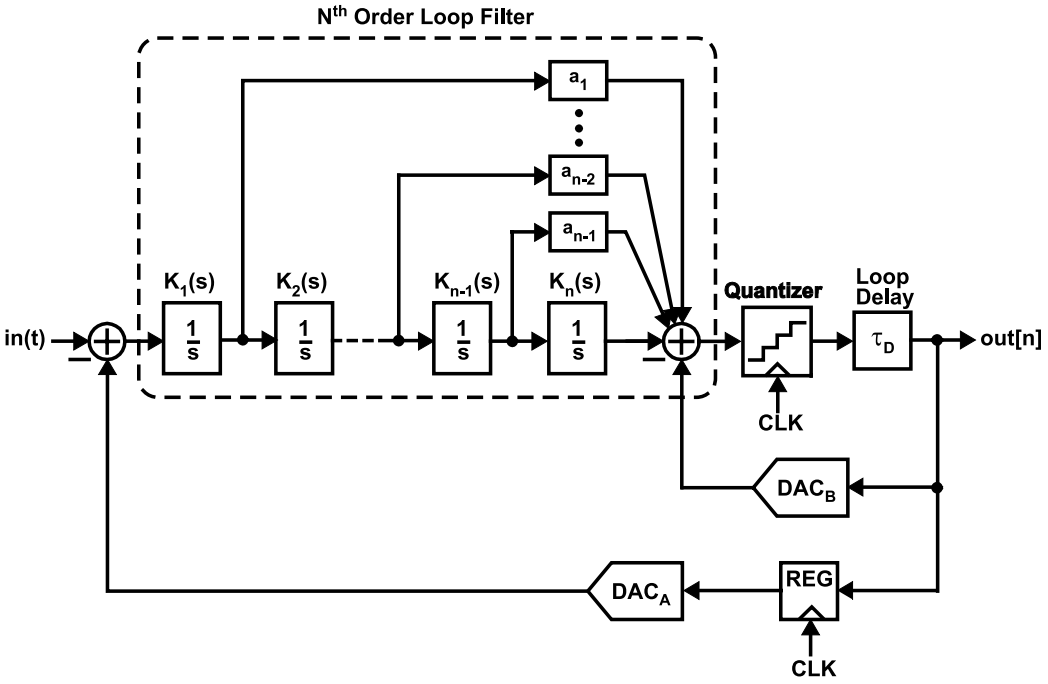


Figure 1-15: loop delay compensation using a second feedback DAC (DAC_B) around the quantizer to generate the desired filter impulse response [64].

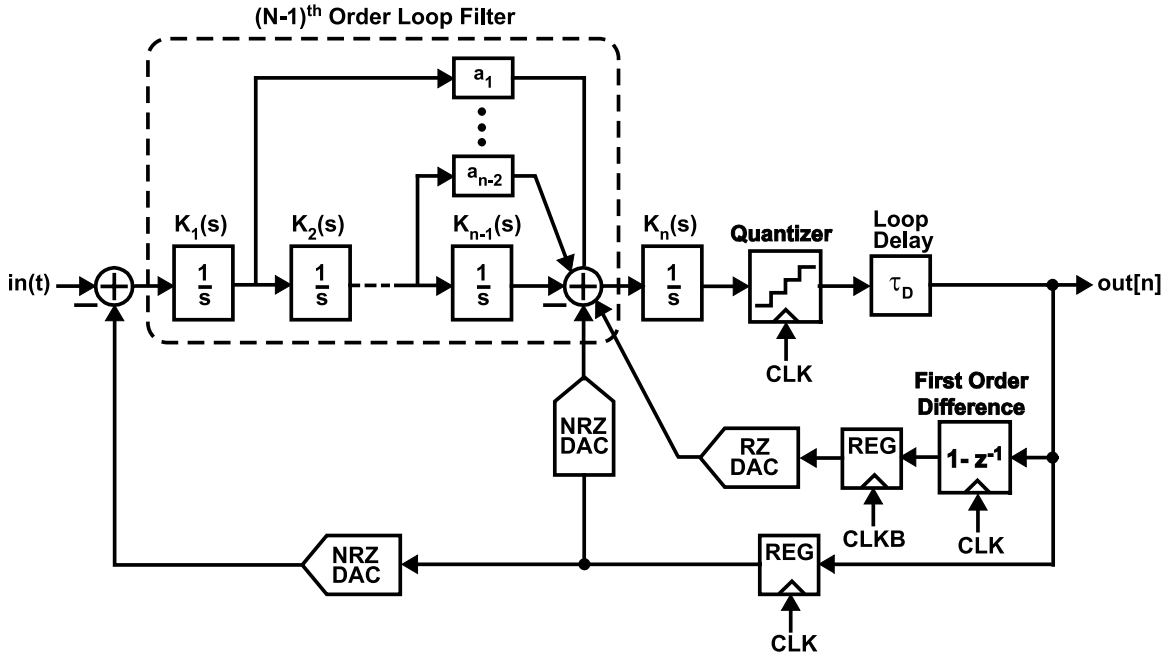


Figure 1-16: loop delay compensation by differentiating the quantizer output and then integrating the resulting DAC signal.

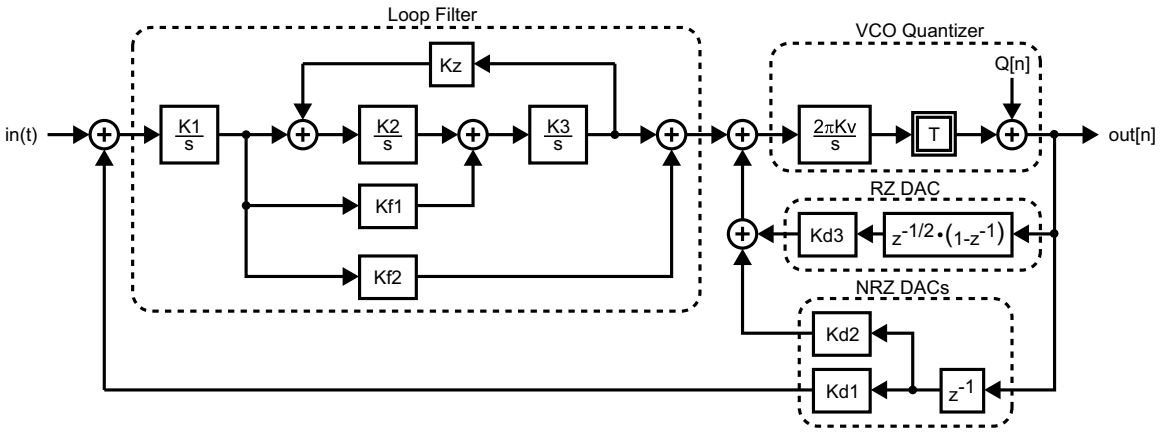
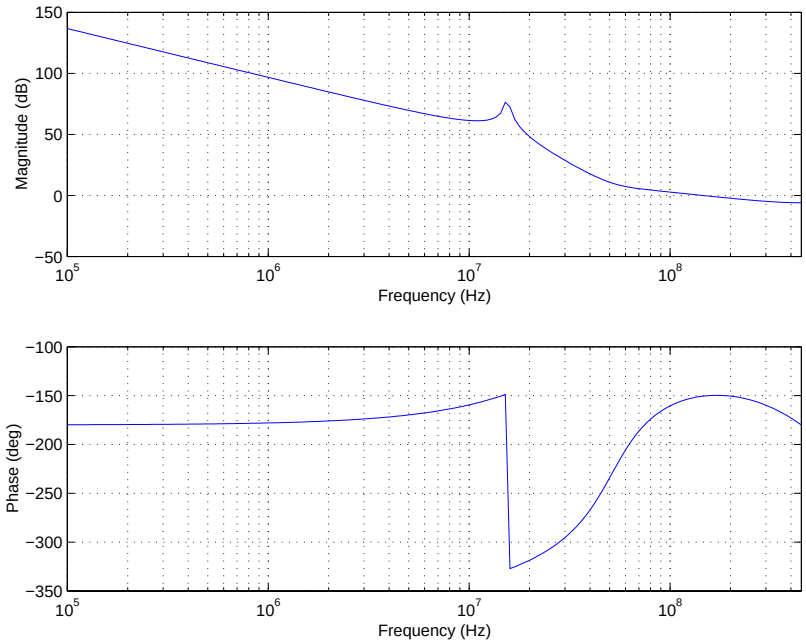


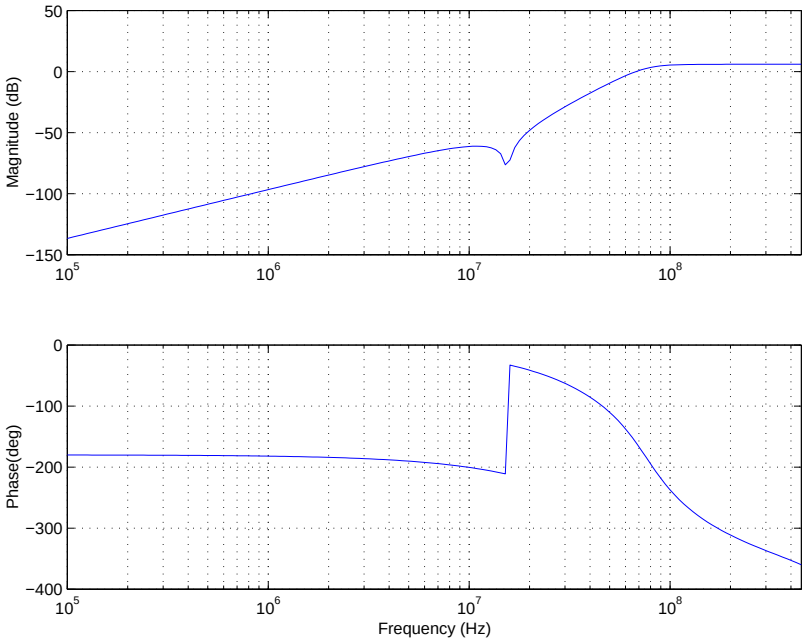
Figure 1-17: loop filter block diagram with VCO quantizer and feedback DAC's indicated.

additional DAC feedback path, modifying the filter coefficients, and performing signal summation at the input of the final integrator of the loop filter (see Figure 1-16). At the same time, loop delay compensation can still be accomplished by differentiating the quantizer output, and then integrating the result using the same final integrator. In the case of the VCO quantizer, the derivative corresponds to its frequency, and is easily obtained by performing a first-order difference using XOR gates and registers as done in [55]. Note that the loop delay compensating DAC will have its unit element mismatch noise shaped by the automatic DEM that results from the voltage-to-frequency conversion. Furthermore, note that the delay compensating DAC is a return-to-zero (RZ) DAC in order to absorb the propagation delays of the quantizer and first-order difference logic. As described earlier in this thesis, an RZ DAC was not used for the main feedback DAC due to its heightened sensitivity to clock jitter.

A block diagram for the proposed 4^{th} order loop filter with feed-forward and feedback stabilization is shown in Figure 1-17, and the filter coefficients shown in Table 1.2. The coefficients for the filter were chosen using the Schreier Delta-Sigma Toolbox [51]. Since the toolbox returns coefficients for a DT filter, the equivalent CT loop filter coefficients were obtained by applying the `d2c` (discrete-time to continuous-time transformation) function available in the MATLAB Signal Processing Toolbox. Bode plots of the ideal loop filter and noise transfer function (NTF) are shown in Figure 1-18(a) and 1-18(b), respectively.



(a)



(b)

Figure 1-18: Bode plot of the (a) loop filter and (b) noise-transfer function (NTF) assuming a clock frequency of 900 MHz (OSR=22.5).

Coefficient	Value
K1	900.0e6
K2	135.0e6
K3	43.95e6
Kf1	1.2147
Kf2	0.2043
Kz	1.5973
Kv	900.0e6
Kd1	1.0000
Kd2	0.4294
Kd3	0.6738

Table 1.2: coefficients of the proposed loop filter.

The loop filter schematic is shown below in Figure 1-19. Opamp-RC integrators were chosen over Gm-C integrators for their higher linearity and ability to drive resistive loads. Each integrator comprises a fixed capacitance and a 5-bit binary weighted capacitor bank, which enables the RC time-constant to be tuned in 5% steps over the combined resistor and capacitor process variation of +/- 40%. An additional amplifier is eliminated by using passive resistors to perform the summation of the main signal path and the feed-forward paths. Note that a pole formed by the summing node resistance and the wire and device capacitances from the VCO and feedback DAC's can degrade loop stability. Consequently, the summing node impedance is chosen low enough so that the additional phase lag from the parasitic pole is minimal.

1.5.3 First-order dynamic weighted averaging (DWA) sequence generation

Since excess feedback loop delay compromises the stability of CT $\Delta\Sigma$ ADC's, it is crucial that DEM algorithms employed in the feedback path finish processing as quickly as possible. While one sample period of delay can be compensated using the method described in [64], the DEM still has little time to finish processing when the setup-and-hold times of the retiming DAC latches and the clock-to-Q delay of the quantizer are factored in. Consequently, prior architectures that have implemented DEM in the feedback have seldom operated faster than a couple hundred MHz. In

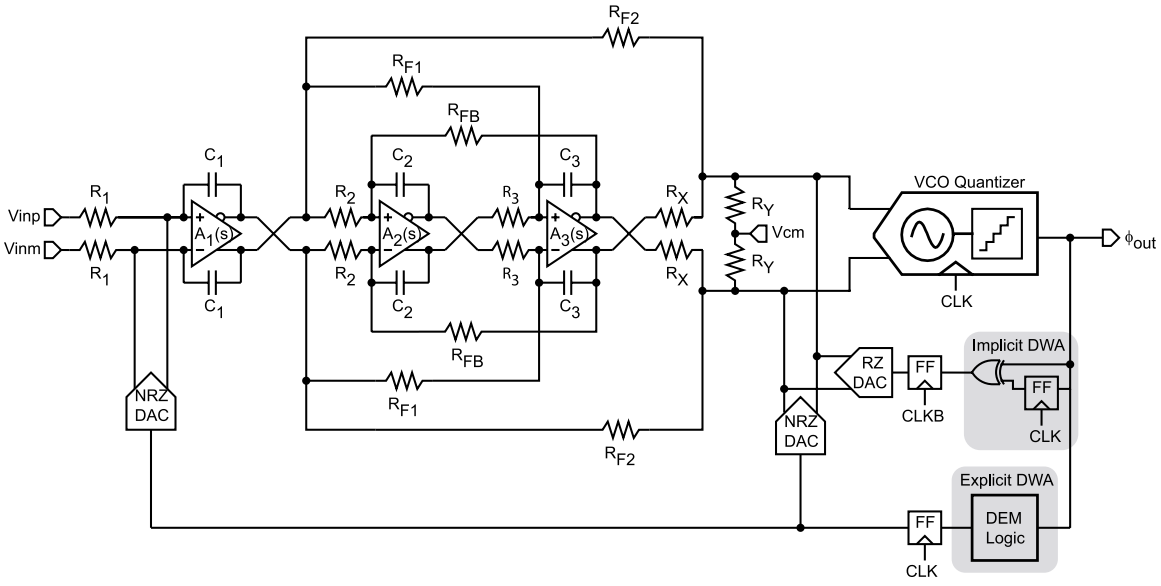


Figure 1-19: schematic of the proposed 4^{th}-order CT $\Delta\Sigma$ ADC with VCO quantizer.

the case of the 640 MHz clocking frequency of [36], the authors simply eliminated the DEM, and instead relied on very careful device sizing and layout techniques to obtain the best DAC unit element matching possible.

In this project, greater than 12-bit precision in a 20 MHz bandwidth is desired, making DEM a necessity (see explicit DWA in Figure 1-19). First-order DWA is chosen for its excellent mismatch noise-shaping performance and easy implementation. While increasing the OSR and the number of quantizer bits will reduce inband mismatch noise power for a given bandwidth, the subsequent increase in complexity, power consumption, and delay of the DWA discourages this approach. Ultimately, a converter sample rate of 900 MHz and a 4-bit quantizer were chosen as a compromise to these tradeoffs.

A direct implementation of a first-order DWA algorithm is shown in Figure 1-20, which mimics the accumulation and differentiation of the VCO voltage-to-frequency translation that automatically generates a DWA pattern. Unfortunately, the architecture suffers from a cascade of propagation delays, the most serious coming from the N-bit accumulator ($t_{pd,acc}$) and the thermometer-to-binary ($t_{pd,t2b}$) encoders. An equation describing the timing constraint of the DWA is shown below:

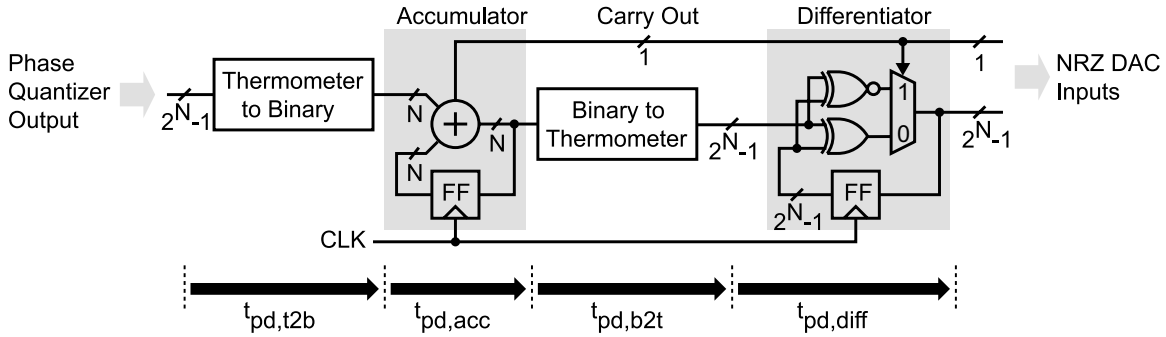


Figure 1-20: the direct implementation of the DWA algorithm and its linear cascade of propagation delays.

$$t_{pd,t2b} + t_{pd,acc} + t_{pd,b2t} + t_{pd,diff} < T - t_{clk2q} - t_{pd,det} - t_{sh,dac} \tag{1.1}$$

where T is the sample period, $t_{pd,t2b}, t_{pd,acc}, t_{pd,b2t}$ and $t_{pd,diff}$ are the propagation delays of the thermometer-to-binary encoder, accumulator, binary-to-thermometer encoder, and differentiator, respectively, and $t_{clk2q}, t_{pd,det}$ and $t_{sh,dac}$ are the clock-to-Q delay of the phase quantizer, the propagation delay of the phase detecting logic, and the setup-and-hold time of the DAC retiming latch, respectively.

Note that the propagation delay of the phase quantizer (t_{clk2q}) as well as the sample and hold time of the feedback DAC retiming latches ($t_{sh,dac}$) further reduce the timing margin. At the same time, pipelining is not an option since the data must propagate through the DWA in less than a sample period. In order to meet timing, each block must compute a result in a fraction of a sample period, a requirement that necessitates high power consumption, and may not even be feasible in the given 0.13 μm technology.

A contribution of this thesis is an improved DWA architecture that can meet the timing constraints without the excessive power dissipation of the direct approach. As shown in Figure 1-21, the propagation delay of the DWA can be significantly reduced by rotating the quantizer output thermometer code with the aid of a barrel shifter and a rotating pointer. A depiction of the thermometer code shifting in time is shown in the figure, and illustrates the benefit of the proposed approach. Note that the number of times that the current quantizer thermometer code needs to be shifted by

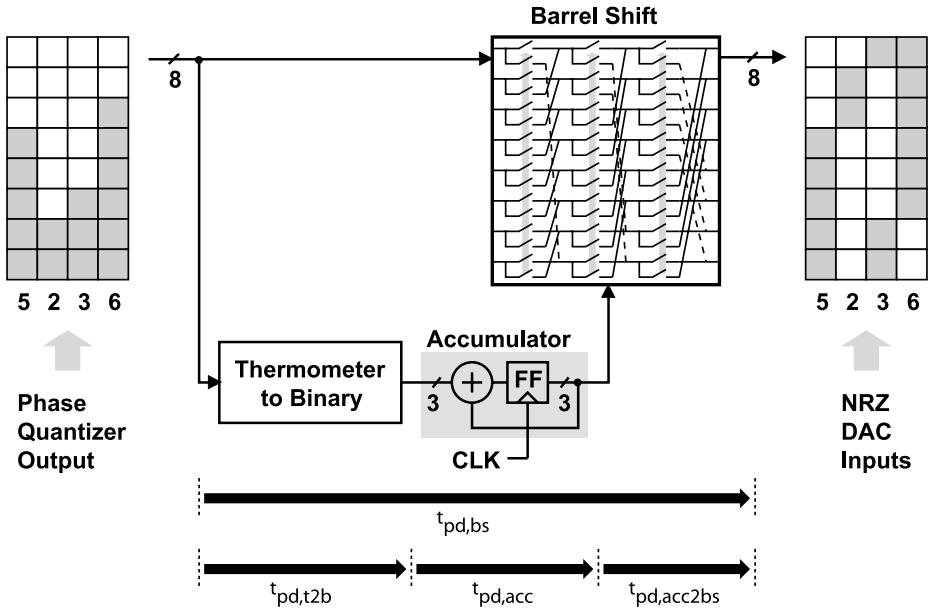


Figure 1-21: proposed parallel implementation of the DWA algorithm.

is equal to the modulo-2^N accumulated sum of the previous quantizer output values. Consequently, the DEM can be split into two parallel paths, one which shifts the input thermometer code, and the other which records the previous quantizer value and updates the pointer. The timing constraint for the path through the barrel shift is then:

$$t_{pd,bs} < T - t_{clk2q} - t_{pd,det} - t_{sh,dac} \tag{1.2}$$

where $t_{pd,bs}$ is the propagation delay through the barrel shift. Note that the accumulator to barrel shift propagation delay ($t_{pd,acc2bs}$) is approximately the same as the phase quantizer clock-to-Q delay ($t_{pd,clk2q}$), and therefore does not add to the propagation delay through the barrel shift. The timing constraint for the path through the thermometer to binary decoder and accumulator is then:

$$t_{pd,t2b} + t_{pd,acc} < T - t_{clk2q} - t_{pd,det} \tag{1.3}$$

As will be seen later in a later chapter, the second of the two timing constraints forms the bottleneck in the DWA. Nevertheless, the implementation significantly relaxes

timing constraints, making DWA at such high speeds possible.

Recall from the previous section that the use of a VCO-based quantizer enables the loop delay compensating DAC to also have it's unit element mismatch noise shaped by the phase-to-frequency post quantization differentiation (see implicit DWA in Figure 1-19). The value of this inherent DWA can be greater appreciated in light of the significant effort involved in performing DWA for the two other feedback DAC's within a sample period. Note that explicitly performing DWA on the delay compensating DAC in the conventional architecture of Figure 1-15 would require the algorithm to finish processing in less than half a sample period—an extremely challenging feat using any known DWA implementation unless the ADC clock frequency were halved or the number of DAC/quantizer bits reduced.

1.6 Thesis Outline

The remainder of this thesis delves into the implementation details of the proposed ADC. Chapter 2 focuses on architectural verification through behavioral simulation, and rigorously explores various non-idealities that impact the overall converter performance. Chapter 3 highlights the major circuit blocks of the ADC—opamps, DAC's, VCO-quantizer, DWA logic—and discusses the power-speed-noise trade-offs that motivated the adoption of the implemented circuit topologies. Measured results are presented in Chapter 4, and validate not only the proposed architecture, but also the application of VCO-based ADC's in high performance applications. Chapter 5 proposes further improvements to the architecture, and provides insight on how the ADC performance will be affected by technology scaling. The thesis concludes in Chapter 6 with an overview of accomplishments and contributions.

Chapter 2

Behavioral Simulation

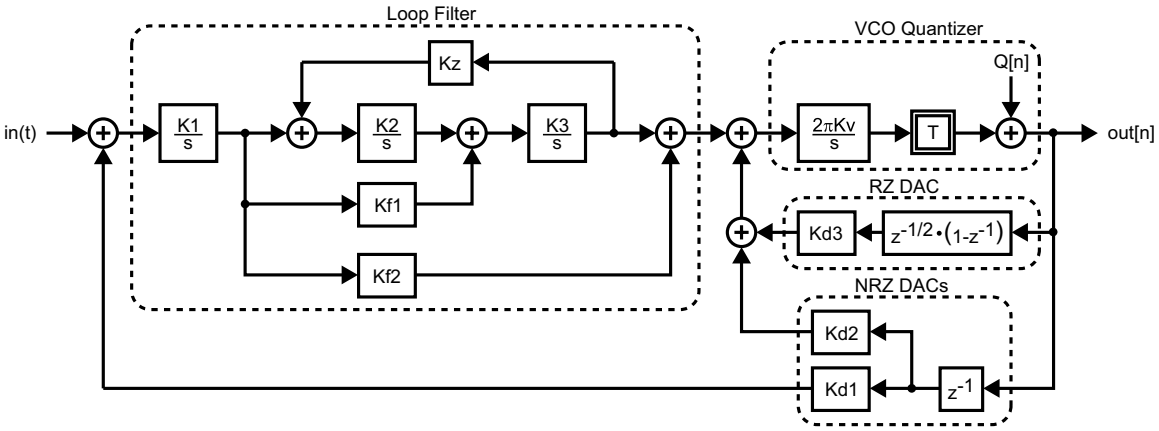


Figure 2-1: block diagram behavioral model of the proposed 4^{th}-order CT $\Delta\Sigma$ ADC leveraging the voltage-to-phase VCO-based integrator and quantizer.

Due to the complexity of mixed-signal systems, architectural design and evaluation are often cumbersome and time-consuming tasks to accomplish at the transistor level. Fortunately, behavioral simulators offer an alternate means of evaluating system architectures with simulation times that are orders of magnitude shorter, and can produce results that closely match those of a transistor level simulator when critical non-idealities are correctly modeled. The architectural analysis of the proposed ADC is accomplished through the use of CppSim [48], a C++ behavioral simulator that enforces a fixed simulation time-step and area conservation, enabling high-accuracy simulations of noise floors, jitter, SNR, and other quantities highly sensitive to timing.

CppSim as well as the behavioral model discussed in this thesis can be downloaded for free on the Internet [47].

This chapter will build on the simple block-diagram behavioral model of the proposed ADC (repeated in Figure 2-1 for clarity) by incrementally adding non-idealities to the model. This way, the impact of mismatches, noise, and other error sources found in real circuits can be studied both independently and collectively, elucidating which non-idealities limit the proposed converter's performance. At the same time, this methodical process of introducing real circuit non-idealities will eventually produce a behavioral model that can accurately predict the converter's actual measured performance.

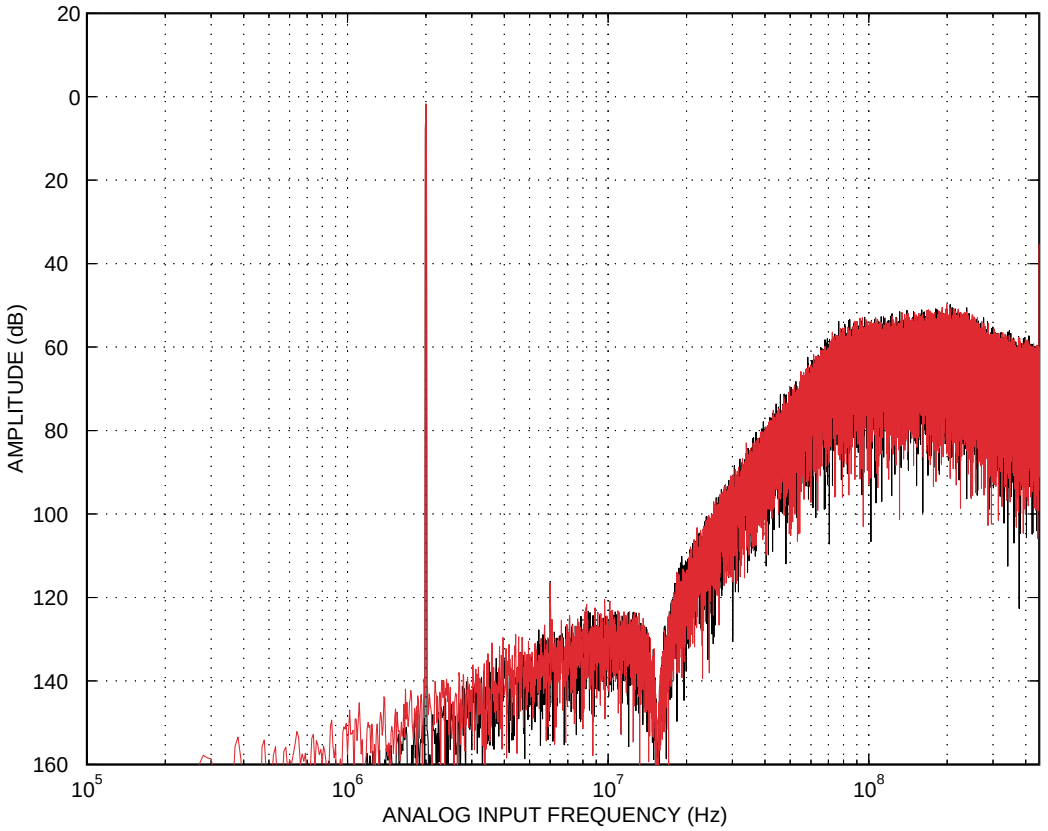


Figure 2-2: 100,000 point FFT's generated from behavioral simulation of the proposed ADC architecture assuming a linear K_v (dark) and non-linear K_v (light).

Behavioral simulation results in the introduction have already shown that a simple 1^{st}-order CT $\Delta\Sigma$ VCO-based ADC is robust to K_v non-linearity when the VCO is used as a voltage-to-phase integrator and quantizer. The same holds true when the VCO-

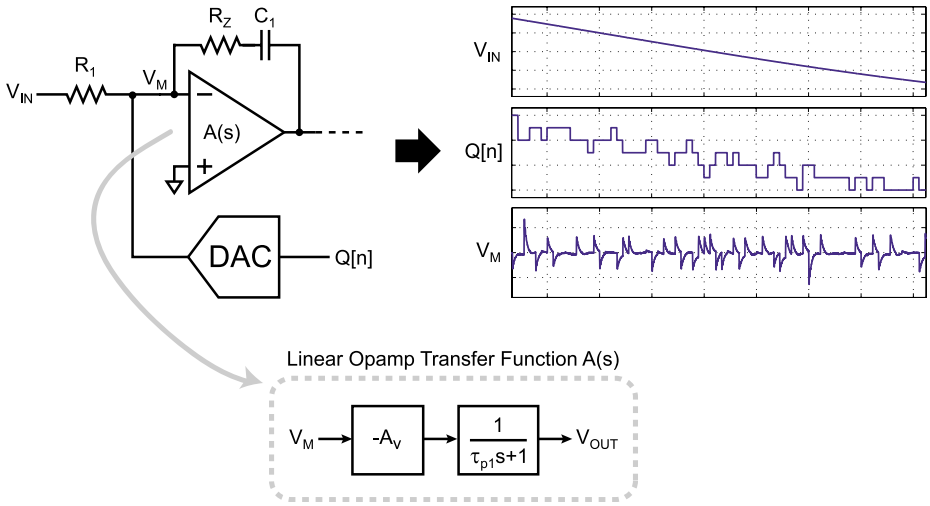


Figure 2-3: quantization noise appearing at the input of the first opamp-integrator, where the opamp is characterized as a linear transfer function A(s). One possible and very simple realization for A(s) consists of a linear gain and a dominant pole.

based integrator and quantizer is included in the behavioral model of the proposed 4^{th} CT $\Delta\Sigma$ ADC of Figure 2-1. As the FFT overlay in Figure 2-2 shows, the inclusion of VCO K_v non-linearity (light) has no observable impact on the simulated spectrum when compared to the ideal case of a perfectly linear VCO K_v (dark). Indeed, the ideal simulated SNR/SNDR of 95.7/95.5 dB degrades by less than 1 dB to 95.0/94.9 dB when non-linearity is included in the behavioral model.

The remainder of this chapter will investigate other key non-idealities that ultimately limit the performance of the proposed ADC, with particular emphasis placed on the unit-element mismatch and ISI of the main feedback DAC, which have the greatest impact on the converter's resolution. A tabulated summary of these behavioral simulation results will be shown at the conclusion of this chapter.

2.1 Amplifier Finite Gain-Bandwidth

Intuitively, the impact of finite amplifier gain and bandwidth can be understood when considering the signals stimulating the input of the first opamp of the loop filter (see Figure 2-3). Here, the opamp is abstracted as a linear transfer function A(s), and one possible realization of A(s) shown in the dashed box (a simple gain

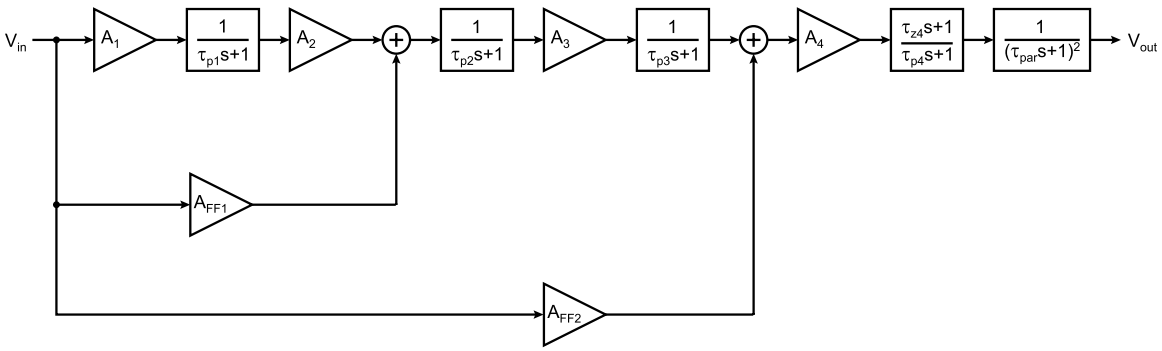


Figure 2-4: the nested-Miller amplifier behavioral model that forms the linear opamp transfer function A(s).

and a dominant pole). Quantization noise resulting from the difference between the input signal and the main feedback DAC output signal perturbs the input nodes of the opamp. The opamp's negative feedback acts to cancel out the perturbation to re-establish a virtual ground condition. However, the finite gain and settling time of the amplifier will result in some residual quantization noise remaining at the opamp input at the end of a given sample period. This error not only causes incomplete suppression of the inband quantization noise, but also can create inband distortion tones due to the signal dependency of the residual quantization noise itself.

The degree to which the converter's performance will be affected by these non-idealities will depend on the opamp's open-loop characteristics, which will in turn depend on the implemented topology. Prior work [36] has demonstrated that the multi-stage nested Miller amplifier enables superior gain-bandwidth performance when compared to the standard 2-stage Miller amplifier. A simple linear block-diagram model of a 4-stage Nested Miller amplifier that describes the linear opamp transfer function A(s) is shown in Figure 2-4. Here, a cascade of 4 gain stages enables a high DC gain while 2 feed-forward stages ensure overall amplifier stability. Note that the settling characteristics of the amplifier are primarily determined by the cascade of the second feed-forward gain stage (A_{FF2}) and the output gain stage (A_4), which collectively resemble a 2-stage Miller amplifier. Thus, the nested Miller topology provides similar unity-gain bandwidths as a 2-stage Miller, but enables higher gain over a greater portion of the amplifier's bandwidth, as illustrated in the bode plots of Figure 2-5.

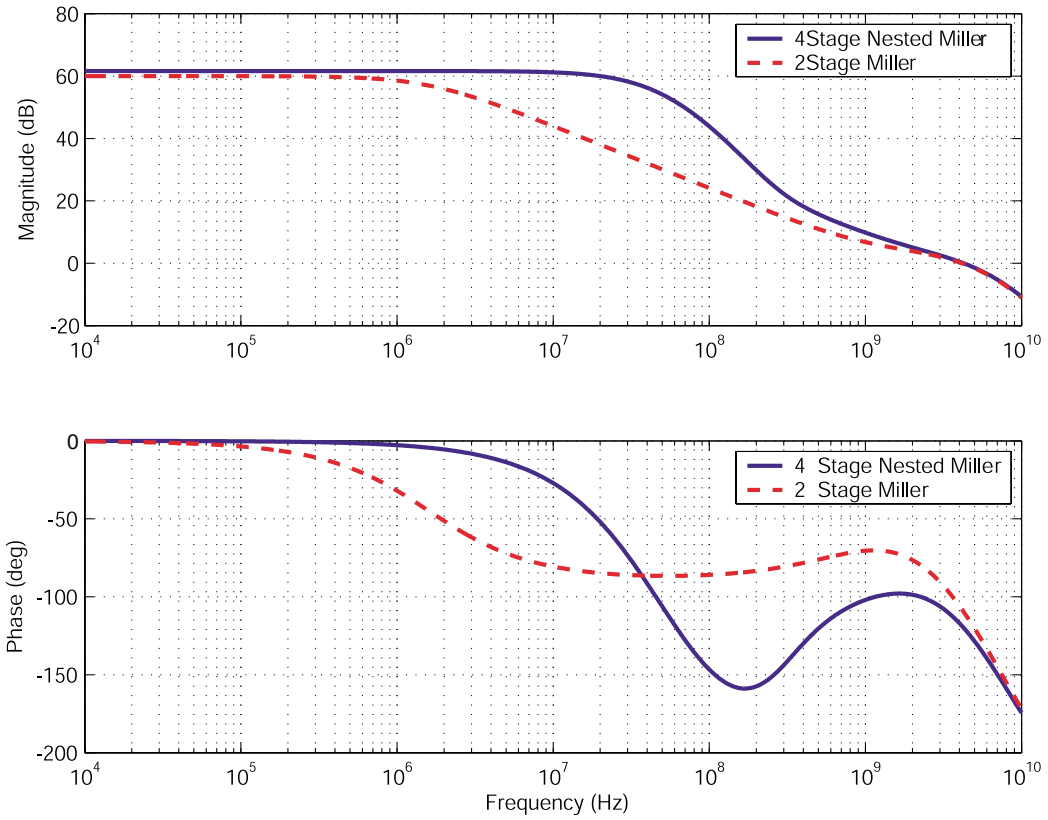


Figure 2-5: bode plot of the open loop characteristics of a 4-stage nested Miller amplifier (solid) and the standard 2-stage Miller amplifier (dashed). Both amplifiers are designed to have a DC gain of 60 dB and a unity gain frequency of 4 GHz.

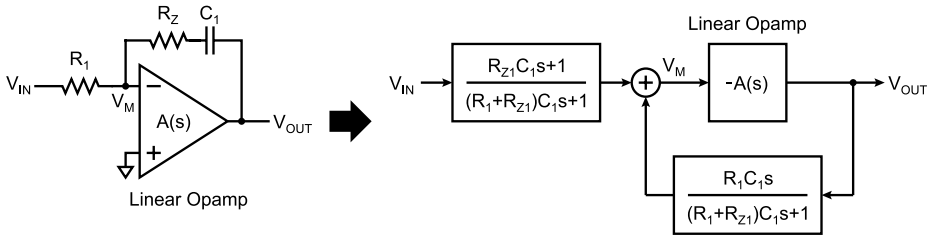


Figure 2-6: the integrator behavioral model with linear opamp transfer function A(s) and linear feedback network transfer functions.

For these reasons, a 4-stage nested Miller amplifier was implemented for the proposed ADC.

To quantify the impact of amplifier finite gain and bandwidth on the proposed ADC architecture, the 4-stage nested Miller linear opamp model is embedded in an integrator behavioral model. As shown in Figure 2-6, the integrator behavioral model comprises the linear opamp transfer function A(s), as well as the linear transfer functions describing the feedback network. Figure 2-7 shows the proposed ADC's simulated SNR/SNDR for varying DC gains and unity-gain bandwidths. As can be seen from the plot, the finite amplifier gain and bandwidth result in a minor SNR degradation that is no more than 3 dB lower than the ideal SNR of 95 dB. However, the impact of finite gain on the simulated SNDR is far more serious. When the amplifier DC gain is 40 dB, the simulated SNDR drops by more than 6 dB relative to the ideal case due to inband distortion tones arising from the signal dependency of the residual error signal. Note however, that the simulated SNDR achieved assuming amplifiers with 60 dB and 80 dB of DC gain differs only slightly from the ideal SNDR of 94.9 dB. Consequently, it will be assumed from this point forward that the amplifier is designed to achieve a DC gain of at least 60 dB.

The impact on SNR and SNDR caused by finite amplifier DC gain can also be observed in the overlay of two 100,000 point FFT's of Figure 2-8. Here, the proposed architecture is simulated assuming amplifiers with 4 GHz unity gain bandwidths, and DC gains of 40 dB (light) and 80 dB (dark). As can be seen from the plot, the lower DC gain not only introduces a strong second harmonic due to the signal dependency of the residual quantization error, but also fills in the nulls of the quantization noise

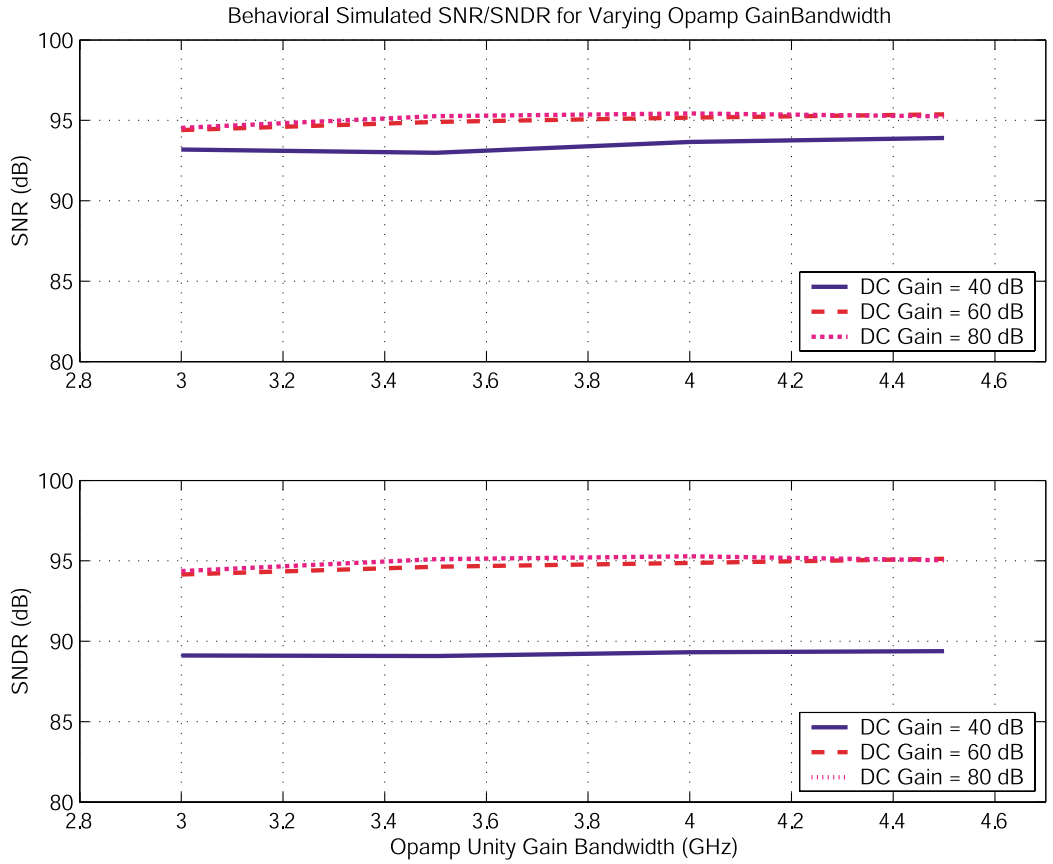


Figure 2-7: behavioral simulated SNR/SNDR of the proposed ADC for various opamp DC gain and unity-gain bandwidths. Only quantization noise and finite gain-bandwidths are considered in these simulations.

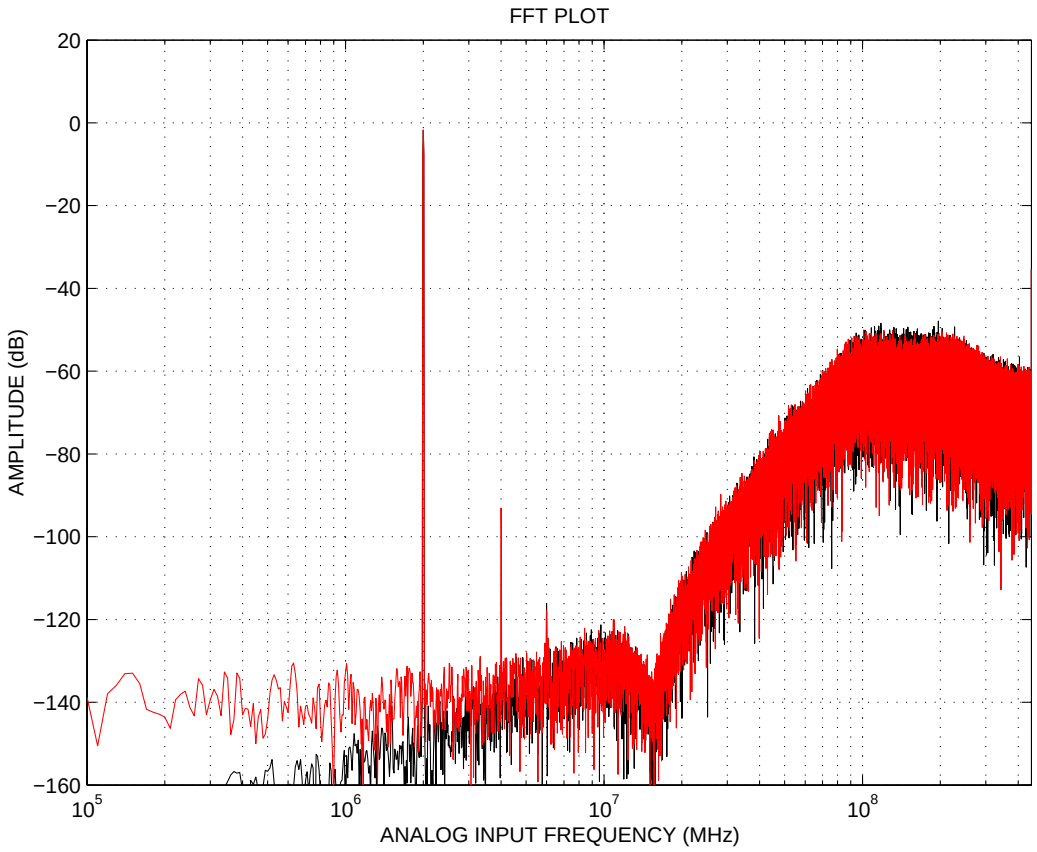


Figure 2-8: 100,000 point FFT's generated from behavioral simulation of the proposed ADC architecture assuming amplifiers with 4 GHz unity-gain bandwidths, and DC gains of 80 dB (dark) and 40 dB (light).

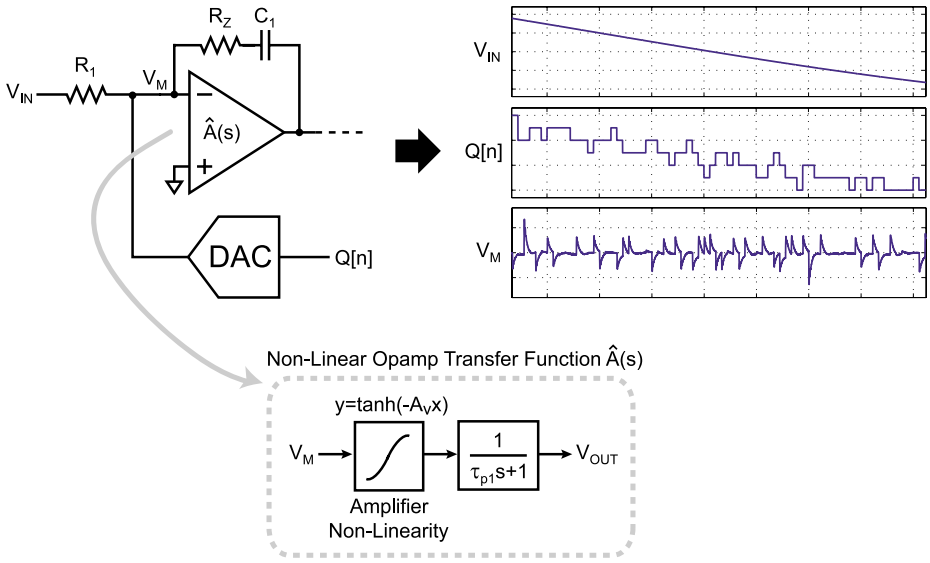


Figure 2-9: quantization noise appearing at the input of the first opamp-integrator, where the opamp is characterized as a non-linear transfer function $\hat{A}(s)$.

profile at DC and at 15.5 MHz.

2.2 Amplifier Non-Linearity

Although finite amplifier DC gain had a very noticeable impact on the simulated SNDR of the proposed ADC, the finite unity-gain bandwidth appeared to have a much less pronounced effect. Analyzing the simulated results from Figure 2-7 might then lead to the incorrect assumption that an amplifier unity-gain bandwidth as low as 3 times the ADC sample rate of 900 MHz is sufficient to achieve the desired performance. However, as will be discussed in this section, the presence of opamp non-linearity will necessitate a much more stringent requirement on the amplifier unity-gain bandwidth.

The effect of amplifier non-linearity as well as its connection to amplifier settling time can be understood intuitively when the signals stimulating the input of a non-linear opamp are considered (see Figure 2-9). As before, quantization noise perturbs the input nodes of the opamp, prompting the amplifier to cancel out the perturbation via its negative feedback network such that the virtual ground condition is re-established. This time, however, the quantization noise will also encounter

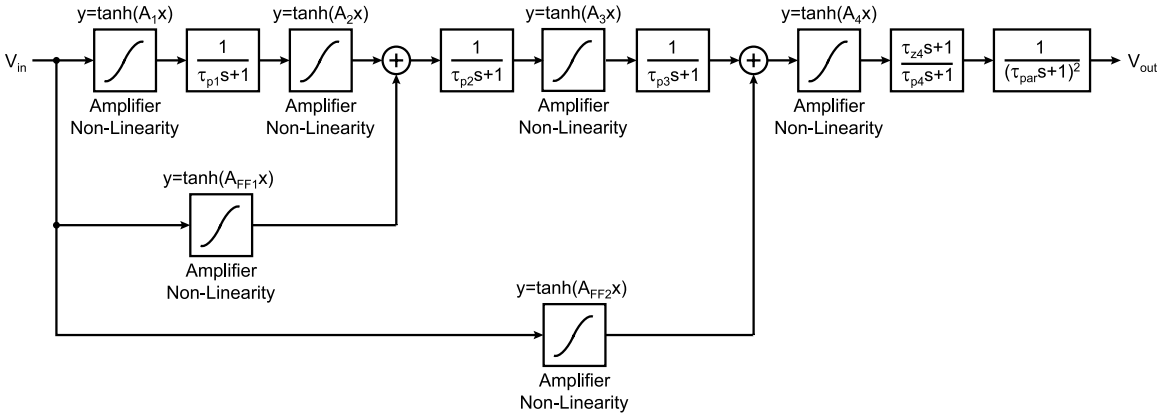


Figure 2-10: non-linear opamp model for the nested-Miller amplifier.

the opamp's non-linear gain characteristic, causing the amplifier to settle in a non-linear fashion, and resulting in inband quantization noise folding. While the amount of quantization noise folding depends on the size of the perturbation as well as the characteristics of the non-linearity, it is also strongly related to the settling speed of the amplifier. A faster amplifier will act to restore the virtual ground condition more quickly, which effectively reduces the time that the quantization noise encounters the non-linearity. This in turn reduces the non-linear settling transient that is integrated by subsequent integration stages in the loop filter, resulting in less quantization noise folding.

To quantify the impact of opamp non-linearity in behavioral simulation, the linear opamp model developed in the previous section must be modified to include the specific characteristics of the non-linearity. Fortunately, circuit simulations reveal that the non-linearity of most differential-pair based gain stages resembles a $\tanh(x)$ function, making this task relatively easy. The behavioral model for the non-linear opamp transfer function, $\hat{\mathrm{A}}(\mathrm{s})$, is shown in Figure 2-10. Figure 2-11 shows the overall integrator behavioral model, which comprises a non-linear opamp transfer function $\hat{\mathrm{A}}(\mathrm{s})$, and linear transfer functions characterizing the feedback network.

Despite the simplicity of these models, significant insight can be obtained from the behavioral simulation results, especially as it pertains to the unity-gain bandwidth requirements for the opamps. Figure 2-12 plots the behavioral simulated SNR/SNDR of the proposed ADC architecture for different opamp unity-gain frequencies, with

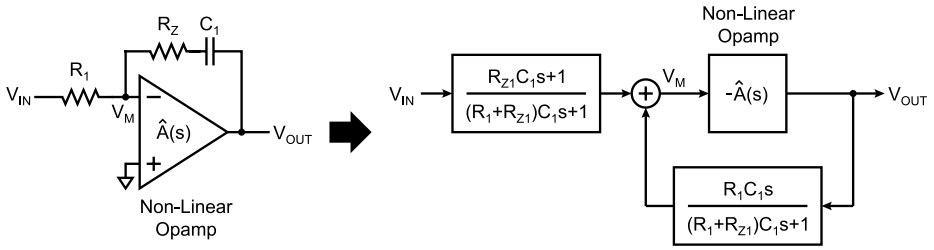


Figure 2-11: the integrator behavioral model with non-linear opamp transfer function $\hat{A}(s)$ and linear feedback network transfer functions.

opamp non-linearity included in the behavioral model. As can be seen from the figure, the SNR/SNDR degrades steadily when the unity-gain bandwidth is decreased from 4.5 GHz down to 2.5 GHz. Indeed, to achieve close to 14 ENOB performance, an opamp with greater than 3.5 GHz unity-gain bandwidth must be designed. Henceforth, it will be assumed that the opamps are designed to achieve a 4 GHz unity-gain frequency.

An overlay of two 100,000 point FFT's generated from simulations of the proposed architecture assuming ideal amplifiers (dark) and the non-linear gain-bandwidth limited opamp model (light) is shown in Figure 2-13. As the plot shows, quantization noise folding effectively fills-in the deep nulls of the noise transfer function, creating an inband noise floor, and resulting in an SNR/SNDR of 88.3/87.7 dB.

2.3 Finite DAC Impedance

As discussed in the previous section, the opamp's finite gain-bandwidth limitation will result in quantization noise appearing at the input node of the amplifier. Unfortunately, any movement at this node will modulate the drain-to-source voltages of the MOSFET's comprising the DAC unit elements, resulting in a parasitic current due to the DAC's finite output resistance. Furthermore, this output resistance will vary according to the applied DAC code, resulting in a parasitic current that varies in a signal-dependent manner.

To quantify the impact of the DAC's finite output resistance on the converter's SNR/SNDR in simulation, the DAC behavioral model shown in Figure 2-14 was cre-

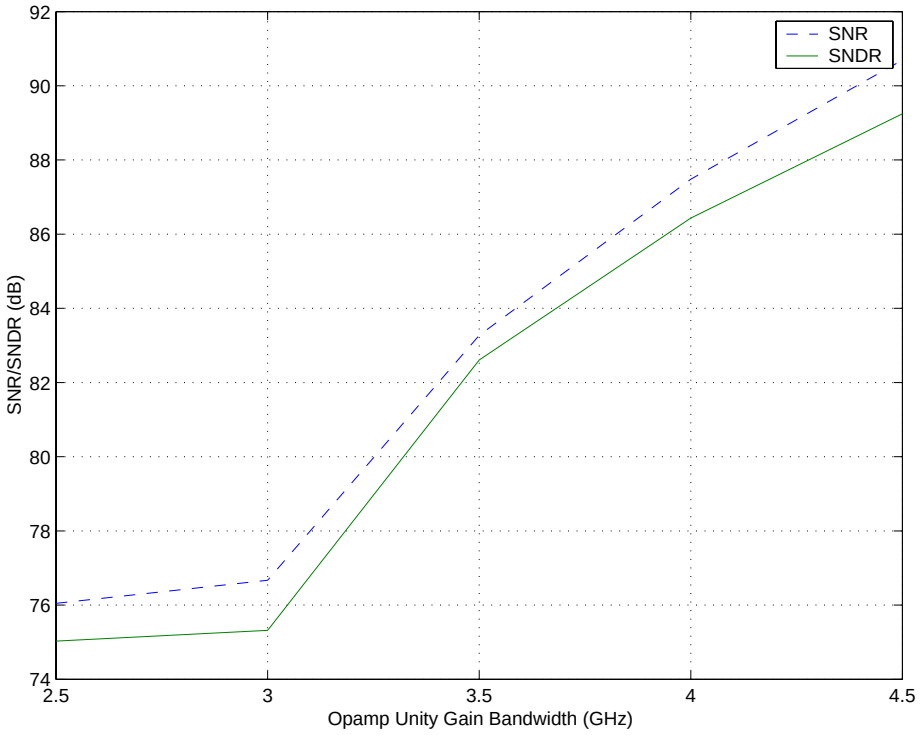


Figure 2-12: behavioral simulated SNR/SNDR of the proposed ADC assuming non-linear opamps with a DC gain of 60 dB, and various unity-gain bandwidths. Only quantization noise and amplifier non-linearity and finite gain-bandwidth are considered in the behavioral simulations.

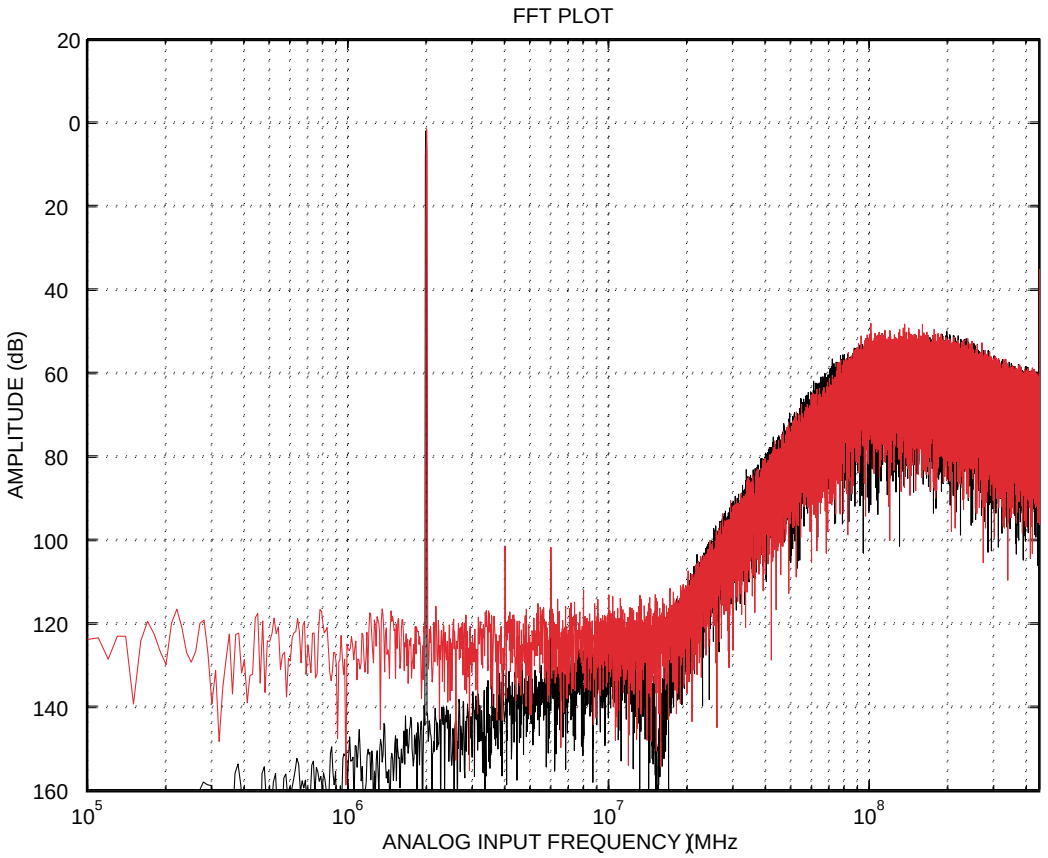


Figure 2-13: 100,000 point FFT's generated from behavioral simulation of the proposed ADC architecture assuming ideal amplifiers (dark) and non-linear gain-bandwidth limited amplifiers (light).

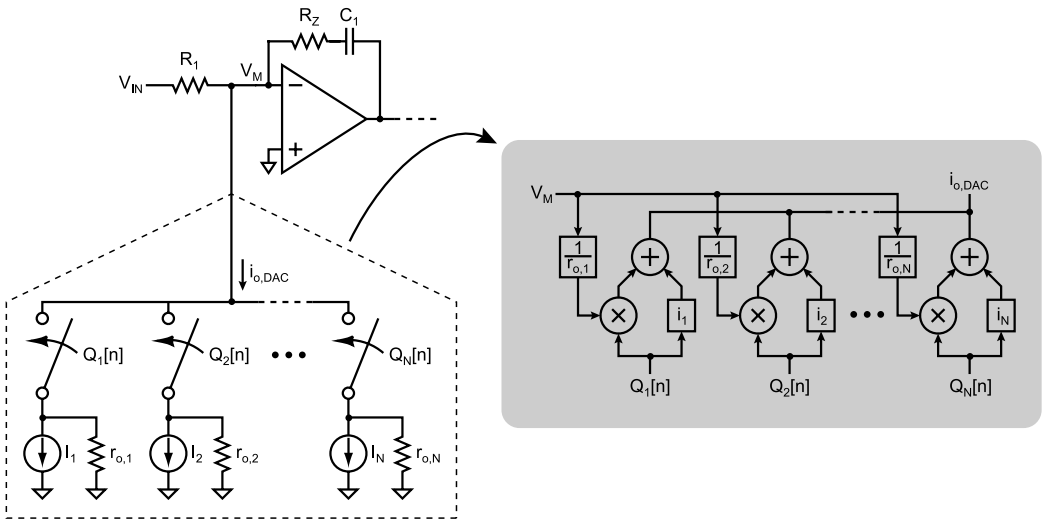


Figure 2-14: the main feedback DAC behavioral model, which includes the effect of finite output resistance.

ated. Note that a single-ended version is shown for simplicity, while fully differential amplifier and DAC topologies were actually implemented. Here, an array of conductances are used to describe the finite resistances of the unit-elements, and are either enabled or disabled to mimic the code dependency of the output resistance.

A plot detailing the simulated SNR/SNDR for a range of DAC output resistances is shown in Figure 2-15. From these results, it is clear that the effect of finite resistance can largely be ignored when a minimum unit-element output resistance of 30 kΩ is achieved. Indeed, quantization noise-folding caused by amplifier non-linearity and gain-bandwidth limitations appear to mask the errors caused by DAC output resistances when this minimum resistance threshold is exceeded.

An overlay of two 100,000 point FFT's generated from simulations of the proposed architecture assuming an infinite DAC output resistance (dark) and a finite DAC output resistance of (70 kΩ) (light) is shown in Figure 2-16. As can be seen from the plots, the inclusion of finite DAC output resistance has a negligible impact on the simulated SNR/SNDR, as the architecture is still able to achieve at least 88 dB for both specifications.

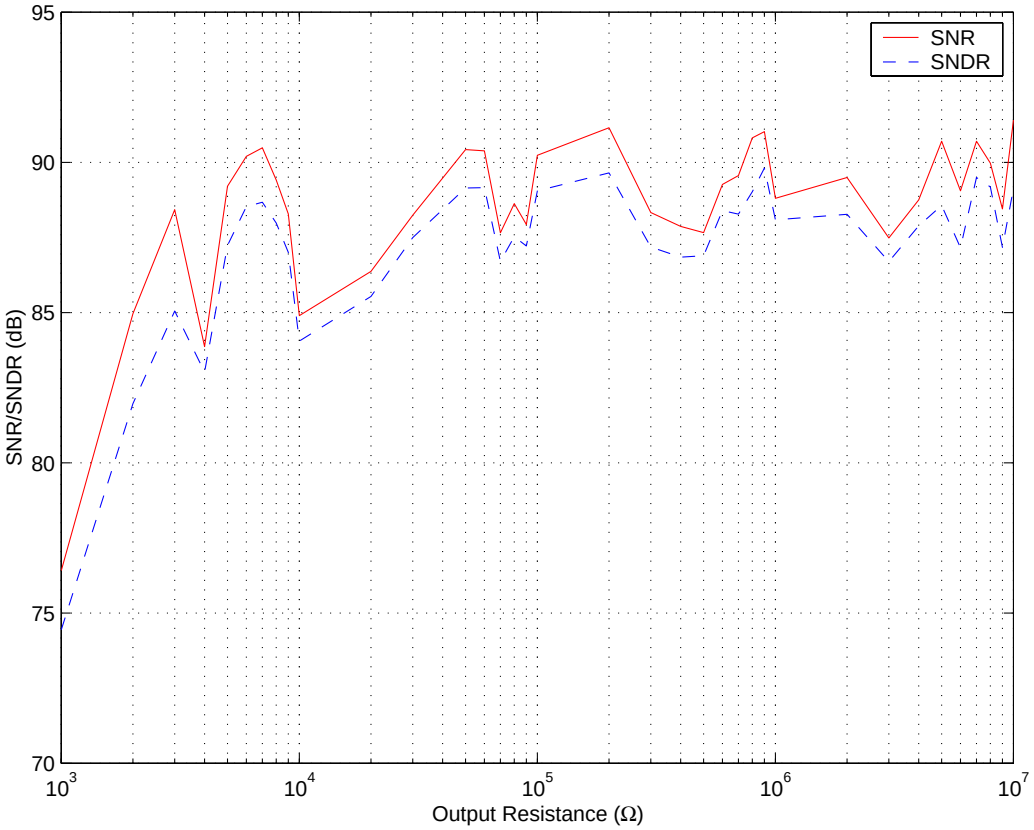


Figure 2-15: impact on SNR/SNDR due to the main feedback DAC's finite output resistance and amplifier non-linearity and finite gain-bandwidth.

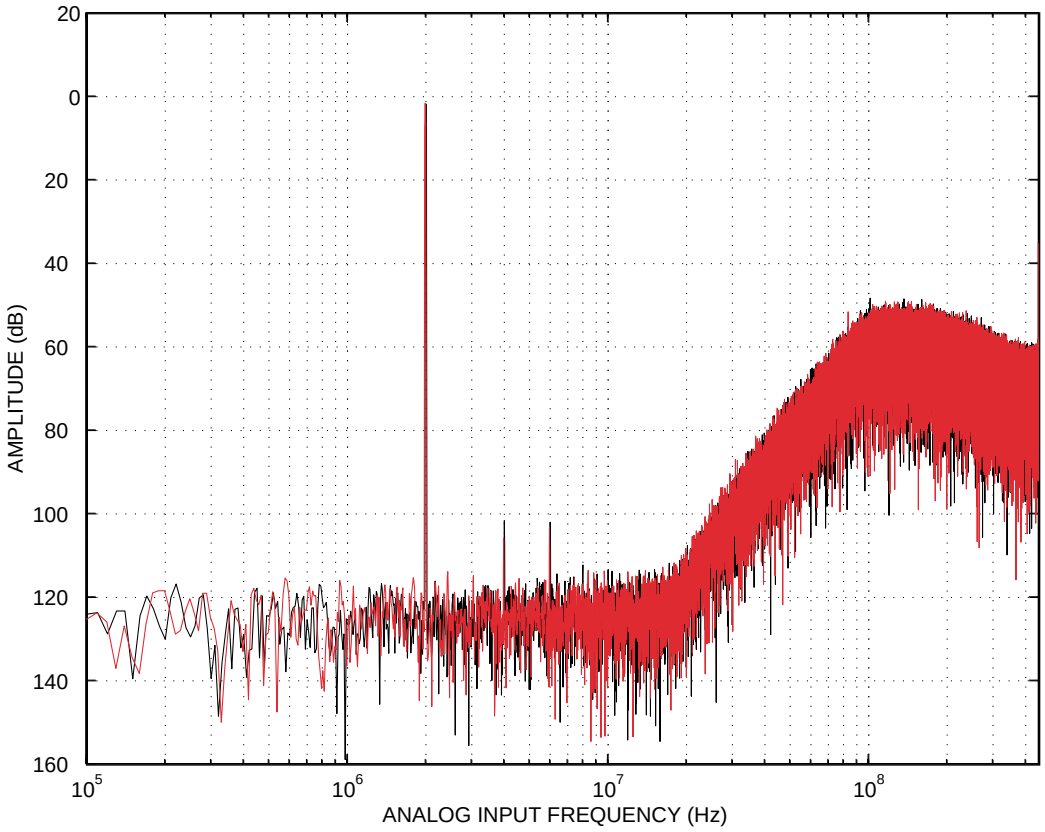


Figure 2-16: 100,000 point FFT's generated from behavioral simulation of the proposed ADC architecture assuming ideal DAC's with infinite output resistance (dark) and a main DAC with an output resistance of 70 kΩ (light).

2.4 Device Noise

In many state-of-the-art data converter designs, device noise establishes the upper limit on achievable SNR. Consequently, the converter resolution ultimately becomes a question of how much power the designer is willing to sacrifice to reduce the device noise to a desired level. In CT $\Delta\Sigma$ ADC's, the device noise primarily originates from the main feedback DAC, the first integrator, and the input resistors.

As the next chapter on circuit design will show, a conservative estimate of all these noise sources given the desired power budget is roughly 5 nV/$\sqrt{Hz}$. To achieve near 14 ENOB resolution then dictates that the full-scale signal be on the order of $2V_{pp,diff}$, resulting in an ideal SNR of 90 dB (14.7 ENOB). Note however, that applying a full-scale input to a $\Delta\Sigma$ ADC can cause saturation in the integrators, resulting in quantization noise-folding. For the proposed topology, behavioral simulations in CppSim show that the maximum input signal possible is -3 dBFS, resulting in a peak ideal SNR of 87 dB. While the SNR appears to offer solid 14 ENOB performance, in reality the thermal noise will add to the quantization noise floor due to opamp non-linearity and finite gain-bandwidth. Consequently, the ADC architecture must be simulated to obtain a more accurate estimate of the SNR/SNDR.

Histograms generated by running 50 Monte-Carlo simulations of the proposed architecture are shown in Figure 2-17. Here, the average SNR/SNDR of 85.1/84.2 dB suggests that the noise floor is effectively 2 dB higher than the thermal noise-limited case due to inband quantization noise folding from the amplifier non-linearity and finite gain-bandwidth. Note however, that additional noise sources (particularly static and dynamic mismatch errors from the main feedback DAC) will add to this noise floor, further degrading SNR/SNDR as will be discussed later.

2.5 VCO Unit Element Mismatch

Mismatches in the delay stages comprising the ring oscillator result in a net accumulated phase error at the end of each sampling period. Fortunately, these errors will

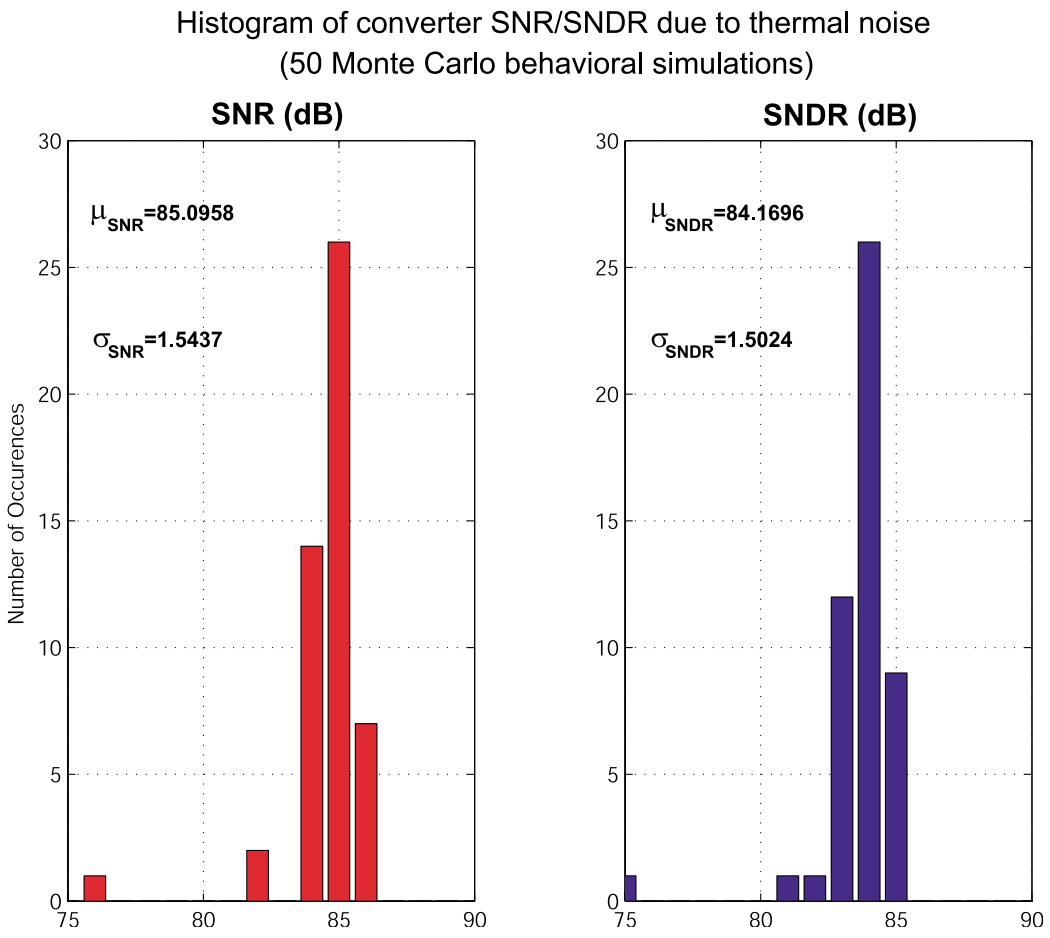


Figure 2-17: histograms of the behavioral simulated SNR/SNDR of the proposed ADC architecture assuming a thermal noise density of 5 nV/$\sqrt{Hz}$. Data obtained by running 50 Monte-Carlo simulations of the proposed architecture, and changing the seed of the random noise generator.

be suppressed by the gain of the preceding loop filter, and should result in a small degradation of SNDR when referred to the input.

To verify the architecture's robustness to this variation, Figure 2-18 shows the histograms of the SNR/SNDR values assuming a ring-VCO delay mismatch of 1σ = 5%, 7.5%, and 10%. The data was generated by running 50 Monte-Carlos simulations of the proposed architecture for each mismatch deviation. As can be seen from the histograms, even a mismatch as large as $1\sigma = 10\%$ will result in an average SNR/SNDR of 84.7/83.9 dB, a degradation of less than 0.5 dB. Note that the ring-VCO inverter delay mismatch cannot be easily determined due to its dependence on not only process, but also wiring capacitances. Consequently, this thesis will assume a worst case mismatch of 10% in all subsequent analysis.

2.6 Main NRZ DAC Unit Element Mismatch

While mismatches in the second and third feedback DAC unit elements will be shaped by the high gain of the preceding loop filter, mismatches in the main feedback DAC unit elements appear directly at the input of the ADC. Consequently, the main feedback DAC must perform at least as well as the entire converter, a very challenging requirement. Fortunately, data-directed dynamic element matching (DEM) algorithms have been developed to shape DAC unit-element mismatch errors, enabling high performance compared to prior scrambling algorithms that relied on random selection of DAC unit-elements [12].

For the proposed ADC, the dynamic weighted averaging (DWA) algorithm [5] was chosen over other data-directed selection algorithms (such as the butterfly [1] and tree DEM [18]) for its superior inband mismatch shaping ability. Nevertheless, behavioral simulations reveal that even this shaped DAC mismatch has a severe impact on converter SNDR. As shown in the histograms of Figure 2-19, even a unit-element mismatch of just 1.5% causes the average SNDR to degrade by 2 dB. While careful design and layout techniques can enable unit-element current source matching of less than 1%, an estimate of 1% will nevertheless be assumed for the remainder of this

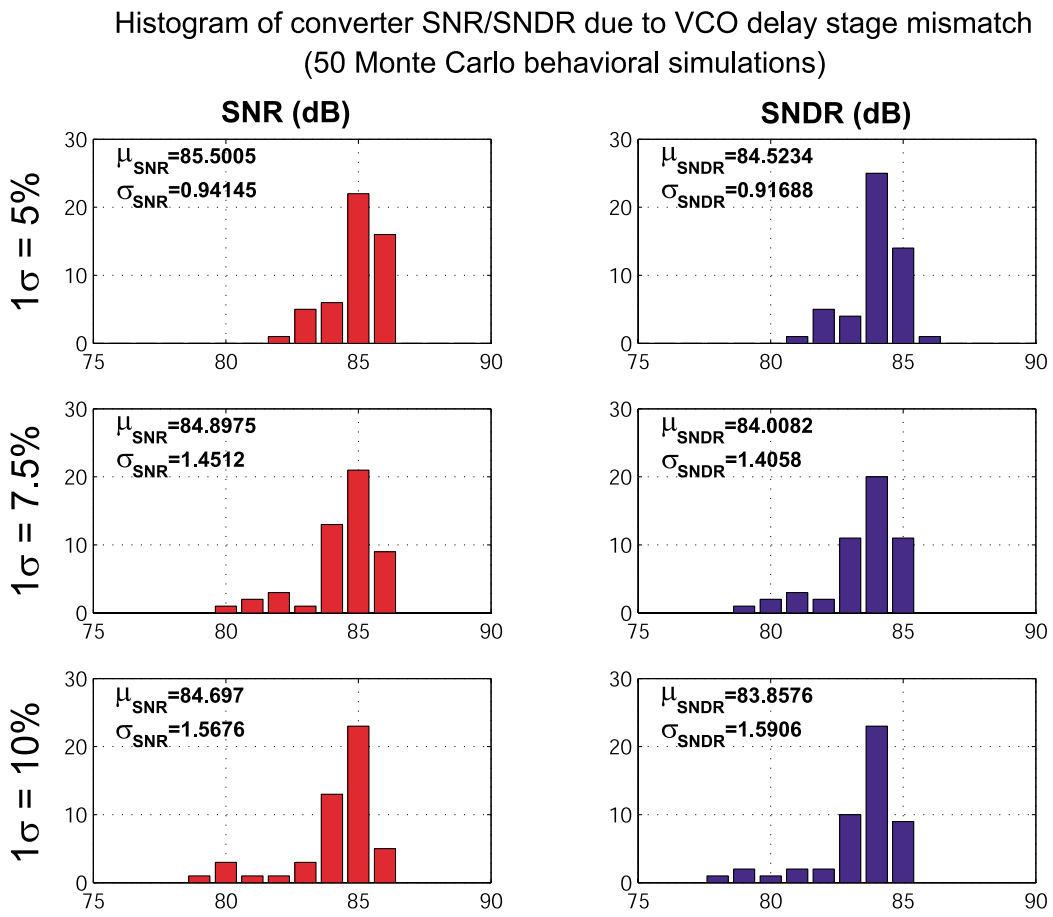


Figure 2-18: histogram of the behavioral simulated SNR/SNDR of the proposed ADC architecture assuming a 15-stage ring-VCO with delay stage mismatches of $1\sigma = 5\%$, 7.5%, and 10%. Data obtained by running 50 Monte-Carlo simulations of the proposed architecture for each mismatch deviation.

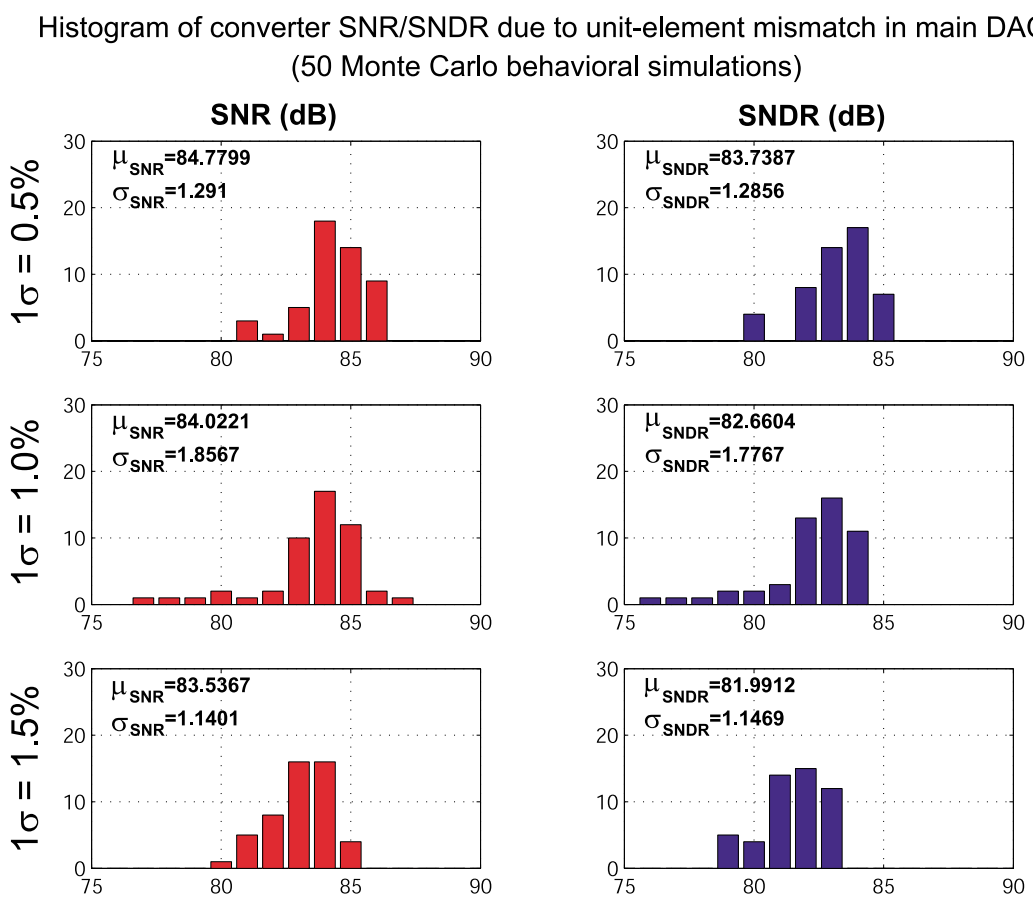


Figure 2-19: histogram of the behavioral simulated SNR/SNDR of the proposed ADC architecture for DAC unit-element mismatches of $1\sigma = 0.5\%$, 1.0%, and 1.5%. Data generated by running 50 Monte-Carlo simulations of the proposed architecture for each mismatch deviation.

thesis. With this assumption, unit-element mismatch in the main DAC would result in an average SNR/SNDR of 84.0/82.7 dB.

2.7 Main NRZ DAC Inter-Symbol Interference (ISI)

In some sense, the term dynamic element matching (DEM) is a misnomer in that its purpose is to shape a static error, namely mismatches in the DC current values of the unit elements in a current-source DAC topology. However, such topologies do encounter a real dynamic error during switching transients, a phenomenon known as inter-symbol interference (ISI). ISI occurs when the unit elements have mismatched output current transients during switching. The mismatch itself can be caused by a number of factors, but is typically due to unequal rising/falling switching time constants, charge injection, and parasitic clock/data feedthrough. When ISI exhibits any code dependency (as is the case for an NRZ DAC), it will cause distortion tones in the ADC output spectrum, degrading the overall converter SNDR. At the same time, these tones cannot be scrambled and shaped by the DEM. As shown in Figure 2-20, although a DWA sequence is inputted to the DAC, the transient mismatches and transition densities still exhibit a code dependency when the DAC code exceeds half of full scale since all selected unit elements will not experience a switching transient.

A common solution to DAC ISI is to adopt a return-to-zero (RZ) DAC structure since all the DAC unit elements will transition once every sample period, effectively breaking any code dependent switching errors. Unfortunately, an RZ DAC can be disadvantageous due to its heightened sensitivity to clock jitter [64], as well as its need for a higher power opamp that can linearly settle to the large output current pulses generated by the DAC structure. At the same time, the RZ DAC signal itself has effectively twice the bandwidth of its NRZ counterpart, requiring higher power DAC switch buffers. For these reasons, an NRZ DAC implementation was chosen.

The impact of ISI on the NRZ DAC can be easily quantified through behavioral simulation. The behavioral model for the NRZ DAC is shown in Figures 2-21(a) and 2-21(b), and comprises N-sets of 4 filters to describe the different rise/fall transients

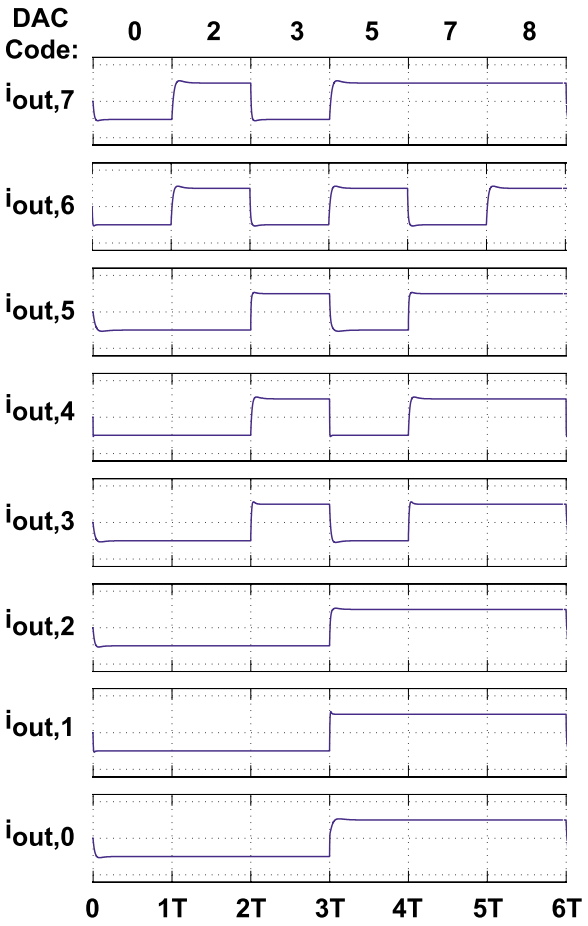


Figure 2-20: behavioral simulated waveforms of an NRZ DAC with 8 unit elements driven by a DWA sequence and illustrating the signal dependency of the transient mismatches and transition densities (ISI).

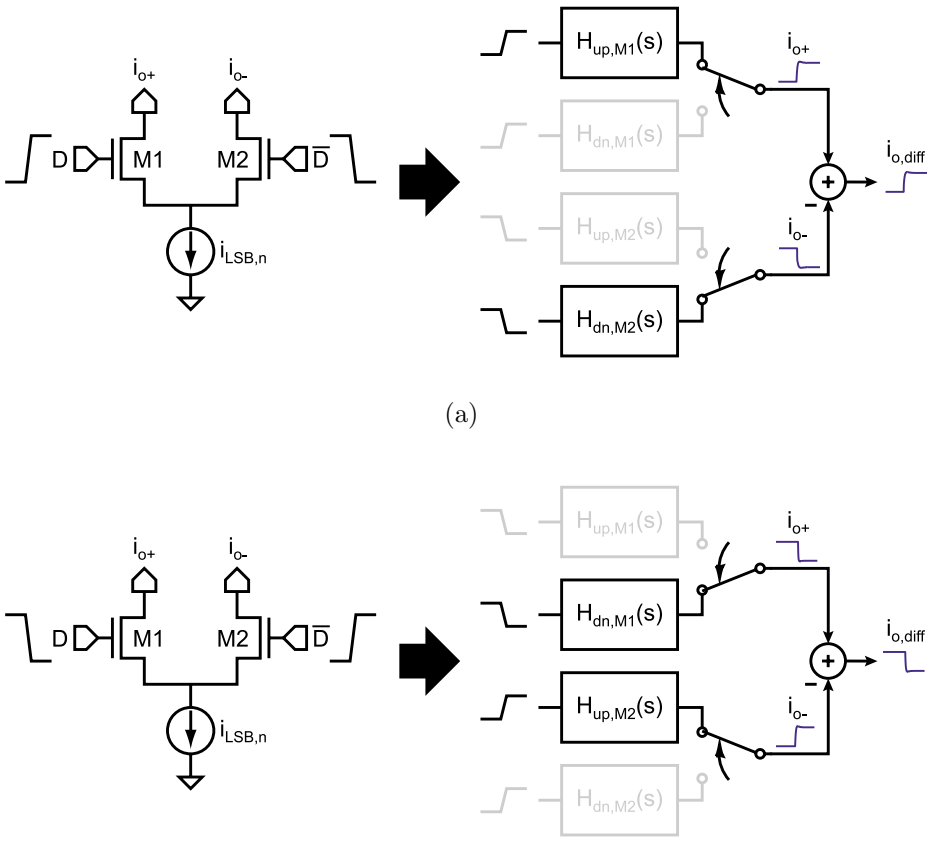


Figure 2-21: ISI model for one unit element of an N-element NRZ DAC depicting a (a) positive switching transient and (b) negative switching transient.

for each switch in a differential pair of an N-element current-steering DAC. While all filters share the same nominal frequency response, the exact pole/zero locations for each filter are purposely varied in a Monte Carlo fashion. Consequently, each filter exhibits different switching transients with variable amounts of peaking (i.e., clock/data feedthrough and charge injection).

As behavioral simulations reveal, ISI degrades converter resolution through its creation of strong distortion tones. Indeed, the histograms of Figure 2-22 show that steadily increasing the mismatch in the switching transients degrades the SNDR by as much as 5 dB compared to the ISI-less case, while the SNR remains relatively constant. Interestingly, the simulation results also reveal another undesirable effect of ISI, namely a wider variation in the range of achievable SNDR. Like the ring-VCO

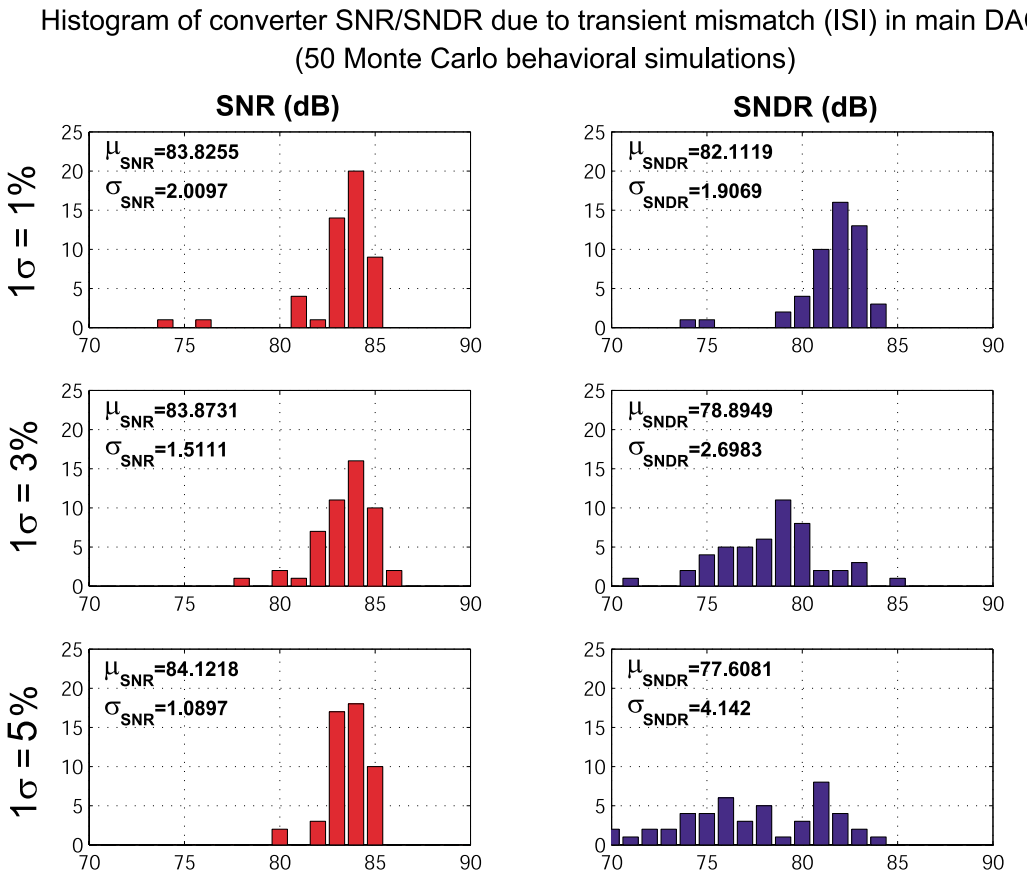


Figure 2-22: histograms of the behavioral simulated SNR/SNDR of the proposed ADC architecture assuming a main NRZ DAC with transient mismatch (ISI) of $1\sigma = 1\%$, 3%, and 5%. Data generated by running 50 Monte-Carlo simulations of the proposed ADC architecture for each mismatch deviation.

delay stages, estimating the transient mismatch is not straightforward as it will vary due to process and layout parasitics. However, the switching devices are much larger than a ring-VCO delay stage in terms of area since they must switch large currents. Consequently, an estimate of 3% will be assumed for this mismatch, resulting in an average SNR/SNDR of 83.9/78.9 dB, almost a 4 dB degradation compared to the ISI-less case.

2.8 Minor-Loop NRZ and RZ DAC Unit-Element Mismatch and ISI

As previously mentioned, errors in the minor-loop DAC's are suppressed by the gain of the loop filter, and will also be shaped by the DWA algorithm. Therefore, the minor-loop DAC's can be made smaller and the architecture can tolerate a higher degree of mismatch and ISI in their unit elements. Histograms of the simulated SNR/SNDR assuming a variety of minor-loop DAC mismatches and ISI are shown in Figure 2-23. Even when using a conservative mismatch estimate of $1\sigma = 5\%$ for both unit-element and transient mismatches, behavioral simulations indicate that the proposed architecture can still achieve an average SNR/SNDR of 83/79 dB. Consequently, it is clear that mismatches in the minor-loop DAC are not as serious as those in the main NRZ feedback DAC thanks to the loop filter gain.

2.9 Clock Jitter

The deleterious effect of clock jitter on the SNDR of CT $\Delta\Sigma$ ADC's has been well documented in the literature [13, 19, 64]. Fortunately, by specifically adopting a multibit NRZ DAC structure, the converter can be made less sensitive to clock jitter than the prototypical single-bit modulator. An expression that estimates the effective SNR given an RMS timing jitter, σ_{jitter}, is shown in Equation 2.1 [64]:

$$SNR_{jitter} = 10\log\left(OSR \cdot \frac{\sigma^2_{I_{DAC,NRZ}}}{\sigma^2_{\Delta I_{DAC,NRZ}}} \frac{T_s^2}{\sigma^2_{jitter}}\right) \tag{2.1}$$

where T_s is the sample period, OSR the oversampling ratio, $\sigma^2_{I_{DAC,NRZ}}$ is the variance of the DAC code, and $\sigma^2_{\Delta I_{DAC,NRZ}}$ is the variance of the first-order difference of the DAC code, $\Delta I_{DAC,NRZ}$. Behavioral simulations in CppSim show that $\sigma^2_{I_{DAC,NRZ}}$ is approximately 14.57 and $\sigma^2_{\Delta I_{DAC,NRZ}}$ is about 0.72. Therefore, given a 900 MHz sample rate and a 1.0 ps RMS clock jitter, the jitter-limited SNR is approximately 90 dB, well below the anticipated device and DAC mismatch noise floor.

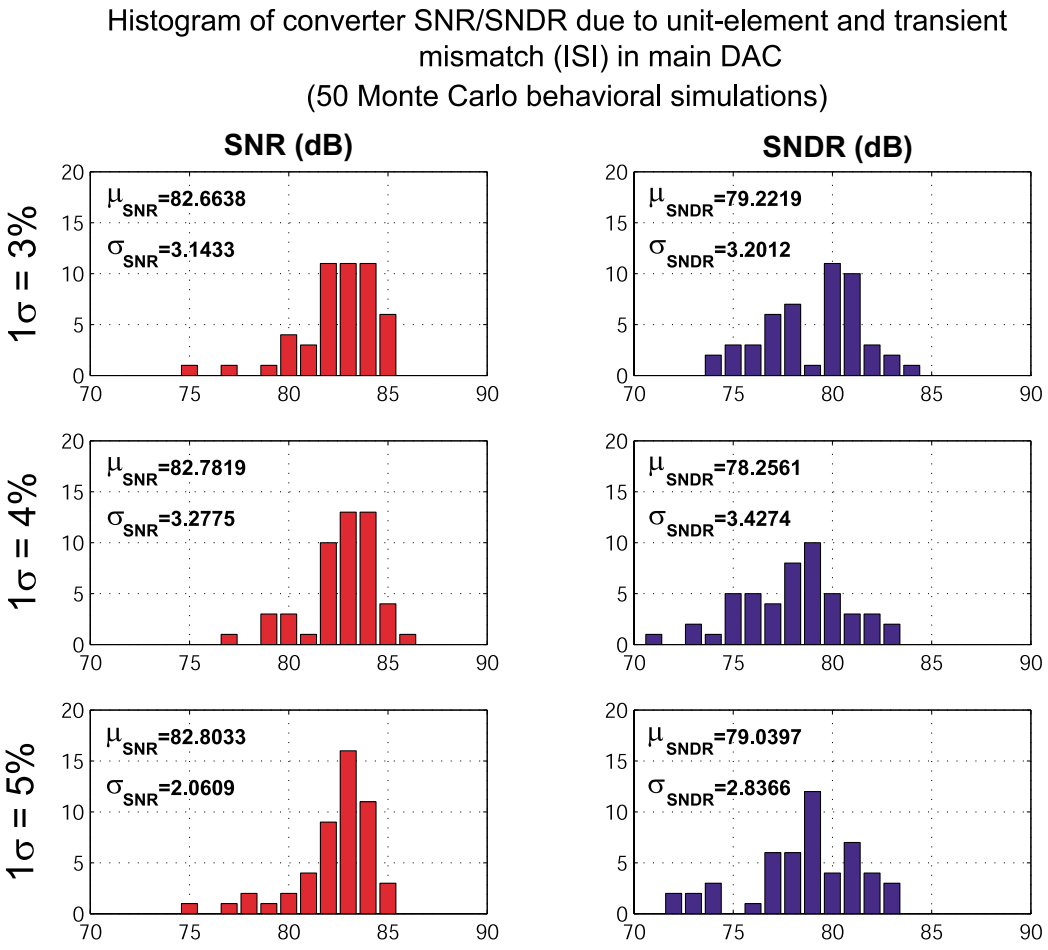


Figure 2-23: histograms of the simulated SNR/SNDR assuming a minor-loop RZ and NRZ DAC's with unit-element and transient mismatches (ISI) of $1\sigma = 3\%$, 4%, and 5%. Data generated by running 50 Monte-Carlo simulations of the proposed ADC architecture for each mismatch deviation.

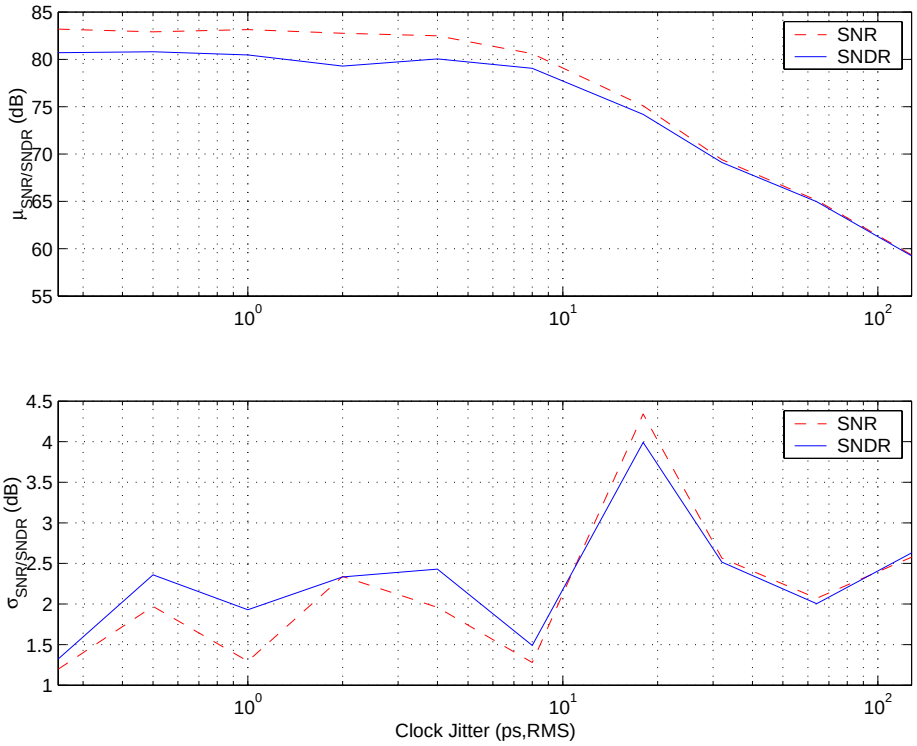


Figure 2-24: average and standard deviation SNR and SNDR for variable amounts of clock jitter, as determined from Monte Carlo behavioral simulations.

To verify the architecture's insensitivity to jitter, the behavioral model is modified to include variable amounts of clock jitter. Figure 2-24 shows the average and standard deviation converter SNR and SNDR from Monte Carlo behavioral simulations, assuming a clock jitter as low as 250 fs,RMS up to more than 100 ps,RMS. As can be seen, the architecture can tolerate up to 4-5 ps,RMS of jitter without significant degradation of converter resolution, thus validating the multibit NRZ DAC's robustness to clock jitter.

2.10 Summary

The simulated performance of the proposed ADC is summarized in Table 2.1, and a representative FFT of the digitized ADC output when sources of noise and nonlinearity are enabled and disabled is shown in Figure 2-25. All SNR/SNDR calculations assume a 20 MHz input bandwidth, a 900 MHz clock rate (OSR=22.5), and

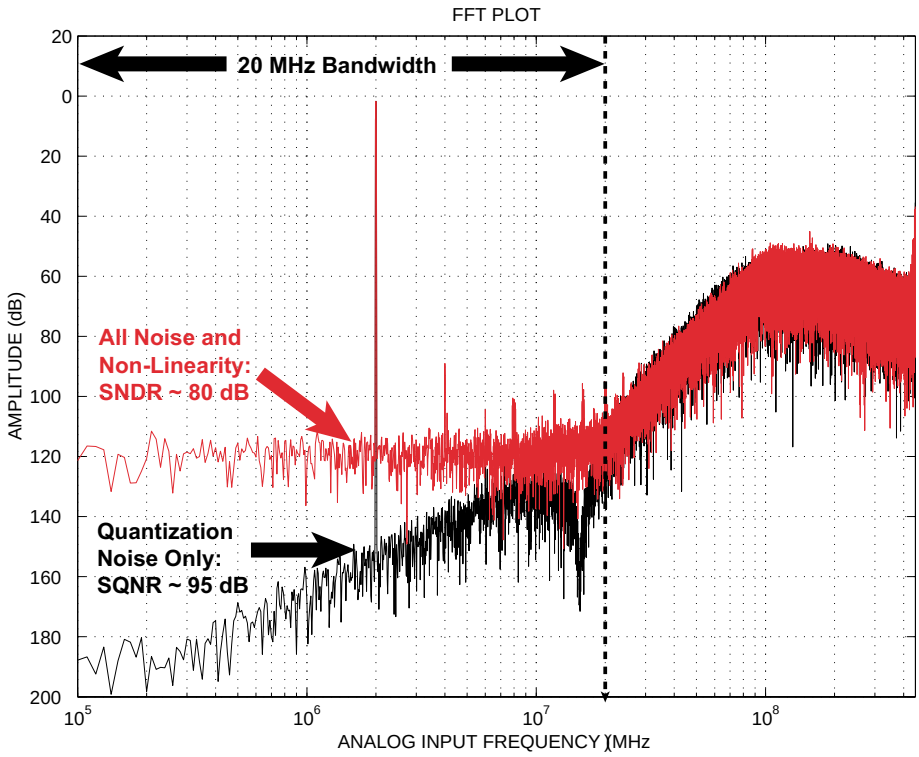


Figure 2-25: representative FFT of the simulated ADC output with quantization noise only (dark) and all noise/mismatch sources included (light).

a 2 MHz input sine wave with an amplitude of -3 dBFS. As shown in row 1 of the table, the converter achieves a signal-to-quantization noise (SQNR) of 95.5 dB. The inclusion of VCO non-linearity in the model (row 2) causes less than 1 dB degradation in SNDR, thus illustrating the advantage of using the VCO as a voltage-to-phase quantizer. Amplifier non-linearity and finite gain-bandwidth, finite DAC output resistance, and thermal noise sources (row 3-5) degrade the SNDR level to about 84 dB. Mismatches in the VCO delay stages (row 6) have less than 1 dB impact on the overall SNDR, despite the high variation of 10%.

To evaluate the effect of DAC unit-element mismatch, variations of $1\sigma = 1\%$ was assumed for the main NRZ feedback DAC, and $1\sigma = 4\%$ were assumed for the minor loop NRZ and RZ feedback DAC's. Although first-order shaped by the DWA algorithm, mismatches in the main DAC feedback (row 7) still degrade the SNR/SNDR by roughly 1 dB. However, ISI in the main DAC has a much larger impact on the converter SNR/SNDR, resulting in a 4 dB decrease (row 8). As expected, ISI and

the first-order shaped mismatches from the minor loop DAC's have a much smaller impact on converter performance compared to the main feedback DAC. Nevertheless, errors in these DAC's result in a 1 dB decrease in SNR (row 9).

-3 dBFS 2 MHz input sine wave with 20 MHz input bandwidth and 900 MHz sample rate (OSR) = 22.5		SNR (dB)	SNDR (dB)
1.	Quantization noise only	95.7	95.5
2.	VCO K_v non-linearity	95.0	94.9
3.	Amplifier non-linearity and finite gain-bandwidth	88.3	87.7
4.	DAC Finite Output Resistance	88.4	88.0
5.	Thermal noise	85.1	84.2
6.	Ring-VCO delay-stage mismatch	84.7	83.9
7.	Main Feedback DAC unit element current mismatch	84.0	82.7
8.	Main Feedback DAC transient mismatch (ISI)	83.9	78.9
9.	**Main and Minor-Loop Feedback DAC's unit-element mismatch and ISI**	**82.9**	**78.3**

Table 2.1: simulated performance of the proposed ADC architecture.

Chapter 3

Circuit Design

This chapter describes the key circuits used in the prototype ADC. The most power intensive block, the analog core, will be introduced first, with the most crucial element toward achieving high performance—the DAC—highlighted. The digital core will be described next, with particular attention paid to the chosen logic family used to implement the DWA circuits. As will be seen, digital power consumption scales with the degree of difficulty in meeting timing specifications for timing critical blocks.

3.1 Analog Core

As mentioned in the previous chapter, the SNDR of the proposed architecture would ideally be limited by thermal noise only. While DAC unit-element mismatch can be minimized with careful layout techniques and device sizing, it is primarily determined by random fabrication and processing conditions, over which the designer has no control. Thermal noise, however, is largely a function of device area and power dissipation, and can be controlled (to some level of accuracy, anyway) by the designer. Therefore, the remainder of this section will not only describe the topologies used to achieve critical analog specifications (i.e. gain, bandwidth, etc.), but will also highlight techniques that enable low noise performance.

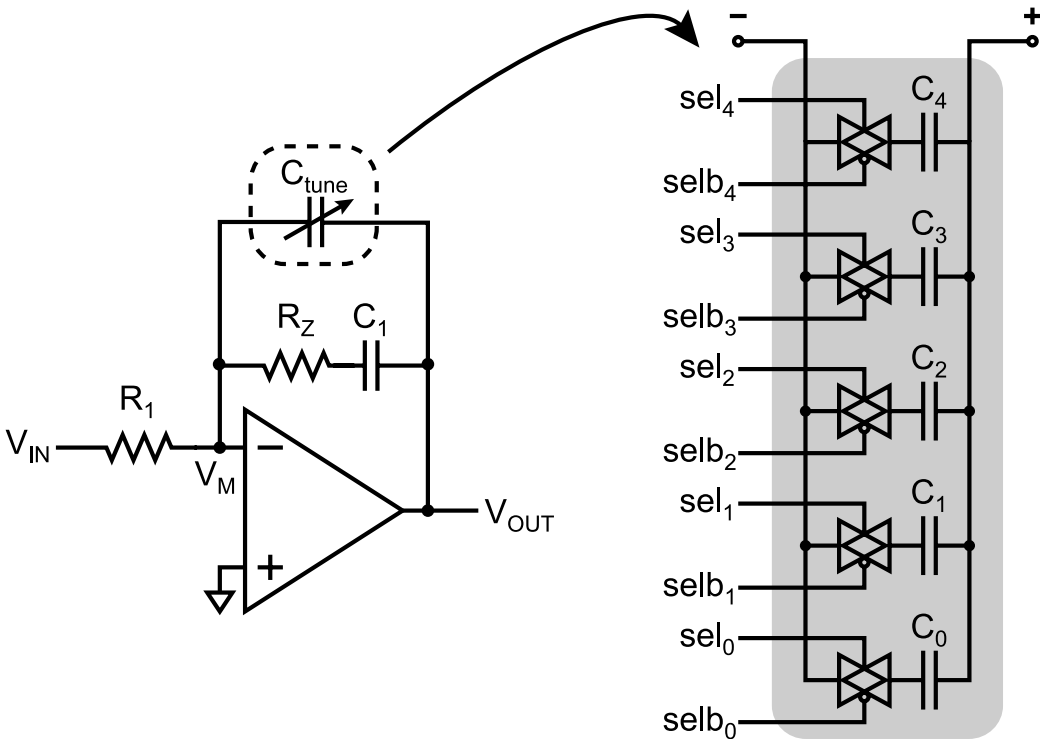


Figure 3-1: tunable integrating capacitor implemented as a 5-bit capacitor bank.

3.1.1 Loop Filter Passives and Calibration

Due to process variations as large as ±40%, the passives in the loop filter (poly resistors and metal-metal capacitors) must be made tunable to obtain the desired frequency response. To cover the desired tuning range, a scheme similar to that used in [36] was adopted. As shown in Figure 3-1, the integrating capacitor value is controlled by a 5-bit DAC, which enables/disables binary-weighted capacitors in a capacitor bank. For the purposes of this prototype, the tuning is performed externally by programming the DAC bits via a shift-register. However, any of the closed-loop calibration algorithms proposed in the literature [64, 36] could easily be adopted to automate this tuning.

3.1.2 Opamp Design

The 0.13 μm CMOS technology used for this thesis presents a few challenges to the design of amplifiers. First, the low power supply of 1.5V introduces voltage headroom

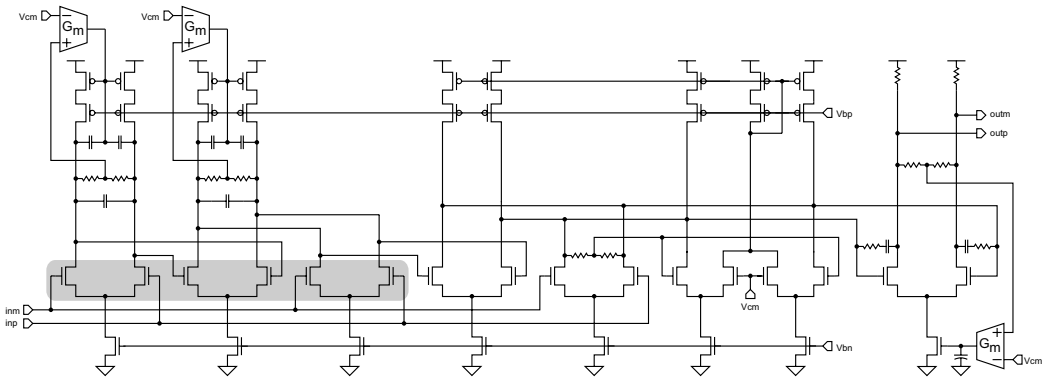


Figure 3-2: schematic of the 4-stage nested Miller opamp. Shaded devices are $1.5 \times L_{min}$

constraints, precluding extensive use of cascoding to obtain high gain in a single stage. Second, transistor flicker noise dominates over thermal noise sources, with the flicker-to-thermal corner frequencies far out into the near gigahertz range for minimum sized devices. Finally, low intrinsic gain (on the order of 12 for a minimum sized device) coupled with the aforementioned headroom issue limits the DC gain of two-stage amplifiers to just above 40 dB, necessitating more complicated and power intensive topologies.

To resolve many of these issues without excessive power dissipation, non-minimum length devices can be used to reduce flicker noise as well as obtain higher intrinsic gain. However, using such devices carries the penalty of reduced f_T, resulting in opamps that typically have lower open loop unity-gain bandwidths for a desired phase margin and given power dissipation than a minimum length device. This poses a severe problem in high-speed CT $\Delta\Sigma$ ADC's since the opamp unity-gain bandwidth should be at least 4 times the ADC sample rate in order to achieve sufficient settling times. Given the proposed architecture's nominal ADC clock frequency of 900 MHz, an amplifier unity-gain bandwidth of 3.5-4 GHz is needed.

Fortunately, multi-stage amplifiers comprising three or more stages (also called nested Miller amplifiers) have been successfully used in prior high-speed CT $\Delta\Sigma$ ADC architectures to achieve the opamp gain and bandwidth requirements [17]. An opamp similar to the 4-stage amplifier proposed in [36] was adopted for this thesis, and is shown in Figure 3-2. Here, high DC gain is obtained by cascading four NMOS

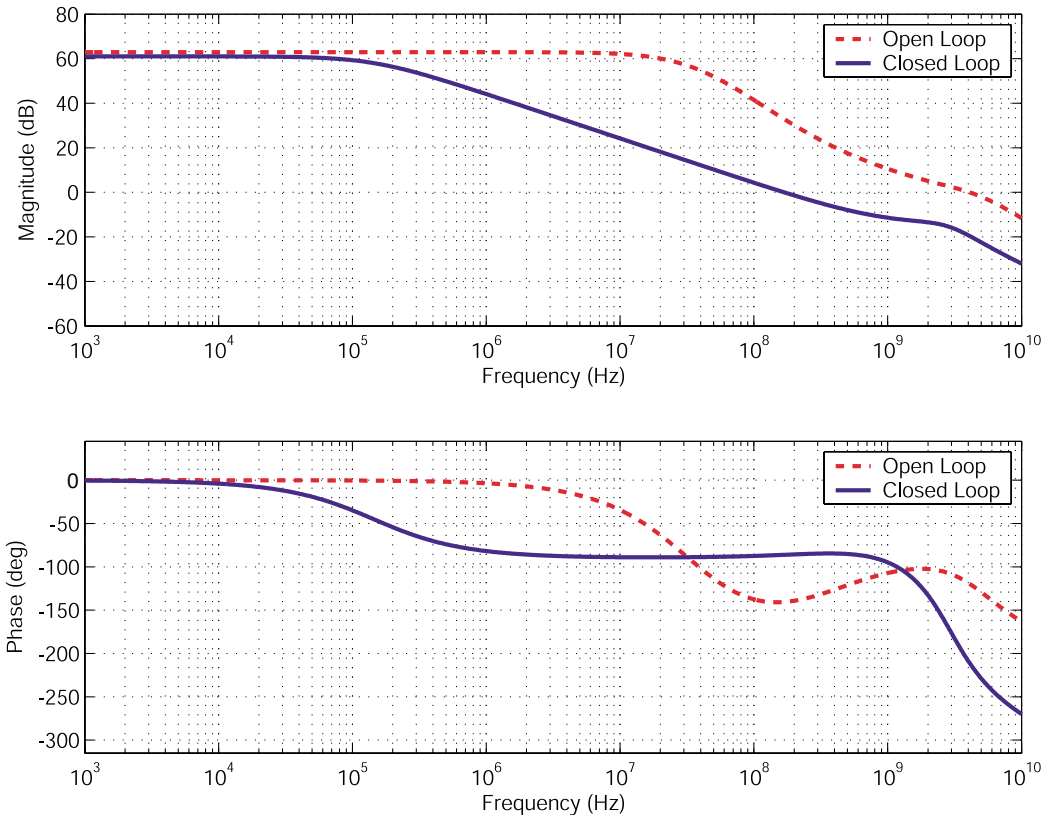


Figure 3-3: simulated open-loop and closed-loop opamp integrator frequency response.

differential pairs loaded by cascoded PMOS current sources. Stability is ensured by the inclusion of two feed-forward paths, which introduce left-half plane zeros that compensate for the additional poles of the cascaded gain stages. Note that the last feed-forward stage that drives the class A output stage is essentially a two-stage opamp, and will primarily determine the unity-gain bandwidth and phase margin of the overall amplifier. A plot of the open-loop frequency response generated from transistor level simulations is shown in Figure 3-3.

The shaded devices in Figure 3-2 use a device length that is 1.5 times greater than minimum length in order to obtain higher intrinsic gain and lower flicker noise. However, the last feed-forward stage and the class A output stage use minimum length devices in order to achieve the desired high unity-gain bandwidth and phase margin. Device noise from these later stages is not a major concern as it is largely suppressed by the gain of the preceding stages.

Since the noise from the first opamp in the loop filter will dominate over the noise from the other amplifiers, it must invariably consume the most power, approximately 22.5 mW. The power dissipation for this first opamp is essentially divided between the first stage input pair and the class A output pair. High currents in the class A stage are needed not only to drive the resistive loads at the output, but also to ensure that the parasitic pole induced by the effective output load capacitance does not significantly degrade the overall amplifier phase margin. This load capacitance is especially large for the first opamp due to the substantial input capacitance of the input devices ($> 1pF$) and the wiring and device capacitance of the main DAC ($> 300fF$).

A summary of the simulated gain, bandwidth, noise, and power dissipation for the first opamp is shown in Table 3.1. Since the noise from second and third opamp will be suppressed by the gain of the first opamp, lower bias currents and smaller devices can be used in the input stages. And since neither of these opamps has a DAC attached to the virtual ground node, the total load capacitance is reduced, enabling smaller currents for the class A output stage. For simplicity, the second and third opamps are identical, each consuming 11.2 mW in order to realize the desired unity-gain bandwidth of 4 GHz. It should be noted that the opamp power dissipation was not optimized, and that a class AB output stage would be more power efficient. Since the opamps consume the majority of the analog power, it is possible that such design refinements and optimizations could reduce this power by as much as 10-20%.

Parameter	Value
DC Gain	63 dB
Unity-Gain Frequency	4.0 GHz
Phase Margin	55^o
Input Referred Noise Power (in 20 MHz Signal BW)	$1.2e^{-10}V^2$
Power ($V_{DD} = 1.5V$)	22.5 mW

Table 3.1: performance summary of the first opamp in the loop filter.

3.1.3 Main and Minor-Loop NRZ Feedback DAC's

In the design of the main feedback DAC, three design specifications are of paramount importance: unit-element matching, device noise, and switching dynamics. While meeting these design specifications are important in the design of all the feedback DAC's, it is especially crucial to do so in the design of the main feedback DAC as all noise, non-linearity, and other non-idealities appear at the input and are not shaped. This section will address each of these specifications, starting with the static characteristics: device noise and unit-element matching.

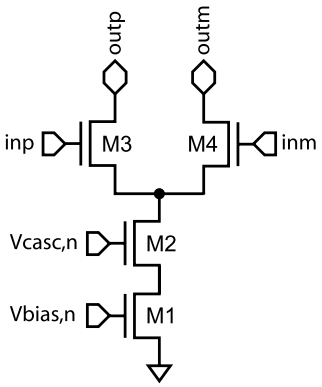
As was the case in the design of the amplifiers, flicker noise dominates the output current noise profile of the standard cascoded DAC (see Figure 3-4(a)). Using long devices ($L \gg 1\mu m$) can help reduce the flicker noise contribution from the dominant noise source (the tail device M1), but necessitate that the width be proportionately scaled to ensure device saturation, resulting in a large area penalty.

A simpler and much lower area solution is to use poly resistors, which do not exhibit flicker noise (see Figure 3-4(b)). While the output resistance of the resistor is lower than that of the saturated NMOS, double and even triple cascoding can be leveraged to boost the output resistance of the DAC further. Triple cascoding is made possible by ensuring that the switch devices are saturated. DAC noise of the structure shown in Figure 3-4(b) will then largely be dominated by the thermal noise of the resistor and the flicker noise from the degenerated cascoded device (M1). Indeed, thermal and flicker noise of the degenerated device will be lowered by the degeneration gain:

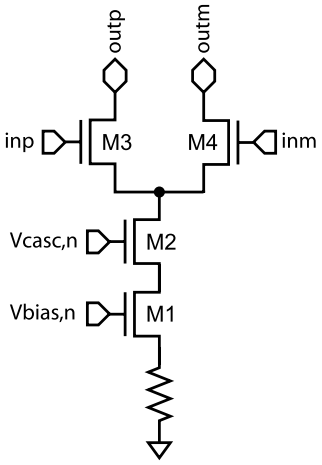
$$i^2_{no,M1}(f) \approx \left(\frac{8}{3}\gamma kT g_{m.M1} + \frac{K g^2_{m,M1}}{WLC^2_{ox}f}\right) \cdot \left(\frac{1}{1 + g_{m,M1}R}\right)^2 \tag{3.1}$$

While low, this flicker noise can be further reduced by using slightly longer devices (twice minimum length) and increasing the device width.

Monte-Carlo simulations have shown that the structure of Figure 3-4(b) had a 1σ deviation of less than 0.6%. Due to the resistive degeneration of the cascoded device, the matching largely appears to be determined by the matching of the poly resistors,



(a)



(b)

Figure 3-4: schematics of (a) a standard cascoded current-steering DAC, and (b) the implemented current-steering DAC with resistive degeneration to minimize flicker noise.

which are assumed to have nearly the same deviation.

Parameter	Value
I_{total}	$10mA$
I_{LSB}	$625\mu A$
Unit-Element Output Resistance	$70k\Omega$
Unit-Element Output Current Noise Power (in 20 MHz Signal Bandwidth)	$1.1e^{-15}A^2$
Total Input Referred Noise Power (Total Output Current Noise Power $\times R_{in}^2$)	$1.7e^{-10}V^2$
Power ($V_{DD} = 1.5V$)	15 mW

Table 3.2: performance summary of the main feedback DAC.

Switching dynamics add layers of complexity to the overall DAC design, as charge injection, clock feed-through, and rise-fall mismatches can influence the overall ADC's performance as much as unit-element mismatch and noise. While the literature is rife with various DAC implementations to address these issues, a design methodology similar to that in [64] was adopted as it had been successfully used to achieve high resolution ($\approx$ 14 ENOB) in a prior CT $\Delta\Sigma$ ADC.

The complete main DAC signal path is shown in Figure 3-5, and plots generated from transistor-level simulations of the unit element output current and low-swing buffer voltage output switching waveforms are shown in Figure 3-6 . Since the digital data from the DWA will arrive at arbitrary times within a sample period T_s, a latch is needed to retime and generate differential data signals for the DAC switching buffers. A differential, regenerative TSPC structure was used for its simplicity, requiring only one clock phase [67].

Charge injection, clock/data feedthrough, and other switching-related errors are minimized by connecting the buffer supplies ($V_{DD,SW}$ and $V_{SS,SW}$) to two external voltage supplies to generate low-swing outputs, and sizing the PMOS devices to generate strong pull-up edges, and weak pull-down edges. This particular signaling ensures that at least one of the switching devices is always saturated, enabling triple cascoding of the DAC unit element. At the same time, the scheme minimizes perturbations caused by the discharging the DAC unit-element tail node capacitance that would otherwise generate large current spikes at the output. Note, however, that the

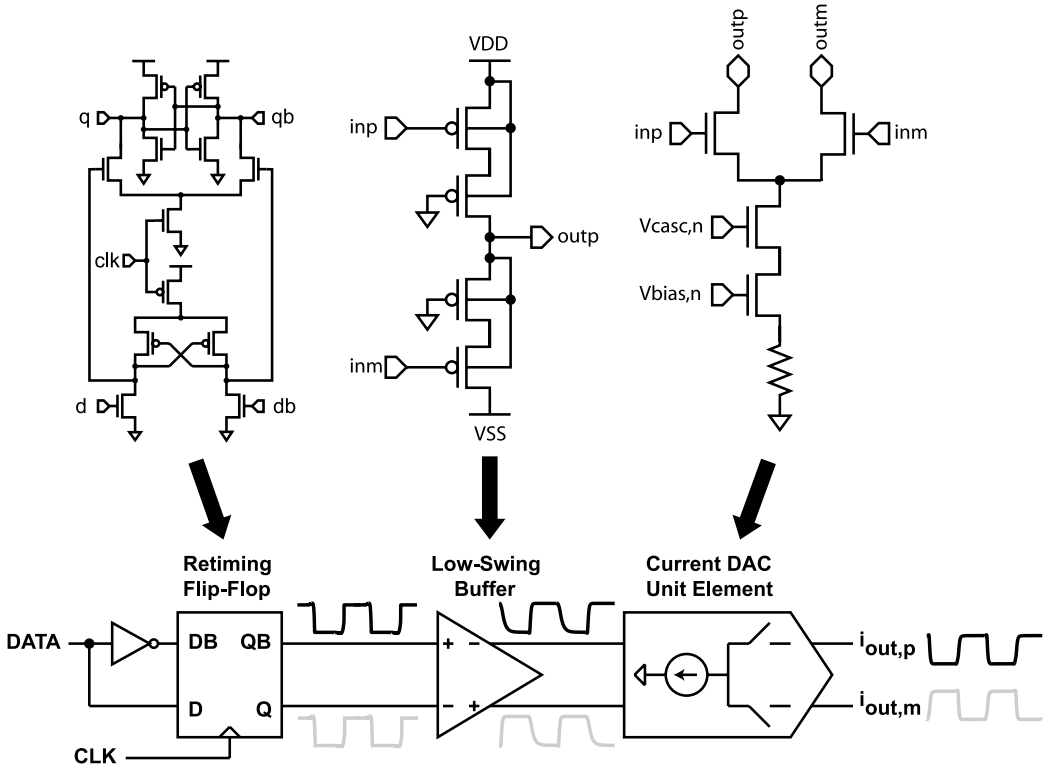


Figure 3-5: the main NRZ DAC signal path and switching waveforms with key circuit blocks. For the sake of simplicity, the supply voltages for the low-swing buffer ($V_{DD,SW}$ and $V_{SS,SW}$) are provided off-chip.

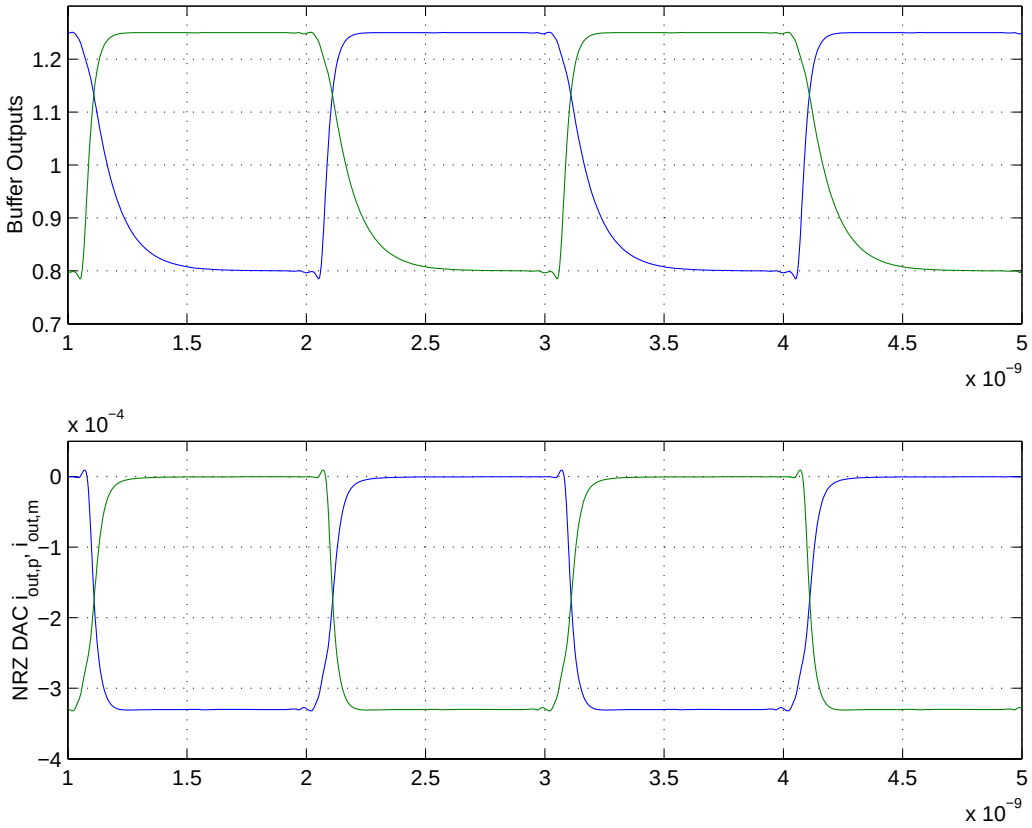


Figure 3-6: transistor-level simulation of unit-element output current and low-swing buffer output voltage switching with strong pull-up and weak pull-down.

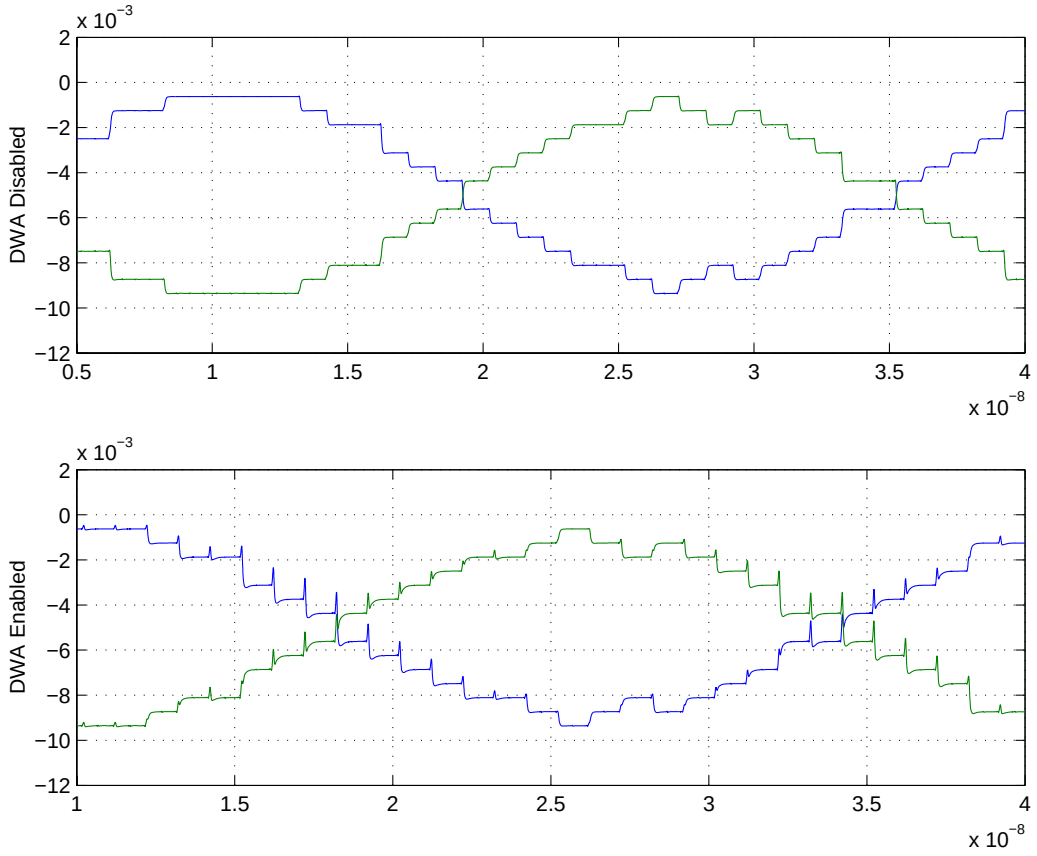


Figure 3-7: transistor-level simulation of main NRZ DAC output current when DWA is disabled (top) and enabled (bottom).

code-dependence of any switching transient mismatches will still be present, and will not be shaped by the DWA. As described in the previous chapter, the DWA cannot shape such ISI when codes larger than half of full scale are input into the NRZ DAC, which is evident in the transistor-level simulation plot of Figure 3-7.

Since the noise and mismatch error of the minor-loop NRZ feedback DAC is suppressed by the gain of the loop filter, neither poly resistor degeneration nor very long tail devices ($> 1\mu m$) are necessary. Instead, a standard cascoded DAC structure identical to that in Figure 3-4(a) can be adopted. As before, triple cascoding is enabled by limiting the voltage swings to the current steering pair such that one device is always saturated. All other circuitry (retiming latches, limited swing drivers) is identical to those in the main feedback DAC. However, the smaller devices and absence of resistive degeneration will result in a higher unit-element mismatch. Indeed, Monte-

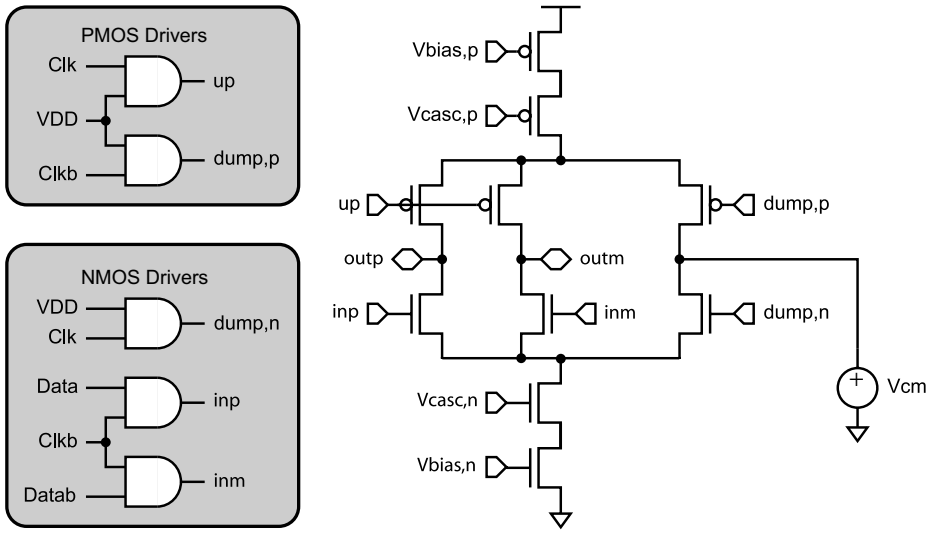


Figure 3-8: schematic of the loop delay compensating RZ DAC.

Carlo simulations reveal that this secondary DAC has a mismatch with a 1σ deviation of 3.2%.

3.1.4 RZ feedback DAC

Unlike the NRZ DAC, switching transient mismatch (ISI) is not a significant concern for the RZ DAC. Since the output sees both a rising and falling transient within the sample period, the glitch energy from clock/data feed-through, charge injection, and other transient effects will always be encountered, eliminating code dependency so long as the DAC output waveform settles—a constraint that is more challenging to meet as the bandwidth of RZ signals are effectively twice that of NRZ. Nevertheless, the RZ signaling scheme's robustness to glitch energy allows the use of full swing logic instead of limited swing drivers to control the DAC.

A schematic of the RZ DAC structure and the RZ pulse shaping logic are shown in Figure 3-8. Note that retiming latches are not needed so long as the input to the logic settles before the rising edge of CLKB. During the zero clock phase (CLK), the DAC current is dumped to a third drain connected to an external voltage V_{CM}, with a nominal value of $\frac{V_{DD}}{2}$. Also note that only the NMOS current steering devices are controlled in a data-dependent matter, while the PMOS current steering devices

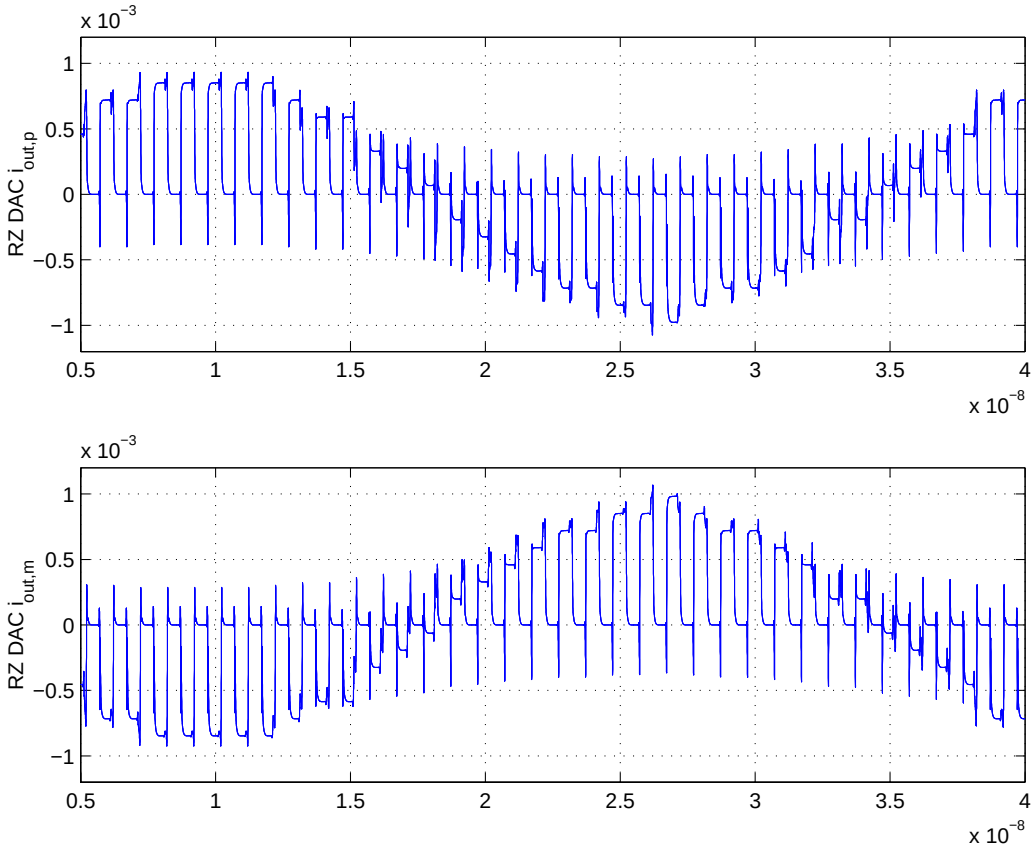


Figure 3-9: transistor-level simulation of the RZ DAC output currents.

are controlled by the clock phases CLK and CLKB. While both NMOS and PMOS current steering devices could be controlled by the data, resulting in lower DAC noise, the simpler structure shown in Figure 3-8 was adopted since such noise is suppressed by the loop filter gain. A transistor-level simulation plot of the RZ DAC output current is shown in Figure 3-9. Monte-Carlo simulations reveal that the RZ DAC unit elements have a mismatch of $1\sigma = 2.7\%$.

3.1.5 VCO Integrator and Quantizer

The highly digital nature of the proposed VCO integrator and quantizer can be appreciated with the aid of Figure 3-10. The VCO delay element is based on the current starved inverter from [55], and enables full-swing output signals as well as pseudo differential control of the output frequency. The nominal oscillation frequency and K_v can be tuned to cover process variations through the selection of 4 digital bits

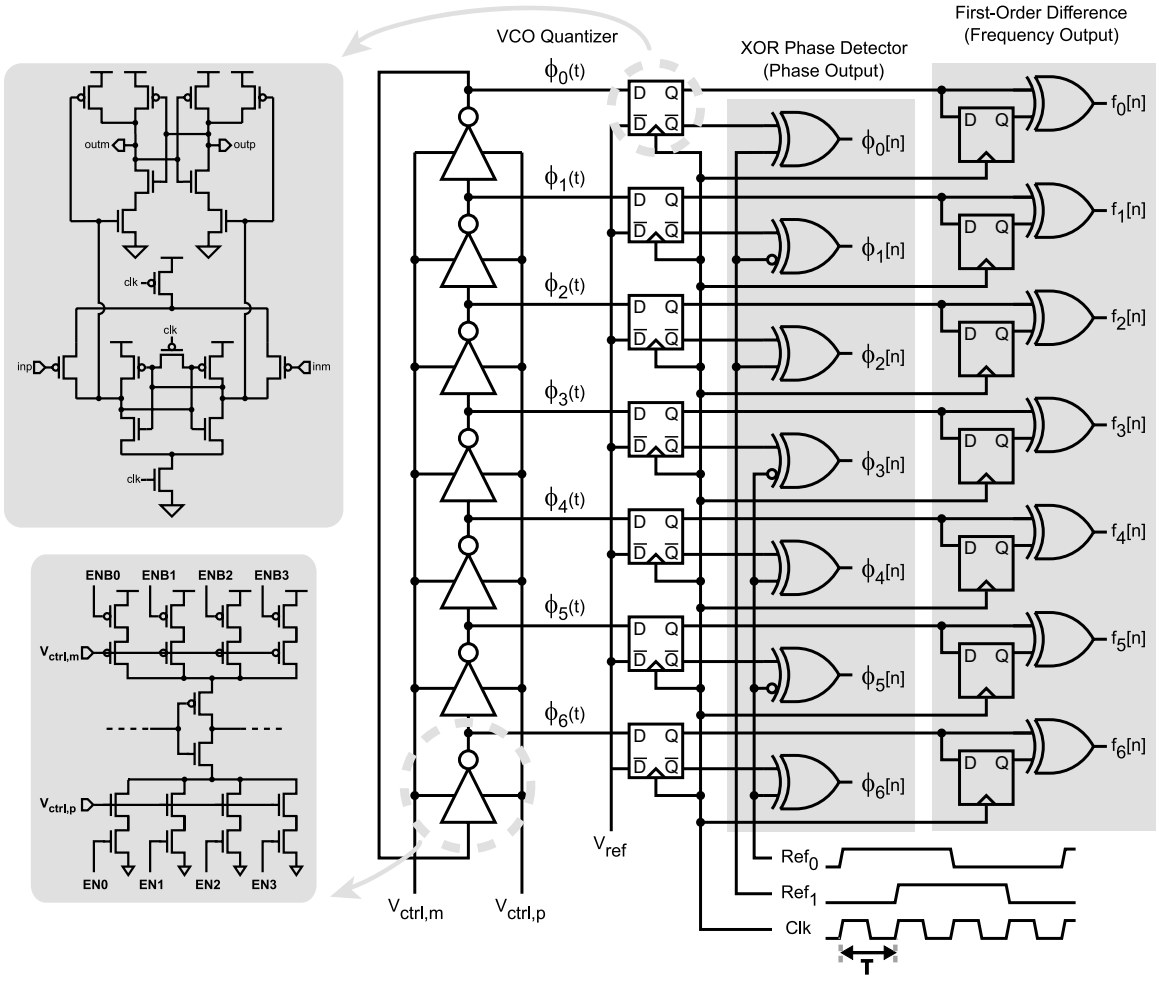


Figure 3-10: schematic of the ring-VCO integrator and SAFF quantizer, phase detector and frequency detector (first-order difference).

($EN_0 - EN_3$). The sense-amp flip-flop (SAFF) from [40] quantizes the VCO output phase by comparing the continuous output level of a given VCO phase tap to the chip common mode voltage at half of the supply. Phase detection and first-order difference computation are achieved using static CMOS XOR gates and single-ended TSPC flip-flops.

The ring-VCO nominally oscillates at a frequency of 225 MHz, but can span from nearly 0 Hz to approximately 450 MHz when the control voltages are swept (see Figure 3-11). A phase noise plot of the VCO when oscillating at the nominal frequency is shown in Figure 3-12. While large, the phase noise is largely suppressed by the loop filter gain, and will therefore have a negligible noise contribution when input-referred.

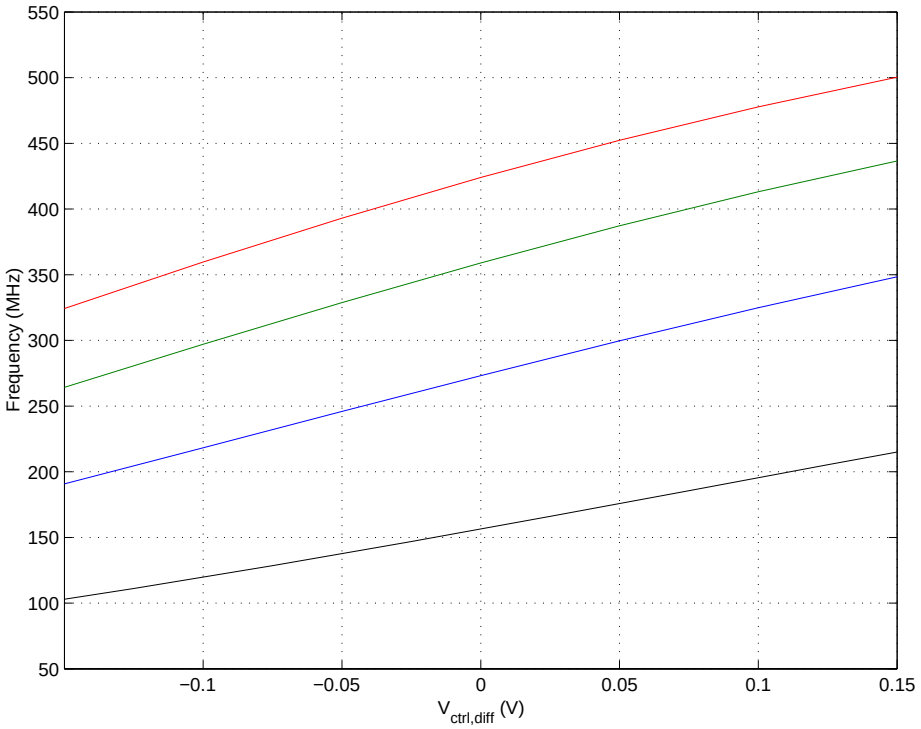


Figure 3-11: K_v tuning curves of the 15-stage ring-oscillator for different tuning gains enabled.

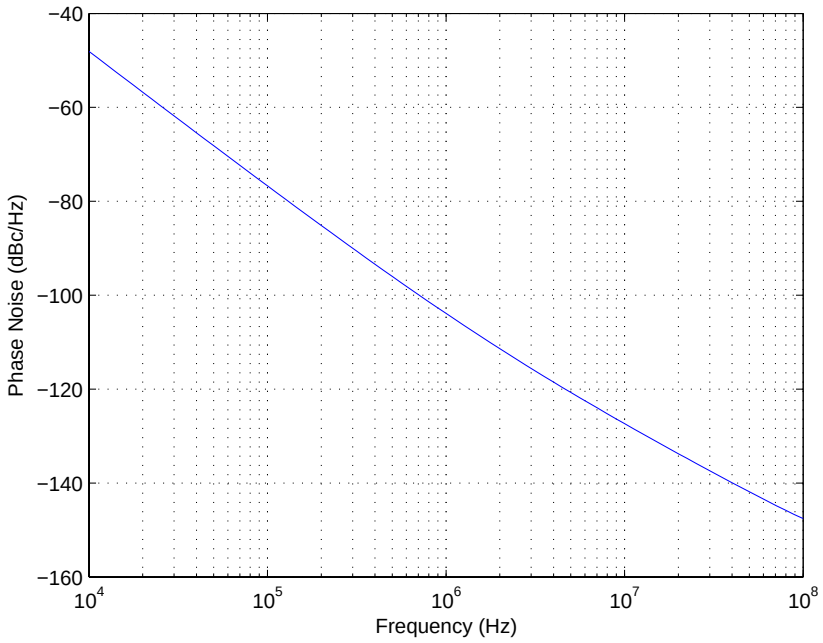


Figure 3-12: simulated phase noise of the 15-stage ring-oscillator when oscillating at approximately 225 MHz.

The phase detector reference signals also have a frequency of 225 MHz, and can easily be generated by dividing the 900 MHz ADC clock frequency by 4. The quadrature relationship between Ref_0 and Ref_1 can be obtained by simply delaying one reference signal relative to the other by one period of the 900 MHz clock. Since the ADC clock rate is at least twice the maximum VCO oscillation frequency, the frequency output thermometer code generated by the first-order difference ($f_0[n]$ to $f_6[n]$ in Figure 3-10) will automatically correspond to a DWA sequence, as was the case in [55]. Consequently, the RZ DAC's will implicitly have their mismatch first-order shaped.

The output phase error is generated by XOR'ing each quantized VCO phase with one of two reference phases (or their complements). The resulting thermometer code ($\phi_0[n]$ to $\phi_6[n]$ in Figure 3-10), is then proportional to the phase error. A subtle issue with this particular phase detection scheme is that the phase error thermometer output does not have a consistent order like conventional thermometer codes generated by flash ADC's. Rather, the code tends to toggle back and forth depending on the reference phase, which can complicate the computation of the DEM sequence and the equivalent binary code. Consequently, the circuits that explicitly perform DEM on the phase error output must deal with this issue, as will be discussed next.

3.2 Digital Core

While architectural innovations can alleviate bottlenecks in timing-critical digital blocks, the finite gate delays in the $0.13\mu m$ technology used in this thesis nevertheless dictate the choice of logic family and implementation. Unavoidable interconnect parasitics can complicate matters further by reducing timing margins and precluding the use of standard, static CMOS logic. Consequently, the power dissipated by a given digital block is often proportional to the degree of difficulty in satisfying its timing constraints. This section will highlight this tradeoff between timing and power in the design of the proposed DWA architecture (a 3-bit version is repeated in Figure 3-13 for convenience).

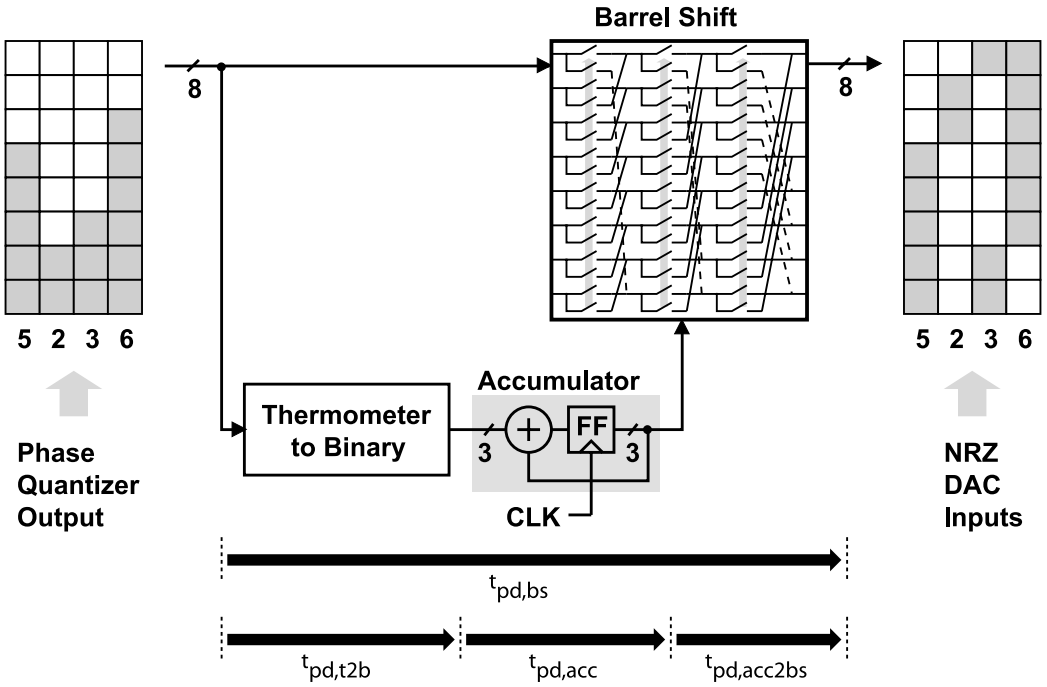


Figure 3-13: proposed DWA architecture, comprising a barrel shift and an accumulator.

3.2.1 DWA Barrel Shift and Accumulator

A topology that correctly generates the desired DWA sequence while accounting for the toggling thermometer code of the quantized VCO phase outputs is shown in Figure 3-14, where for simplicity, a 3-bit design is shown while in actuality, a 4-bit version was implemented. Here, a barrel shift is controlled by an accumulator residue and a half-rate clock signal generated by a divider. Since the thermometer code toggles around mid-scale at every-other cycle, the half-rate clock inverts the MSB control at every-other cycle so that the code maintains a regular order.

A subtlety in using a binary controlled barrel shift is that while the ring-VCO has an odd number of stages (and therefore an odd-number of outputs), the matrix must have an even number of inputs in order to be controlled by a standard 4-bit accumulator. While the extra input to the switch matrix can be simply grounded, its zero value must also toggle around mid-scale as the input thermometer code does in order to be correctly compensated for by the MSB inversion. Once again, this can be accomplished with the aid of the half-rate clock signal (flip) controlling an array of

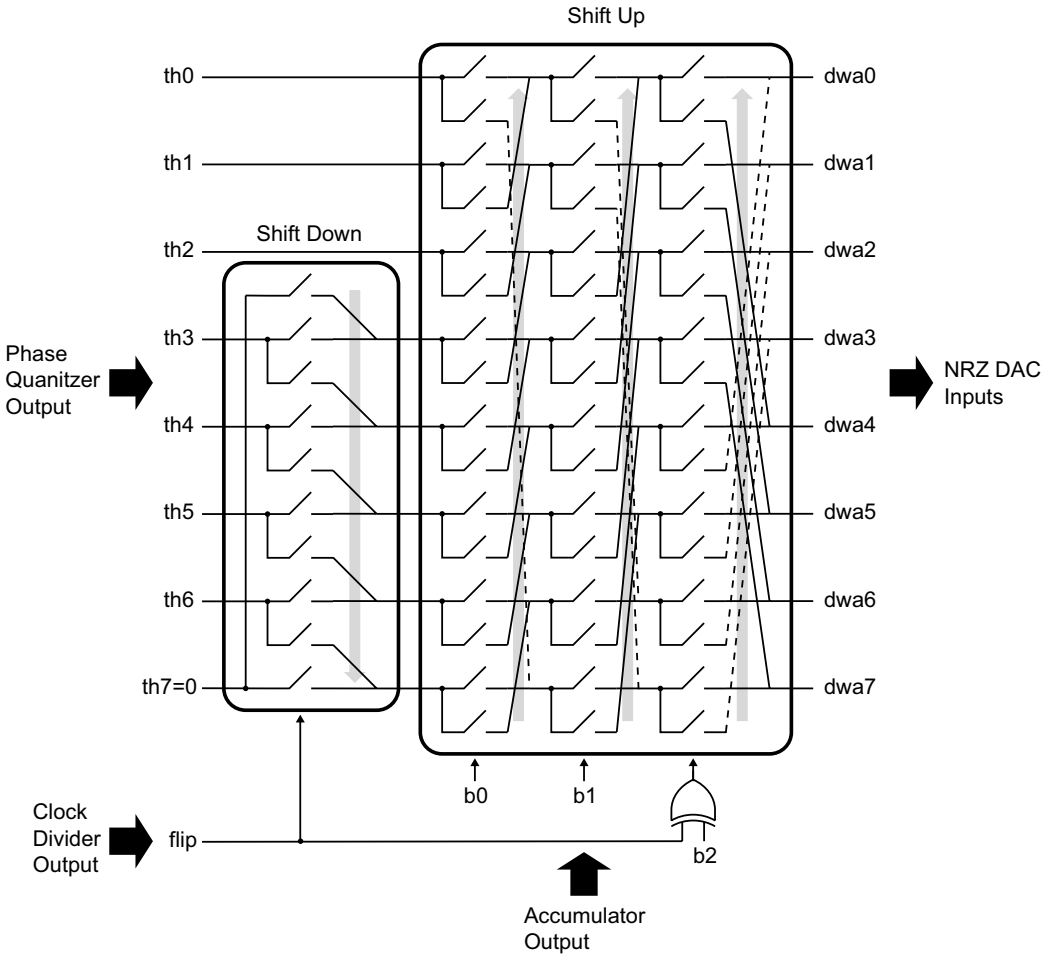


Figure 3-14: schematic of the binary controlled barrel shift. For simplicity, a 3-bit version is shown, though a 4-bit version was actually implemented.

switches at the input, as shown on the left hand side of Figure 3-14. Use of close to minimum-sized transmission gates and regenerating buffers enables data to propagate through the switch matrix in half a sample period, exclusive of the clock-to-Q delay of the phase quantizer and phase detection logic. Thus, the barrel shift itself does not present a significant bottleneck in the DWA timing.

The toggling thermometer code output from the VCO phase quantizers also complicates the computation of the equivalent binary code in the thermometer-to-binary encoder. One solution to this problem is to implement a cascade of half adders to sum up all the thermometer bits to form the equivalent binary code (see Figure 3-15). The adder-based encoder accomplishes this task with a maximum depth of 10 gates to generate the 4-bit binary output code, and 15 gates to generate the accumulated output. Unfortunately, a fully static-CMOS implementation of the logic was not able to satisfy the timing requirements with sufficient margin due to wiring capacitances that extended nominal gate delays from 25 ps to 50 ps. Dynamic or domino logic cannot be used as adder outputs may glitch as data propagates through the accumulator, necessitating complicated skewed clocking schemes that could still be prone to glitch errors. A pseudo NMOS logic implementation using PMOS loads was able to satisfy timing, though at the expense of higher power consumption (15 mW for pseudo NMOS, compared to < 7 mW for static CMOS). Fortunately, the use of inverting gates as well as leveraging the embedded NAND/NOR output inside the XOR/XNOR gates enabled a minimal gate count (see Figure 3-16).

3.2.2 Clocking

While the full-rate 900 MHz clock signal to the ADC is supplied off-chip, a series of buffers, dividers, and retiming flip-flops are needed to generate the necessary clock and reference phases to the DAC's, quantizer, phase detector, and DWA. As shown in Figure 3-17, the external clock signal is buffered on-chip to full-scale using CMOS inverters. Since the DAC's are very sensitive to jitter, their clock signals are distributed using the fewest number of intermediate buffers possible. The phase detector reference signals are generated using a cascade of divide-by-two's and retiming flip-flops.

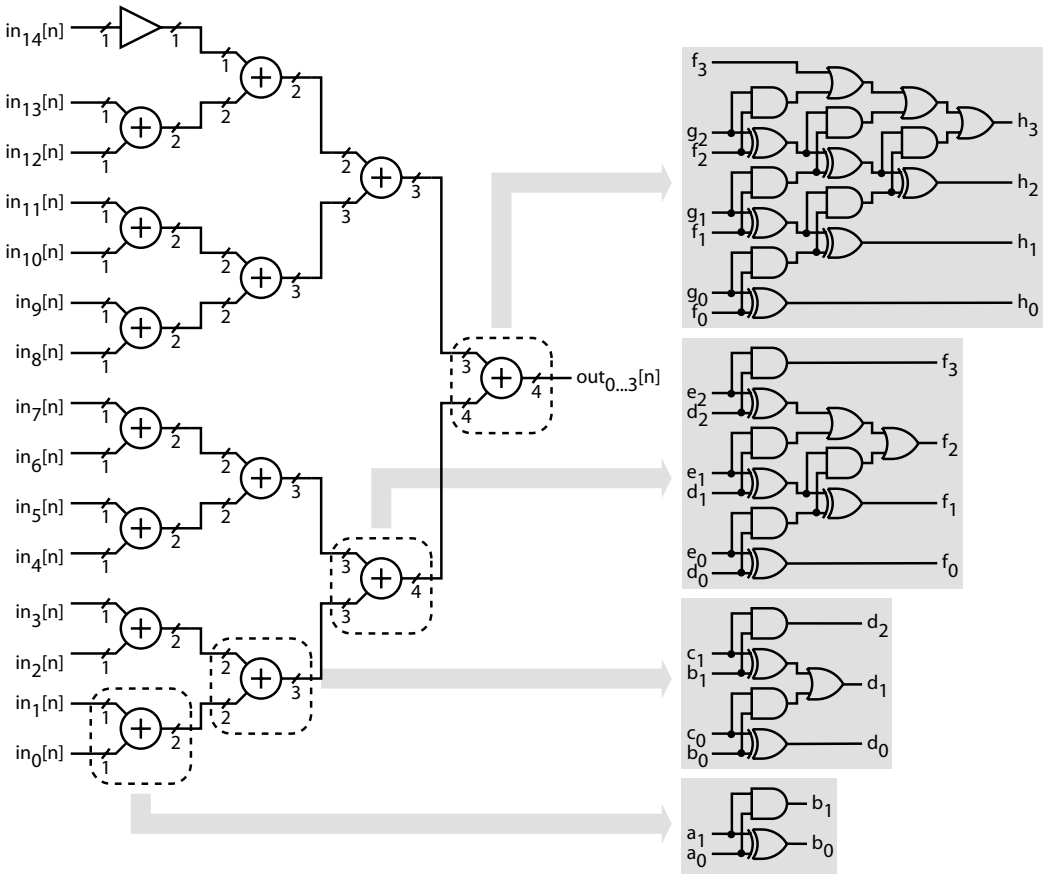


Figure 3-15: the thermometer to binary converter implemented by summing individual thermometer bits with a cascade of half-adders.

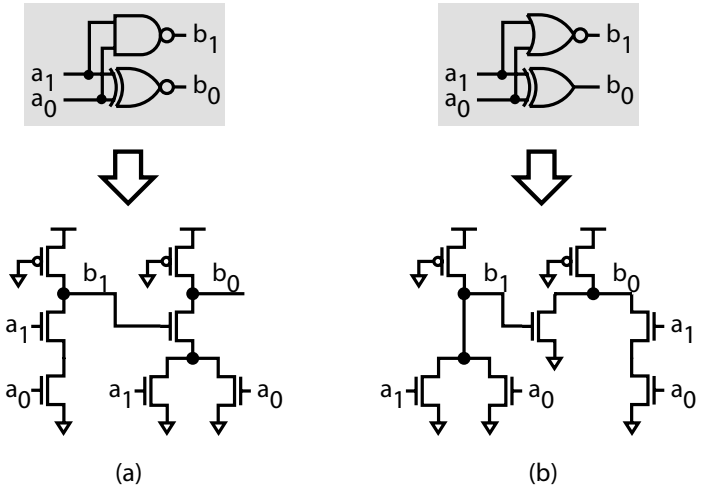


Figure 3-16: Pseudo NMOS logic with PMOS load implementation of the XOR/XNOR operation with embedded NAND/NOR.

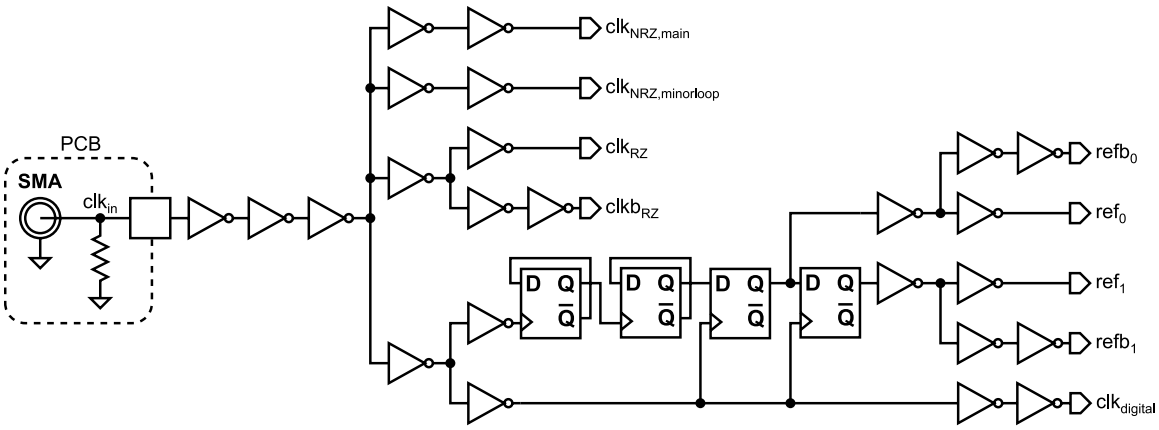


Figure 3-17: CMOS clock buffering, reference generation, and distribution circuits.

Retiming of the reference phases generated by the asynchronous dividers is possible since the extra clock-to-Q delays of these flip-flops is smaller than those of the phase quantizers.

3.2.3 Output Buffers

While full-swing CMOS buffers can be designed large enough to drive a bond pad, they can potentially cause undesirable noise coupling to sensitive analog circuits through the substrate as well as significant ringing on the power supply. Consequently, fully differential, low-swing ($400mV_{pp,diff}$) CML buffers were implemented with the hopes that their constant bias currents would minimize charge injections into the substrate during switching. As shown in Figure 3-18, the buffers are progressively scaled up until the last buffer in the chain can drive a 50Ω load. Outside the chip, output data PCB traces are drawn to provide an approximate impedance match, and terminated either by the 50Ω load of the high-speed sampling scope or a 50Ω resistance to the board ground plane.

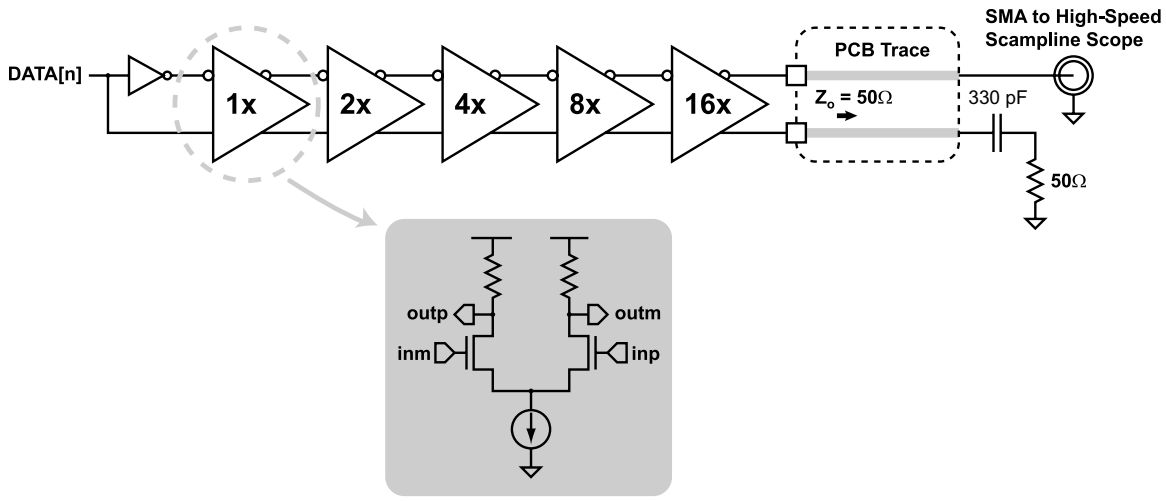


Figure 3-18: CML buffer chain to drive output data onto PCB.

Chapter 4

Measured Results

The test setup used to evaluate the prototype ADC is shown in Figure 4-1. Here, an analog signal source (Agilent E4430B) drives a 2 MHz tone into a passive bandpass filter (TTE KC7T-2M-10P-50-720B), which suppresses the harmonics and phase noise of the signal source. An RF transformer (Mini-Circuits ADT1-6T+) converts this spectrally purified tone into a differential signal that serves as the input to the prototype ADC. The ADC clock signal is generated by a high-speed pattern generator (HP 70843B), which can generate low-jitter, square waveforms (< 1 ps,RMS in bandwidth of interest). The 4 digital output bits generated by the prototype ADC are stored into the memory of a high-speed sampling oscilloscope (Agilent DSA 80000B), and then downloaded to a PC for post-processing.

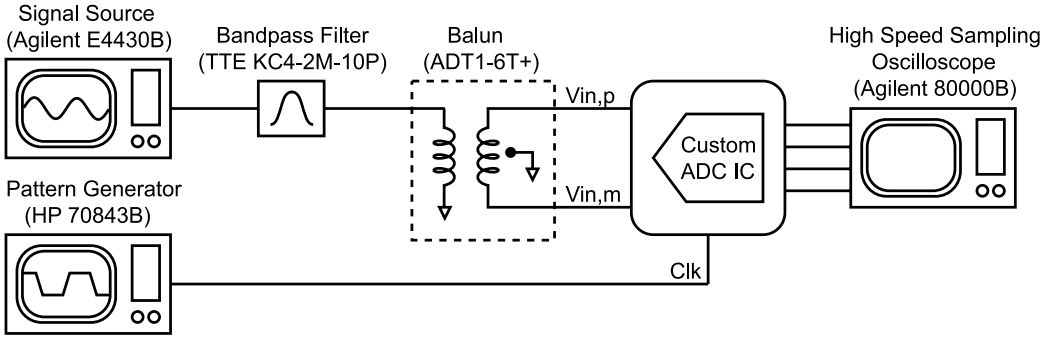


Figure 4-1: test site for the evaluation of the prototype ADC.

A die-photo of the fabricated prototype ADC in IBM's $0.13\mu m$ CMOS is shown in Figure 4-2. The active silicon area of the ADC is $0.45mm^2$, and the total chip area

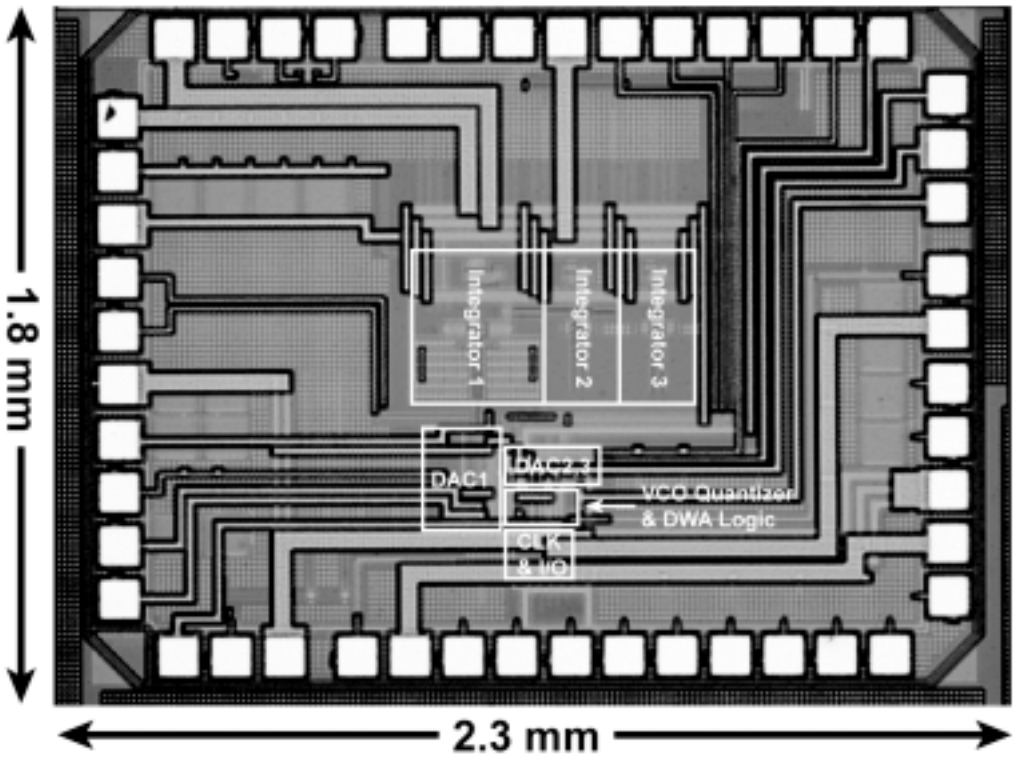


Figure 4-2: die photo of the prototype ADC fabricated in a $0.13\mu m$ IBM CMOS process. The active area is $0.45mm^2$.

Specification	Value
Sampling Frequency	900 MHz
Input Bandwidth	20 MHz
Peak SNR	81.2 dB
Peak SNDR	78.1 dB
Analog Power	69 mW (1.5V)
Digital Power	18 mW (1.5V)
FOM	330 fJ/conv
Active Area	$0.45mm^2$
Technology	$0.13\mu m$ IBM CMOS

Table 4.1: performance summary of the prototype ADC.

including 48 pads is $2.3mm \times 1.8mm$. A table summarizing the ADC performance is found in Table 4.1, where the figure of merit (FOM) is defined as:

$$FOM \equiv \frac{P_{diss}}{2 \times f_{BW} \times 2^{ENOB}}. \tag{4.1}$$

The prototype ADC dissipates 87 mW from a 1.5V supply, with the analog and digital supplies drawing roughly 46 mA and 12 mA, respectively. Although there is no direct way to measure the subsystem current, bias currents indicate that the DAC's consume 15 mA, the operational amplifiers consume 30 mA, and the VCO consumes less than 1 mA. Simulations indicate that the data-weighted averaging logic comprises the majority ($> 75\%$) of the digital power dissipation due to the use of current mode logic in the accumulator, with VCO phase quantizer flip-flops and clock generation/distribution circuits comprising the remainder.

The SNR and SNDR versus input amplitude curves are shown in Figure 4-3. For these measurements, the input tone frequency is 2 MHz, the analog bandwidth is 20 MHz, and the sample rate is 900 MHz. For a -2.4 dBFS input tone, the ADC achieves a peak SNR of 81.2 dB and a peak SNDR of 78.1 dB (12.7 ENOB, FOM $\approx$ 330 fJ/conv).

A fast Fourier transform (FFT) of the ADC output with a 2 MHz input signal at -2.4 dBFS is shown in Figure 4-4. Fourth-order quantization noise shaping is visible in the frequency range from 20 MHz to 70 MHz, and peaks locally at 70 MHz due to a phase margin degrading parasitic pole at the loop filter output summing junction.

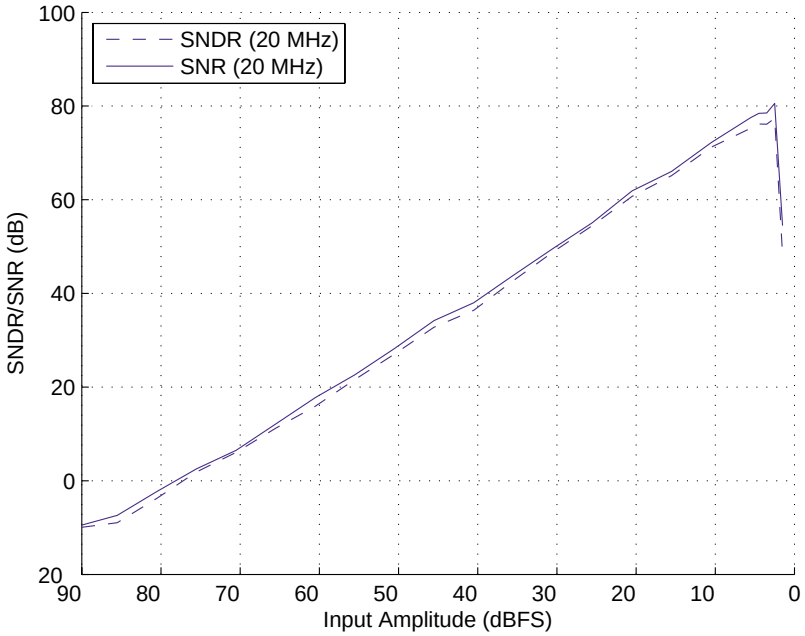


Figure 4-3: measured SNR/SNDR versus input amplitude.

Behavioral simulations suggest that the tones appearing in the 200-250 MHz range and centered at 225 MHz ($\frac{F_s}{4}$) are most likely due to the phase detector reference clock signal and the VCO output phases parasitically coupling into the VCO control node. Fortunately, these tones are far out of band and did not affect the resolution or stability of the ADC.

Note the slight increase in the noise floor in the 5-20 MHz range, as well as the presence of even and odd order distortion tones (present even with no input power). Both of these artifacts are most likely caused by mismatches in the DAC unit element currents and switching transients. As was predicted in the behavioral model, the first-order shaped unit-element mismatch noise power tends to rise above the thermal noise floor in the 5-20 MHz frequency range, resulting in a degraded SNR. At the same time, mismatches in the NRZ DAC switching transients cause greater ISI error, leading to inband distortion tones similar to those encountered in measurement. Indeed, varying the supply voltage of the buffers that drive the DAC switches provided some empirical evidence of ISI, as any deviations consistently resulted in worsened inband distortion. While these results indicate that the SNDR of the converter could be improved by

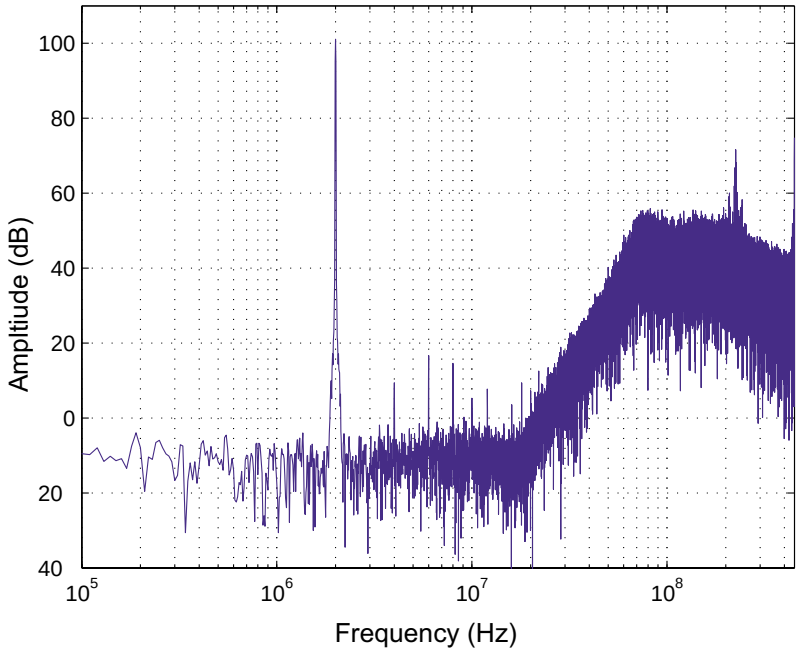


Figure 4-4: 100,000 point FFT plot generated from the measured output data stream of the prototype ADC.

using a DAC structure that has better matching and is more robust to ISI, they more importantly demonstrate that the proposed architecture is robust to the VCO K_v non-linearity that limited the resolution of prior voltage-to-frequency VCO-based ADC's.

A comparison of the measured results of this work with other CT $\Delta\Sigma$ ADC's operating at a sample rate above 250 MHz is shown in Table 4.2. The 80 dB SNR and 78 dB SNDR of this work shows that VCO-based ADC's can be leveraged in high performance applications, and that the non-linearity of the VCO K_v curve is not a limiting factor to achieving such performance. Continued device scaling should improve the power efficiency of the entire structure, as full-swing static CMOS can replace the power hungry pseudo NMOS logic, yielding greater than 50% reduction in digital power consumption. At the same time, a more optimized opamp design can likely yield greater than 10% reduction in the overall analog power consumption. Indeed, equivalent performance with near 50 mW power consumption may be possible by simply scaling the design to the next technology node.

Ref.	Fs (MHz)	BW (MHz)	SNR (dB)	SNDR (dB)	Power (mW)
[61]	276	23	70	69	46
[10]	340	20	71	69	56
[45]	400	12	64	61	70
[50]	640	10	72	66	7.5
[36]	640	20	76	74	20
[49]	1000	8	63	63	10
[55]	950	20	75	67	40
This work	**900**	**20**	**81**	**78**	**87**

Table 4.2: comparison of recent CT $\Delta\Sigma$ ADC's with similar input bandwidths and technology.

Chapter 5

Future Directions

The measured results from the previous chapter suggested that the prototype ADC's resolution was most likely limited by ISI from the main feedback DAC. This suspicion was also confirmed through behavioral simulation, which showed that the proposed architecture's primary limitation to achieving > 13 ENOB performance was mismatch and ISI in the feedback DAC's. At the same time, behavioral modeling of the opamp's non-linearity showed that the amplifiers needed to achieve unity-gain bandwidths that were at least four times that of the sampling frequency in order to suppress quantization noise-folding effects—a challenging requirement to meet in the 0.13 μm technology.

The circuit design portion of the thesis revealed that while the proposed explicit DWA implementation could significantly relax timing constraints, performing the thermometer-to-binary conversion and binary accumulation still presented a bottleneck. As a result, the 0.13 μm prototype required a more power-intensive pseudo NMOS implementation for these digital blocks in order to have sufficient timing margins. Although simulations indicated that future technology nodes (i.e., 90nm, 65nm) could perform the necessary computation with full-swing static logic, the ability to increase the DWA beyond 4-bit and/or increase the sample rate beyond 900 MHz using the proposed architecture could still be a major challenge, despite the benefits of scaling.

With these issues in mind, the first half of this chapter will suggest improvements

to the proposed architecture that will extend the converter's resolution to > 13 ENOB. In particular, a more linear DAC structure that eliminates ISI code-dependency will be introduced, as will a faster DWA implementation that shows promise of enabling 5-6 bit DWA using full-swing logic in the 90 nm and 65 nm nodes. The second half of this chapter will discuss how the characteristics of the analog-intensive blocks (opamps, DAC's) of the proposed ADC will scale with technology through a comparative study of the IBM 130nm, 90nm and 65nm nodes. As will be seen in the following analysis, the overall power-efficiency of the architecture will improve with scaling despite the poorer analog characteristics of devices in future nodes.

5.1 Architectural Improvements

5.1.1 A Lower ISI DAC Topology

As discussed earlier in this thesis, transient mismatches (ISI) in the main NRZ feedback DAC generate distortion tones in the ADC output spectrum due to the signal dependency of the ISI error. This was confirmed both in behavioral simulation and in measurements, and suggested that a more linear DAC structure was needed for the converter to achieve its true SNR-limited resolution. While the RZ DAC could generate waveforms that were robust to ISI, it was highly sensitive to clock jitter and presented large pulsing transients to the inputs of the opamp integrator, exacerbating the impact of amplifier non-linearity and finite gain-bandwidth.

Fortunately, a simple yet highly linear DAC structure that is robust to ISI error was proposed in [2], and is shown in Figure 5-1. This dual return-to-zero (DRZ) DAC structure breaks the signal dependency of ISI errors in the NRZ DAC by forcing all switching devices to transition during each sample period. Indeed, the output waveform generated by the DRZ DAC essentially mimics two time-interleaved RZ DAC waveforms, which when summed together, resemble the equivalent NRZ waveform, but with the RZ switching transients evident at the rising and falling edges of the clock.

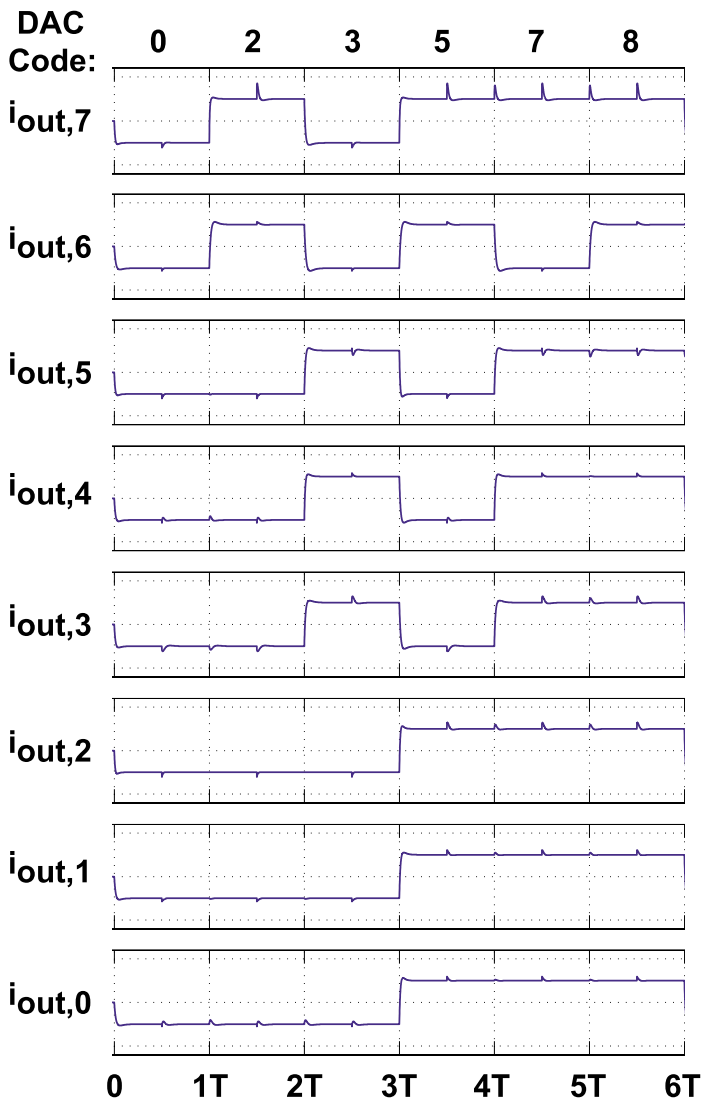


Figure 5-1: behavioral simulated waveforms of a 3-bit DRZ DAC. Note that since all switching devices experience a constant transition density, the DRZ DAC does not exhibit any code-dependent ISI.

The resemblance of the DRZ DAC's output waveform to that of an NRZ carries additional benefits. First the DRZ output waveform is more continuous than the RZ waveform, and therefore will enable opamp unity-gain bandwidth and settling specifications similar to those in an NRZ DAC-based implementation. Secondly, the DRZ DAC waveform will benefit from the same clock-jitter rejection that the NRZ DAC enjoys, since jitter will only affect the LSB's in the DAC code that differ from sample to sample.

The only significant penalty of the DRZ scheme is the doubling of the bandwidths of the DAC switching waveforms, which require fast latching and reset signals. Furthermore, perturbations on the tail node of the DAC unit element must be minimized since the settling time of a large disturbance can easily exceed the half-sample period of the DRZ waveform. Fortunately, such disturbances can be greatly minimized by designing the DAC switching waveforms to have a strong pull-up edge and slower pull-down edge, as was discussed earlier in this thesis.

The complete DRZ DAC signal path is shown in Figure 5-2, and plots generated from transistor-level simulations of the unit element output current and latch switching waveforms are shown in Figure 5-3. As was the case for the NRZ DAC, circuitry is needed to retime the DAC waveform as well as to generate the differential outputs to drive the DAC switching devices. But unlike the differential flip-flop structure used in the NRZ DAC, the DRZ latch has four outputs to drive the four inputs of the DRZ DAC unit element. Furthermore, a given differential output pair must alternately latch the input data and reset itself depending on the phase of the clock signal. Consequently, a slightly more sophisticated latch structure is required.

The impact of ISI on the DRZ DAC can be easily quantified through behavioral simulation. The behavioral model for the DRZ DAC is shown in Figures 5-4, 5-5 and 5-6, and comprises N-sets of 8 filters to describe the different rise/fall transients for each switch in the two differential pairs of an N-element current-steering DRZ DAC. While all filters share the same nominal frequency response, the exact pole/zero locations for each filter are purposely varied in a Monte Carlo fashion. Consequently, each filter exhibits different switching transients with variable amounts of peaking

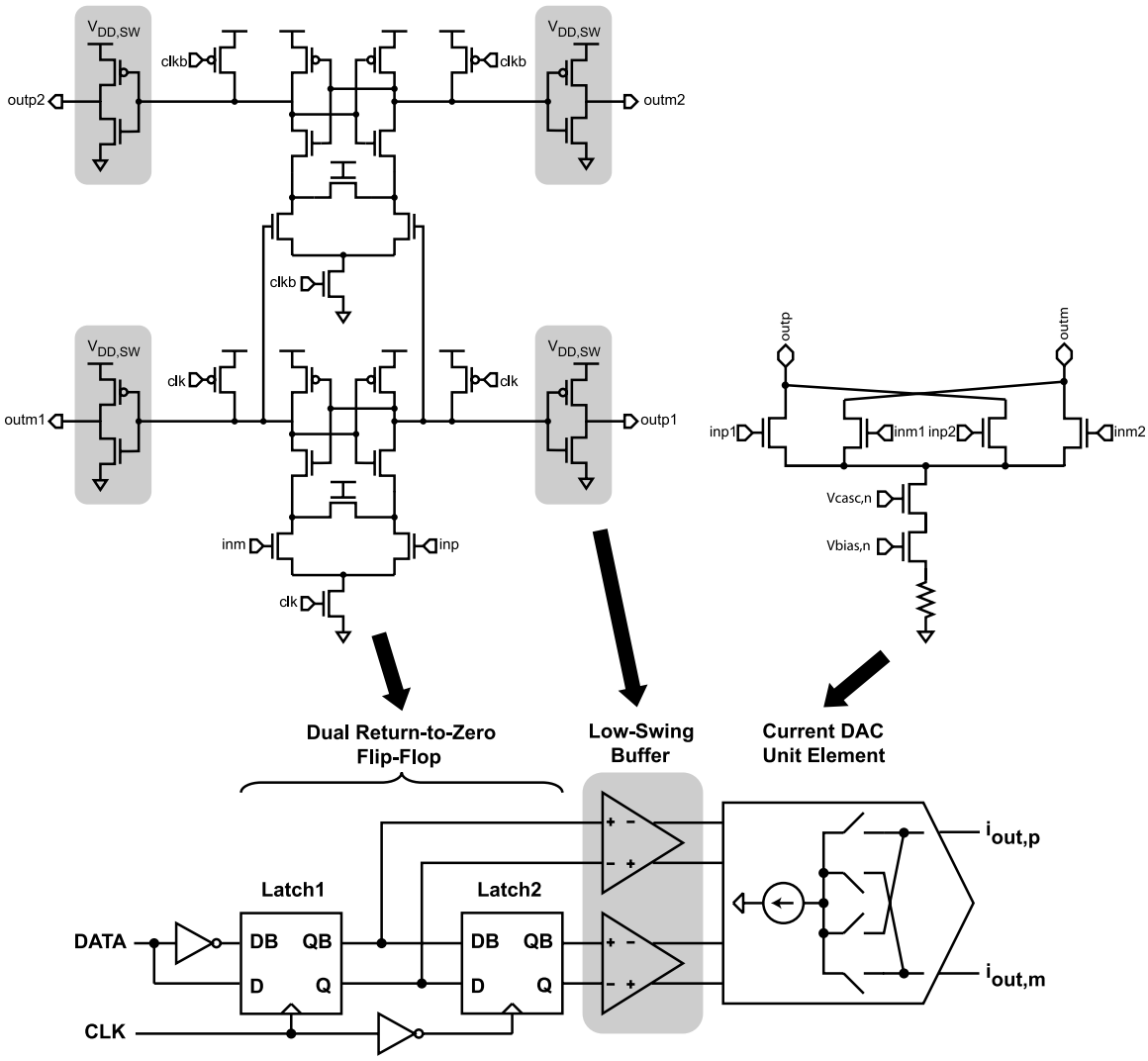


Figure 5-2: the DRZ DAC signal path and key circuit blocks.

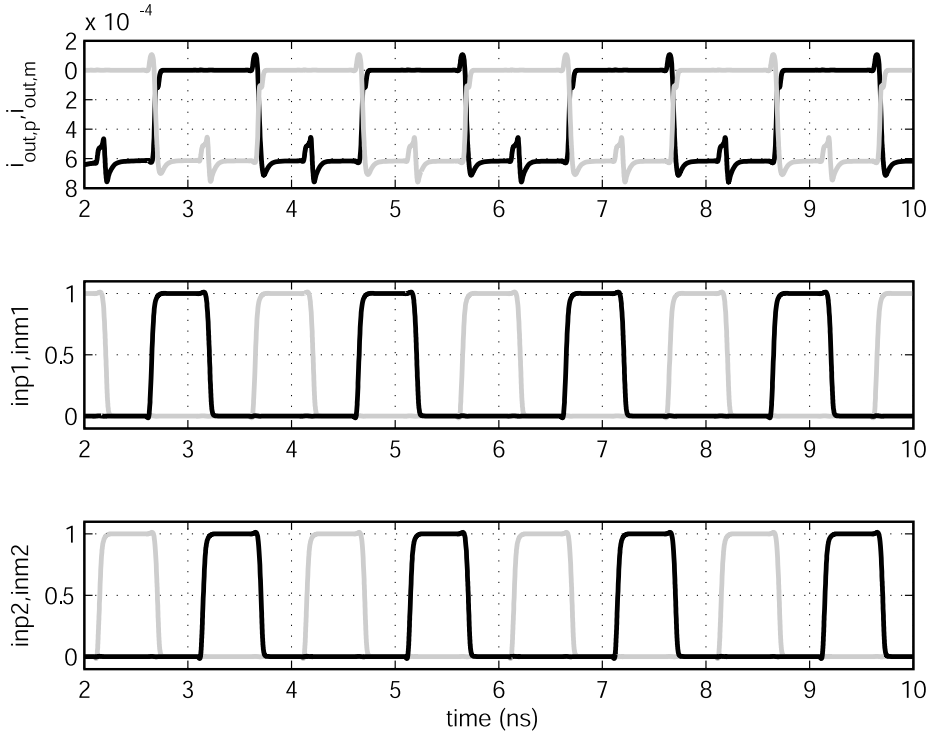


Figure 5-3: transistor-level simulated switching waveforms of 1 unit-element in the DRZ DAC.

(i.e., clock/data feedthrough and charge injection).

The improvement in linearity afforded by the DRZ structure can be appreciated with the help of Table 5.1. Here, Monte-Carlo simulations of the prototype ADC architecture implemented with a NRZ DAC and a DRZ DAC are performed assuming transient mismatches of $1\sigma_{mm,tran} = 3\%, 4\%$, and 5%. As can be seen from the table, the DRZ signaling scheme enables the converter to achieve an average SNDR of greater than 80 dB consistently. Furthermore, the DRZ enables a much smaller variation in the SNDR values compared to a NRZ implementation.

	$1\sigma_{mm,tran} = 3\%$		$1\sigma_{mm,tran} = 4\%$		$1\sigma_{mm,tran} = 5\%$	
Parameter	NRZ	DRZ	NRZ	DRZ	NRZ	DRZ
μ_{SNR} (dB)	82.9	83.0	83.1	82.6	81.5	82.4
σ_{SNR} (dB)	3.9	1.1	1.7	2.2	2.1	1.6
μ_{SNDR} (dB)	78.3	81.9	76.7	81.4	76.0	81.4
σ_{SNDR} (dB)	3.8	1.0	3.0	2.1	3.1	1.8

Table 5.1: simulated SNR and SNDR average and standard deviation assuming an NRZ/DRZ DAC implementation with $1\sigma_{mm,tran} = 3\%, 4\%$, and 5%.

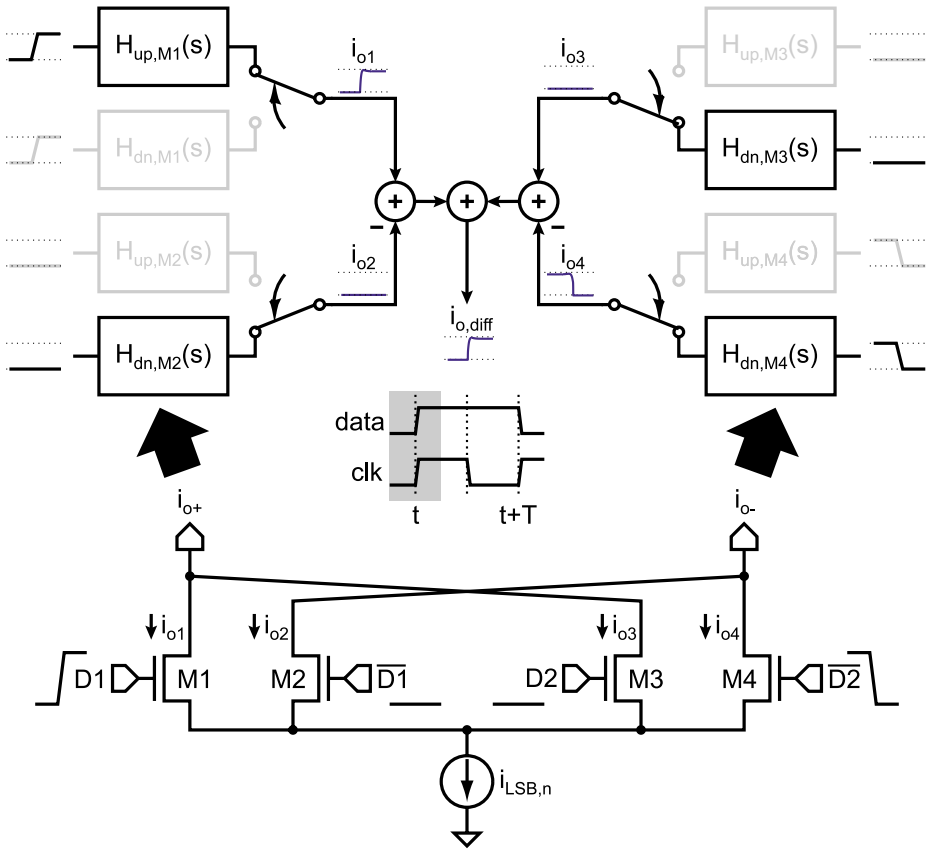


Figure 5-4: ISI model for one unit element of an N-element DRZ DAC depicting a "0" to "1" transition at the rising edge of clock.

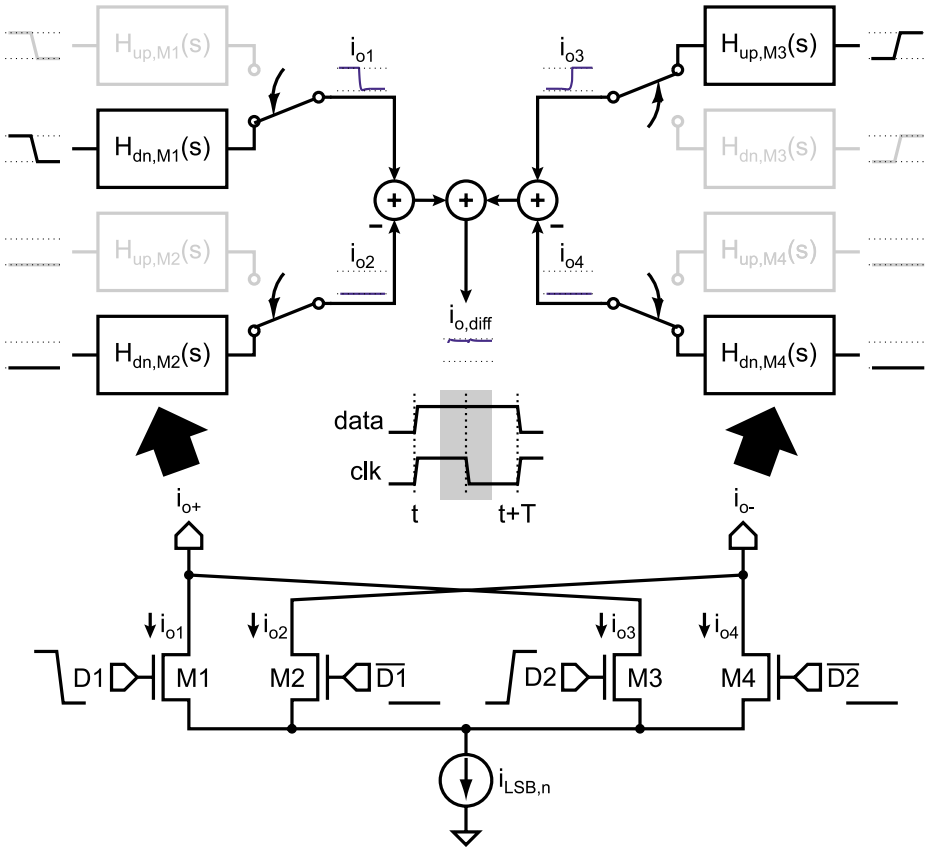


Figure 5-5: ISI model for one unit element of an N-element DRZ DAC depicting the passing of the "1" value from the first switching pair (M1,M2) to the second switching pair (M3,M4).

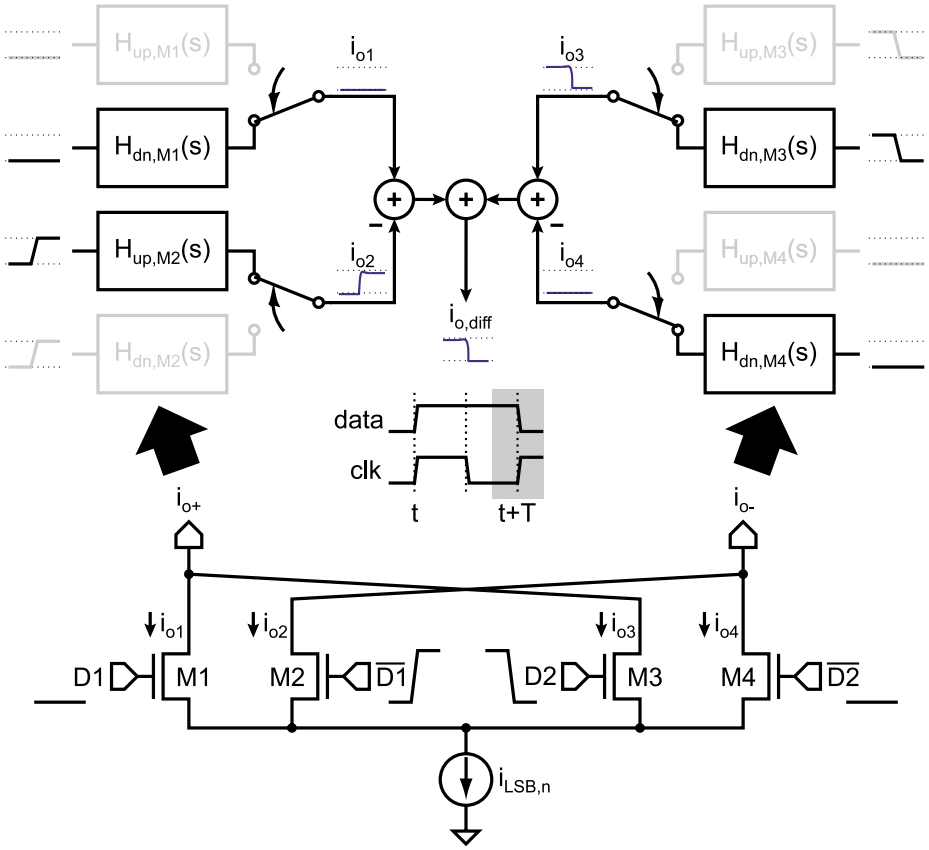


Figure 5-6: ISI model for one unit element of an N-element DRZ DAC depicting a "1" to "0" transition at the next rising edge of clock.

5.1.2 Going Beyond a 4-bit Quantizer/DAC

The previous section demonstrated that the DRZ DAC was robust to ISI, enabling the prototype ADC architecture to achieve close to ideal SNR-limited resolution (13 ENOB). However, for the given architecture to achieve higher resolution, the quantization noise floor must be lowered further. This can be accomplished by increasing the number of bits in the quantizer/DAC. Of course, this carries the penalty of a more complicated DWA structure that may not meet timing for the given sample rate if implemented as described earlier in this thesis. Fortunately, efforts in developing this thesis have engendered new ideas for faster DWA implementations. Indeed, the next section will show that even 6-bit DWA using full-swing logic may be possible in the next technology node.

Table 5.2 shows the simulated SNR and SNDR average and standard deviation assuming a 4-bit and 5-bit quantizer/DAC implementation for the proposed ADC architecture. The simulated results are further separated according to the specific DAC structure (NRZ or DRZ) to quantify the architecture's sensitivity to ISI. It is assumed in these simulations that the unit element and transient mismatches for the DAC's are the same as those for the implemented 4-bit prototype ADC.

	4-bit		5-bit	
Parameter	NRZ	DRZ	NRZ	DRZ
μ_{SNR} (dB)	82.9	83.0	87.0	86.9
σ_{SNR} (dB)	3.9	1.1	0.6	0.5
μ_{SNDR} (dB)	78.3	81.9	82.6	85.8
σ_{SNDR} (dB)	3.8	1.0	3.9	0.4

Table 5.2: simulated SNR and SNDR average and standard deviation assuming a 4-bit and 5-bit quantizer and NRZ/DRZ DAC.

As the simulations show, close to 14 ENOB can be obtained with a 5-bit quantizer and DRZ DAC implementation. Furthermore, the advantage of using the DRZ signaling scheme over NRZ is clear, as it improves the SNDR by 1.3 dB and reduces the variation in SNDR by more than a factor of 2. The next section now concerns implementing a more timing efficient DWA architecture that can enable scaling of the quantizer/DAC bits to achieve higher resolution.

5.1.3 A Faster DWA Implementation

While scaling enables faster digital gates, the DWA implementation proposed earlier in this thesis suffers from a rapidly growing gate delay in the thermometer-to-binary converter and binary accumulator as the number of quantization bits increases (see Table 5.3). Consequently, while scaling the proposed 4-bit DWA implementation to 90 nm enables the use of full-swing logic, a 5-bit DWA implementation using full-swing logic may not be possible unless the design is scaled to the 65 nm node. At the same time, if the sample rate is increased further, performing 5-bit DWA using full-swing logic in 65 nm may no longer be feasible. Consequently, a more timing efficient DWA implementation that better leverages the benefits of scaling is desirable.

	4-bit			5-bit			6-bit		
Number of Gates	15			21			28		
0 (nm)	65	90	130	65	90	130	65	90	130
Estimated t_{pd} (ps)	450	600	750	630	840	1050	840	1120	1400

Table 5.3: estimated propagation delay of the thermometer-to-binary converter and binary accumulator for different number of bits, assuming the implementation as proposed in the prototype ADC. A conservative estimate for the full-swing CMOS XOR/XNOR gate delays in the 65 nm, 90 nm, and 130 nm technologies are determined to be 30 ps, 40 ps, and 50 ps, respectively.

The proposed DWA architecture with greater timing efficiency is shown in Figure 5-7. Note that for simplicity, a 3-bit implementation is shown, though the ultimate purpose is to scale this architecture up to 4, 5, or even 6 bits, depending on the technology and the sample rate. The key innovation in this architecture is to eliminate the thermometer-to-binary converter and binary accumulator from the DWA feedback path by having the barrel shift accumulate the thermometer encoded DWA pointer. Since the DWA will unidirectionally rotate through the unit elements, simple logic can compare adjacent thermometer code bits to determine where the current DWA code has ended (denoted by the juxtaposition of a 1,0 transition), and therefore where the next DWA code should begin. As long as the input to the DWA is greater than or equal to 1, the logic will correctly determine where the transition has occurred in the thermometer code, enabling the equivalent binary code to be easily determined with

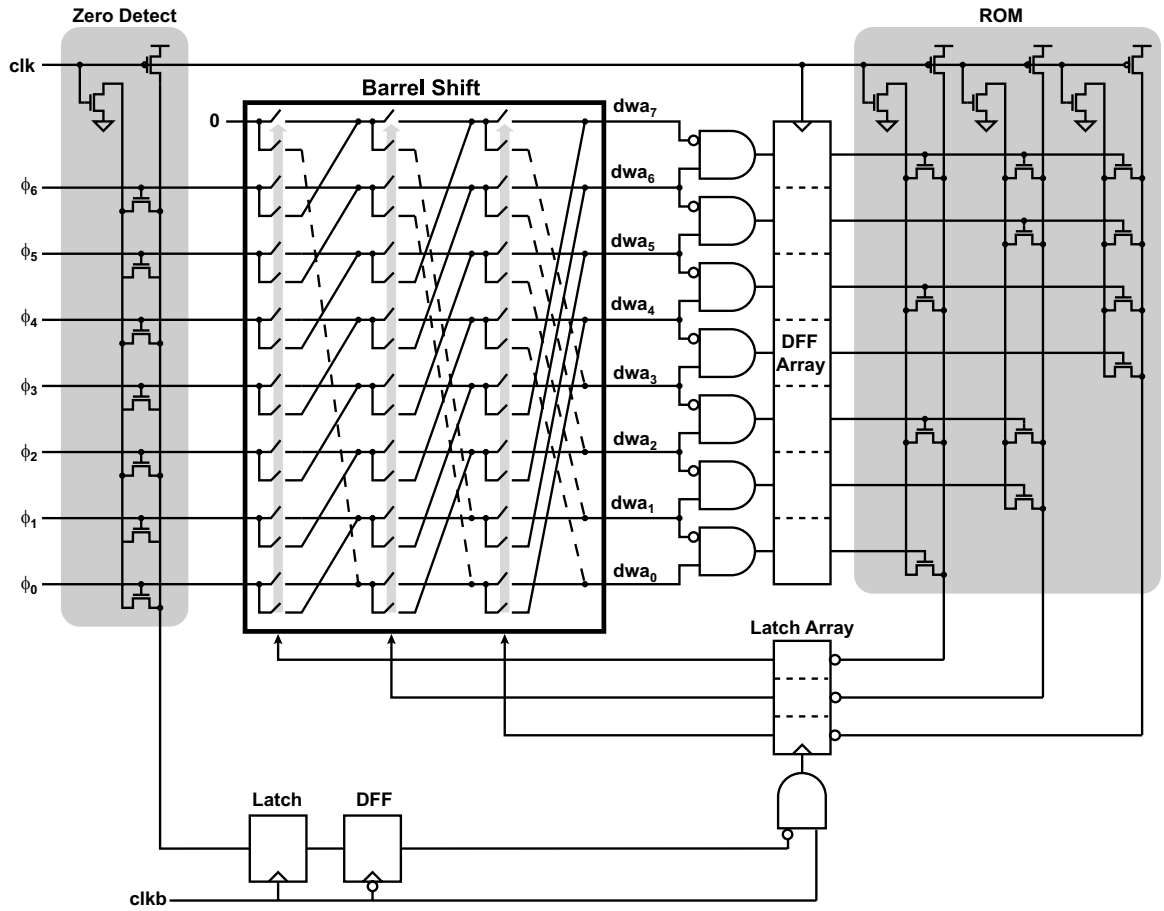


Figure 5-7: the proposed timing efficient DWA implementation.

a simple ROM. The resulting binary code then controls the barrel shift to generate the next DWA code.

While the ROM could be implemented using a resistive pull up, such an implementation would dissipate static power. Instead, a lower-power dynamic ROM that calculates the binary code during the high phase of clock, and resets the outputs during the low phase of clock can be implemented. Latches that are transparent during the high phase of clock, but latch during the low phase of clock can then be used to hold the calculated binary code during the ROM reset. Note that if a zero input thermometer code is fed into the barrel shift, the transition detecting logic should not update the pointer. However, the implementation in Figure 5-7 will attempt to reset the barrel shift control signal to zero, resulting in a loss of the first-order noise-shaping DWA sequence. To prevent that from happening, a zero detecting circuit is leveraged to gate the clock signal to the latch array, such that the DWA pointer is preserved.

Interestingly, the timing constraint for the path from the VCO quantizer and phase detector logic output through the barrel shift to the retiming DAC latches is the same as it was in the prototype ADC:

$$t_{pd,bs} < T - t_{clk2q} - t_{pd,det} - t_{sh,dac} \tag{5.1}$$

where $t_{pd,bs}$ is the propagation through the barrel shift, t_{clk2q} is the clock-to-Q delay of the VCO quantizer, $t_{pd,det}$ is the propagation delay through the phase detection logic, and $t_{sh,dac}$ is the setup-and-hold time of the DAC retiming latch. A similar timing constraint concerns the timing path from the VCO quantizer and phase detector logic through the barrel shift and the transition detecting logic to the DFF array:

$$t_{pd,bs} < T - t_{clk2q} - t_{pd,det} - t_{pd,logic} - t_{sh,dff} \tag{5.2}$$

where $t_{pd,logic}$ is the propagation delay through the transition detecting logic, and $t_{sh,dff}$ is the setup-and-hold time of the D-flop-flop array. Practically speaking, the timing constraints of Equations 5.1 and 5.2 are almost identical. The timing bottle-

neck in the proposed DWA architecture occurs in the DWA feedback path:

$$t_{pd,bs} < T - t_{pd,rom} - t_{pd,lat} - t_{pd,lat2bs} - t_{pd,logic} \tag{5.3}$$

where $t_{clk2q,dff}$ is the clock-to-Q delay of the DFF array, and $t_{pd,rom}$, $t_{pd,lat}$, and $t_{pd,lat2bs}$ are the propagation delays of the ROM, latch, and latch-to-barrel shift, respectively. Extracted simulations from the prototype ADC suggest that:

$$t_{pd,lat} + t_{pd,lat2bs} \approx t_{clk2q} + t_{pd,det} \tag{5.4}$$

Consequently, the excess timing penalty encountered in the DWA feedback path is primarily due to the ROM propagation delay ($t_{pd,rom}$). Indeed, the key design challenge in this DWA architecture concerns how fast of a ROM can be built. Nevertheless, this ROM timing constraint will be significantly easier to meet that that of an N-bit adder and accumulator.

5.2 Scaling of the Proposed Architecture in Future Technology Nodes

5.2.1 Impact of Scaling on Opamp Design

A key challenge in scaling the proposed CT $\Delta\Sigma$ ADC architecture concerns the ease with which opamps can be designed in future technology nodes. Indeed, previous chapters showed that the opamps consumed the majority of the analog power ($>$ 70%), which was necessary to achieve wide unity-gain bandwidths ($>$ 3.5 GHz) and low input-referred noise ($< 6e^{-18}V^2/Hz$).

Fortunately, some improvements can be made to the opamp topology that would enable potentially lower noise and wider unity-gain bandwidths. The suggested topology, shown in Figure 5-8, leverages PMOS's as the input devices due to their lower flicker noise, and utilizes a class AB output stage to push the opamp parasitic poles to higher frequency. This latter benefit is possible since:

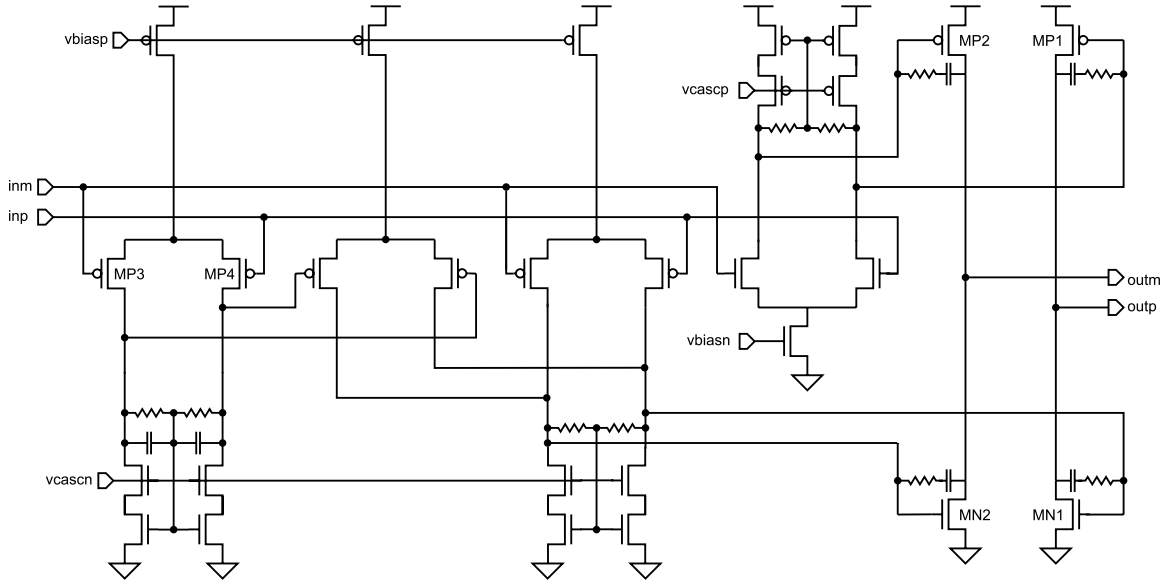


Figure 5-8: schematic of a 3-stage nested Miller opamp with PMOS input devices for lower flicker noise, and a class AB output stage for higher unity-gain bandwidth .

$$f_{par} \approx \frac{g_{m,MN1} + g_{m,MP1}}{2\pi C_L} \tag{5.5}$$

That is, the class AB output stage effectively allows for a doubling of the output transconductance for a given bias current compared to the class A stage, leading to greater power efficiency.

Using this improved topology, the opamp power dissipation in other technology nodes can now be estimated. For simplicity, the following assumptions are made in all the presented transistor-level simulation results:

1. Only the power of the input and output devices are considered

2. The device length is $1.5 \times L_{min}$ for the input devices, but is equal to L_{min} for the output devices

3. The desired noise performance for the main PMOS input devices (MP3, MP4) is $6e^{-11}V^2$ in a 20 MHz bandwidth

4. The desired parasitic pole frequency is $\geq$ 8 GHz

The first assumption serves a practical purpose in that the power dissipation of the intermediate stages is typically a fraction ($< 50\%$) of the power of the input and output stages. At the same time, the number of stages will depend on the desired opamp DC gain as well as the intrinsic gain of the transistors in a given technology. The second assumption is based on the observation that the simulated transistor flicker noise in a given technology reduces by a substantial amount when the minimum device length is increased by just 50%. Longer devices are permissible since the input stages are designed to have low-frequency dominant poles and therefore do not need to operate as quickly as the output stage. However, since the noise contribution of the output stage is negligible, minimum device lengths are used for the higher device f_T. The desired noise specification in the third assumption is simply half of the simulated noise of the first opamp integrator in the prototype ADC. In that design, it was found that the total opamp noise tended to be approximately twice that of the main input devices. The final assumption is based on the behavioral modeling of the opamp, which showed that the parasitic poles needed to be at least 7-8 GHz for the nested Miller amplifier to achieve a 4 GHz unity-gain bandwidth with adequate phase margin.

	65 nm			90 nm			130 nm		
$\left(\frac{W}{L}\right)_{P,in}$	30	60	90	30	60	90	30	60	90
Area (μm^2)	48.48	50.76	55.61	42.65	53.58	67.25	142.59	246.40	349.07
C_{gate} (fF)	354	356	380	373	444	710	437	710	970
$g_m r_o$	13.1	12.3	11.9	19.1	18.7	18.2	13.2	12.8	12.6
$I_{bias,in}$ (mA)	1.70	0.89	0.65	0.78	0.49	0.41	1.25	1.08	1.02

Table 5.4: device area and power needed to achieve desired noise performance of $3e^{-11}V^2$ in IBM's 130 nm, 90 nm, and 65 nm technologies ($L = 1.5 \times L_{min}$) for a multi-fingered PMOS with different aspect ratios, $\left(\frac{W}{L}\right)_{P,in}$. The corresponding gate capacitance and transistor intrinsic gain for each of these points are also quoted.

Table 5.4 details the device area and power needed to achieve the desired noise performance in IBM's 130 nm, 90 nm, and 65 nm technologies assuming a multi-

fingered PMOS with three different aspect ratios: $\left(\frac{W}{L}_{P,in}\right) = 30, 60$ and 90. As expected, a device with a larger aspect ratio results in a larger transconductance and lower input-referred noise. Consequently, fewer fingers and less bias current are needed to achieve the desired noise specification, though at the price of a larger gate capacitance, which effectively loads the class AB output stage. To maintain the desired unity-gain bandwidth, the class AB output stage will have to dissipate more power, thus highlighting a unique tradeoff in the power consumption of the input and output stages. As will be seen shortly, this tradeoff is not necessarily one-for-one, and enables some degree of optimization in the amplifier's design.

Finally, note that Table 5.4 also quotes the intrinsic gain ($g_m r_o$) of the transistors to provide some insight on the number of stages needed to achieve a desired DC gain. Cascoding can be used to boost the output impedances of a given gain stage, as was done in Figure 5-8. Nevertheless, a feed-forward path in parallel with a given gain stage will in general degrade the total impedance, resulting in a lower intrinsic gain. Consequently, to achieve a DC gain of at least 1000, four gain stages may be necessary in the 65 nm and 130 nm nodes, while three gain stages may be sufficient in the 90 nm node.

	65 nm			90 nm			130 nm		
$\left(\frac{W}{L}\right)_{P,in}$	30	60	90	30	60	90	30	60	90
C_L (fF)	825	827	856	848	933	1050	925	1250	1570
$g_{m,tot}$ (mS)	41.5	41.6	43.0	42.6	46.9	52.8	46.5	62.8	78.9
Area (μm^2)	20.28	20.45	20.96	40.18	44.06	49.57	87.88	118.98	149.40
$I_{bias,o}$ (mA)	1.20	1.21	1.24	1.24	1.36	1.53	1.30	1.76	2.21

Table 5.5: NMOS and PMOS device area and power needed to achieve parasitic pole frequency of 8 GHz in IBM's 130 nm, 90 nm, and 65 nm technologies ($L = L_{min}$) assuming different input device aspect ratios $\left(\frac{W}{L}\right)_{P,in}$. Note that the aspect ratios of the multi-finger output devices are fixed: $\left(\frac{W}{L}\right)_{N,o} = 10$ and $\left(\frac{W}{L}\right)_{P,o} = 30$

Power and area estimates for the class AB output stage in each of the technology nodes are shown in Table 5.5. In these simulations, the number of fingers and the applied bias current to the NMOS/PMOS ($L = L_{min}$, $\left(\frac{W}{L}\right)_{MN1} = 10$, $\left(\frac{W}{L}\right)_{MP1} = 30$)

are scaled such that their total transconductance will be large enough to move the parasitic pole to the desired frequency f_{par} (8 GHz). In other words, the area and power are scaled such that:

$$g_{m,tot} = g_{m,MN1} + g_{m,MP1} = 2\pi f_{par} C_L \tag{5.6}$$

As previously mentioned, the total load capacitance depends on the total input device capacitance as well as any other device and wiring capacitances from a DAC tied to the opamp inputs. The opamp design in the prototype ADC found that a conservative estimate for the total gate capacitance was approximately 1.2 times that of the first stage input device (though this factor will scale with the actual number of gain stages in the nested Miller amplifier). Furthermore, the DAC design and extracted layout revealed that a conservative estimate for its device and wiring capacitances was roughly 400 fF. Consequently, the total load capacitance can be approximated as:

$$C_L \approx 1.2 \times C_{gate,1^{st}} + 400fF \tag{5.7}$$

The total bias current needed for the input device and the class AB output devices, as well as the relative breakdown between the two stages, is shown in Table 5.6. The aspect ratio that yields the lowest power dissipation for a given technology node is in boldface text. Note that the quoted total bias current ($I_{bias,tot}$) is twice the sum of the input and output stage currents to account for the differential input and output of the amplifier. Also note that for simplicity this total does not include estimates of the power of the intermediate stages.

As can be seen from the results in Table 5.6, amplifiers designed in the more deeply scaled technologies (i.e., 65 nm and 90 nm) are more power efficient when the input device aspect ratios are increased since the input stage bias current needed to achieve the noise specification decreases proportionately. Although the larger aspect ratios carry the penalty of an increased load capacitance to the output stage, it is still smaller than the gate capacitance of a $0.13\mu m$ device with an equivalent aspect ratio.

	65 nm			90 nm			130 nm		
$\left(\frac{W}{L}\right)_{P,in}$	30	60	**90**	30	**60**	90	**30**	60	90
$I_{bias,in}$ (mA)	1.70	0.89	**0.65**	0.78	**0.49**	0.41	**1.25**	1.08	1.02
$I_{bias,o}$ (mA)	1.20	1.21	**1.24**	1.24	**1.36**	1.53	**1.3**	1.76	2.21
$I_{bias,tot}$ (mA)	5.80	4.18	**3.78**	4.04	**3.70**	3.88	**5.10**	5.68	6.46

Table 5.6: the bias current required for the input PMOS device ($I_{bias,inp}$), the output class AB NMOS/PMOS devices ($I_{bias,o}$), and the corresponding total ($I_{bias,tot}$). Note that these currents are for one side of a differential pair/path, and therefore, the total current will be at least twice the amount shown. Also note that the currents for the intermediate stages of the nested Miller amplifier are not included in this analysis.

Consequently, the amount of power needed to be dissipated by the class AB stage is substantially lower for the deeply scaled technologies, resulting in a net power savings. Recall that these bias current numbers were calculated assuming a fixed DAC/wiring capacitance. In reality, scaling the DAC design will enable the use of even smaller switching devices for the given DAC current, reducing the effective device capacitance. Thus, additional amplifier power savings may be possible when the scaling of the DAC parasitics are also taken into account.

A graphical view of the preceding analysis that considers additional input device aspect ratios is shown in Figure 5-9. These trend lines further support the notion that for a given noise and unity-gain bandwidth specification, the power efficiency of the nested Miller amplifier improves as the CMOS technology scales to the 90 nm and 65 nm nodes, compared to the 130 nm node.

As a final note, it is important to remember that the bias current calculations presented here do not consider the slew-rate requirements of the amplifier. Assuming a main feedback DAC current of 10 mA, and a 16-element DAC implementation (as was the case in the prototype ADC), a 1-LSB change in the DAC output will necessitate that the amplifier instantaneously supply 625 μA of current. Simulations show that the DAC output can change by as much as 3 LSB's (1.875 mA) in normal operation. Consequently, simulations must be performed to verify that the output

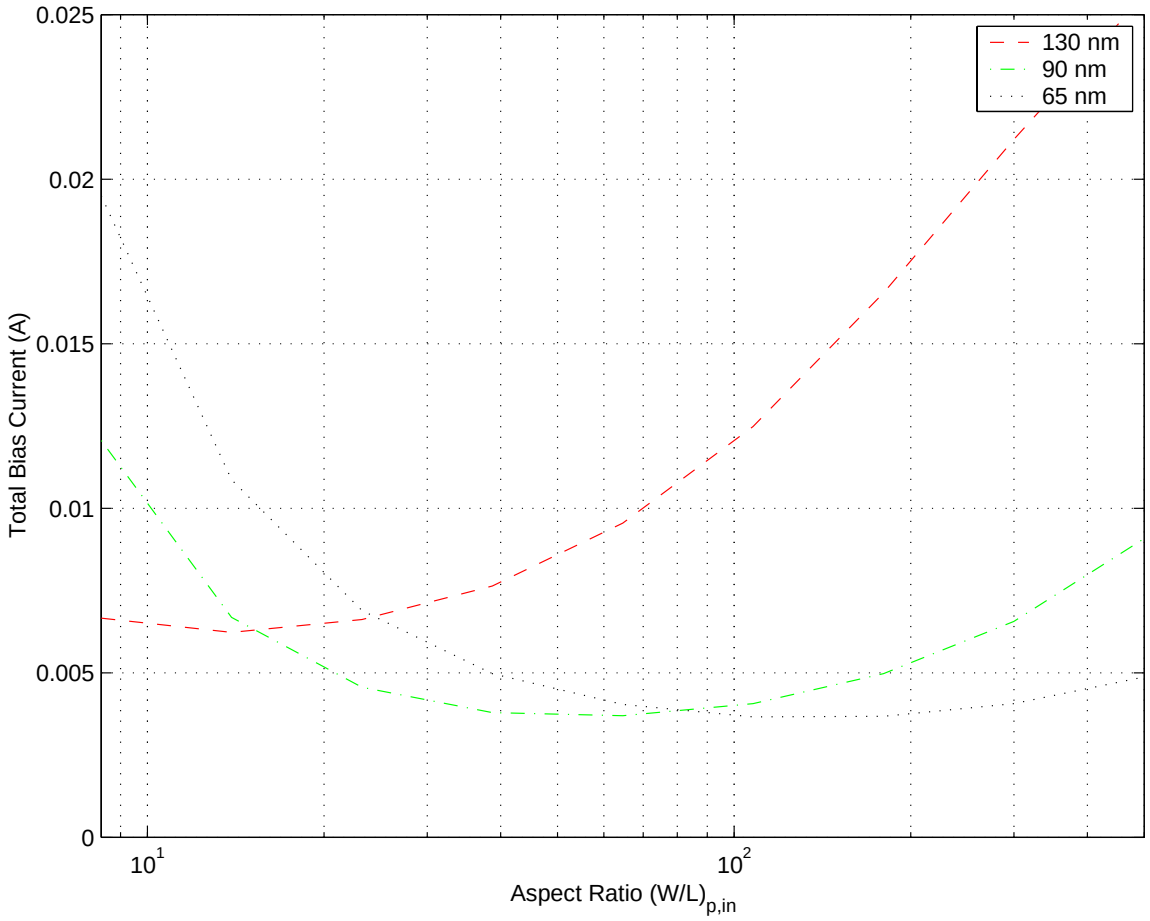


Figure 5-9: amplifier power dissipation as a function of the aspect ratio of the input PMOS devices.

stage bias current is sufficiently large to ensure linear settling during normal operation.

5.2.2 Impact of Scaling on DAC Design

As was mentioned earlier in this thesis, the effect of finite DAC output resistance can largely be ignored when the unit-element output resistance exceeds 30 kΩ. When scaling the DAC design in future technology nodes, the ultimate issue that must be considered is how easily the minimum output resistance target can be met while still meeting the DAC's strict noise benchmark.

Length	R_{out} (kΩ)	Area (μm^2)	σ_{mm} (%)
	65 nm		
L_{min}	66	576	1.40
$1.5 \times L_{min}$	162	756	0.42
$2.0 \times L_{min}$	238	928	0.35
	90 nm		
L_{min}	114	594	2.08
$1.5 \times L_{min}$	220	1152	0.27
$2.0 \times L_{min}$	263	1557	0.22
	130 nm		
L_{min}	146	1290	1.10
$1.5 \times L_{min}$	300	1037	0.65
$2.0 \times L_{min}$	375	922	0.46

Table 5.7: simulated DAC unit-element output resistances, device area, and mismatch in IBM's 65 nm, 90nm, and 130 nm nodes, assuming a gate length of $L = L_{min}, 1.5 \times L_{min}$, and $2 \times L_{min}$.

To that end, the implemented topology for the main feedback DAC was simulated in IBM's 65nm, 90nm and 130nm technologies (see Table 5.7). While maintaining aspect ratios similar to those in the prototype ADC, the number of parallel devices (or fingers) were swept until they met the specified noise target, and the output resistance, total device area, and mismatch quoted at this point. Note that the total device area is quoted for all 16 unit elements and assumes the cascoded structure with resistive degeneration. Also note that the simulations for the 65nm and 90nm implementation assume a 1.2 V supply ($V_{CM} = 0.6V$), while the 130nm node simulation assumes a 1.5 V supply ($V_{CM} = 0.75V$). The power supply assumptions for the 90nm and 65nm

are merited as the majority of recently published high performance ADC's fabricated in these technologies still operate on a 1.2 V supply to relax headroom constraints [8, 43, 54, 53, 9].

As the simulation results show, even minimum length devices in any of the technology nodes will be able to meet the minimum target output resistance of 30 kΩ, which suggests that the scaled DAC topology will not require fundamental changes. However, there still is an advantage to using non-minimum device lengths, aside from the increase in nominal output resistance. As shown in the last column of Table 5.7, using a 50% larger gate length enables the unit-element mismatch to fall below 1% in every technology node, with even longer gate lengths exhibiting a greater degree of matching. Notice, however, that this high degree of matching is largely due to the degeneration resistors in the DAC unit element. Indeed, if a DAC structure without the resistive degeneration were adopted, the unit element mismatch could easily approach 3-4%, even if the gate length were a factor of two larger than the minimum length.

Chapter 6

Conclusion

In this thesis, a new VCO-based ADC architecture that avoided signal distortion issues that had limited the resolution of previously published VCO-based ADC's was demonstrated. A key contribution of this work was the discovery that directly leveraging the VCO's quantized phase precluded the need to span the entire non-linear voltage-to-frequency (K_v) characteristic. Instead, small deviations at the VCO's input could shift the output phase substantially, enabling the entire dynamic range of this VCO integrator and quantizer to be exercised without incurring serious distortion. Through the example of a 1^{st}-order CT $\Delta\Sigma$, it was shown that the proposed *voltage-to-phase* VCO-based ADC nearly eliminated the distortion that had riddled prior *voltage-to-frequency* VCO-based ADC's, enabling ideal SNR-limited resolution.

To show the viability of the proposed VCO-based ADC in high-performance communications applications, a prototype 4^{th}-order CT $\Delta\Sigma$ ADC leveraging the VCO as an integrator and quantizer was implemented in a $0.13\mu m$ CMOS technology, and achieved approximately 13 ENOB (78.1 dB SNDR, 81.2 dB SNR) in 20 MHz of signal bandwidth while consuming 87 mW from a 1.5V supply. The prototype also included a scheme for performing DEM on *all* feedback DAC's, an essential contribution that enabled the proposed architecture to achieve $>$ 12 ENOB.

A third major contribution of this thesis was the behavioral model developed to analyze the proposed ADC architecture, as well as to determine its robustness to circuit non-idealities. Through this effort, it was discovered that the proposed

architecture's primary limitation to achieving > 13 ENOB performance was mismatch and ISI in the main NRZ feedback DAC. At the same time, behavioral modeling of the opamp's non-linearity revealed that the amplifiers needed to achieve a higher unity-gain bandwidth than predicted by a simple linear opamp model in order suppress quantization noise folding effects.

The final major contribution of this thesis involved the analysis of a more linear DAC structure through behavioral simulation, which found that the Dual Return-to-Zero (DRZ) DAC [2] could significantly reduce distortion caused by code dependent ISI errors, enabling close to ideal SNR-limited resolution. At the same time, a new DWA algorithm that has the potential to increase the number of bits processed in the same sample period while using full-swing logic was also described. Indeed, both of these architectural changes suggest that the proposed VCO-based ADC architecture can be modified easily to achieve close to 14 ENOB performance.

Bibliography

[1] R. Adams, K. Nguyen, and K. Sweetland. A 113-dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling. *IEEE J. of Solid-State Circuits*, 33(12):1871–1878, December 1998.

[2] R. Adams, K.Q. Nguyen, and K. Sweetland. A 113-dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling. *IEEE J. of Solid-State Circuits*, 33(12):1871–1878, December 1998.

[3] E. Alon, V. Stojanovic, and M. A. Horowitz. Circuits and Techniques for High Resolution Measurement of On-Chip Power Supply Noise. *IEEE J. Solid-State Circuits*, 40(4):820–828, April 2005.

[4] H. Alzaher, H. Elwan, and M. Ismail. A CMOS Highly Linear Channel-Select Filter for 3G Multistandard Integrated Wireless Receivers. *IEEE J. Solid-State Circuits*, 37(1):27, January 2002.

[5] R. Baird and T. Fiez. Linearity Enhancement of Multibit $\Delta\Sigma$ A/D and D/A Converters using Data Weighted Averaging. *IEEE J. of Solid-State Circuits*, 22(5):899–901, February 1997.

[6] F. Behbahani, A. Karami-Sanjaani, W. Tan, A. Roithmeier, , and A. Abidi. A Broad-Band Tunable CMOS Channel-Select Filter for a Low-IF Wireless Receiver. *IEEE J. Solid-State Circuits*, 35(4):476–489, April 2000.

[7] V. B. Boros. A Digital Proportional Integral and Derivative Feedback Controller for Power Conditioning Equipment. In *IEEE Power Electronics Specialists Conf. Rec.*, 1977.

[8] M. Boulemnakher, E. Andre, J. Roux, and F. Paillardet. A 1.2V 4.5mW 10b 100MS/s Pipeline ADC in a 65nm CMOS. In *IEEE ISSCC Dig. Tech. Papers*, 2008.

[9] L. Breems, R. Rutten, R. Veldhoven, G. Weide, and H. Termeer. A 56mW CT Quadrature Cascaded $\Sigma\Delta$ Modulator with 77dB DR in a Near Zero-IF 20 MHz Band. In *IEEE ISSCC Dig. Tech. Papers*, 2007.

[10] L. Breems, R. Rutten, and G. Wetker. A Cascaded Continuous-Time $\Sigma\Delta$ Modulator With 67-dB Dynamic Range in 10 MHz Bandwidth. *IEEE J. Solid-State Circuits*, 39(12):2152–2160, December 2004.

[11] Z. Cao, Y. Li, and S. Yan. A 0.4 ps-RMS-Jitter 1-3 GHz Ring-Oscillator PLL Using Phase-Noise Preamplification. *IEEE J. Solid-State Circuits*, 43(9):2079–2089, September 2008.

[12] L. Carley. A Noise-Shaping Coder Topology for 15+ Bit Converters. *IEEE J. of Solid-State Circuits*, 24(2):267–273, April 1989.

[13] J. Cherry and W. Snelgrove. Clock Jitter and Quantizer Metastability in Continuous-Time Delta-Sigma Modulators. *IEEE Trans. on Circuits and Systems II*, 46(4):661–676, June 1999.

[14] N. Dalt and C. Sander. A subpicosecond jitter PLL for clock generation in 0.12-μm digital CMOS. *IEEE J. Solid-State Circuits*, 38(7):1275–1278, July 2003.

[15] O. Degani, M. ruberto, E. Cohen, Y. Eilat, B. Jann, F. Cossoy, N. Telzhensky, T. Maimon, G. Normatov, R. Banin, O. Ashkenazi, A. Bassat, S. Zaguri, G. Hara, M. Zajac, E. Shaviv, S. Wail, A. Fridman, R. Lin, and S. Gross. A 1×2 MIMO Multi-Band CMOS Transceiver with an Integrated Front-End in 90nm CMOS for 802.11a/g/n WLAN Applications. In *IEEE ISSCC Dig. Tech. Papers*, 2008.

[16] F. Esfahani, P. Basedau, R. Ryter, and R. Becker. A Fourth-Order Continuous-Time Complex Sigma-Delta ADC for Low-IF GSM and EDGE Receivers. In *IEEE Symp. on VLSI Circ. Dig. Tech. Papers*, 2003.

[17] X. Fan, C. Mishra, and E. Sanchez-Sinencio. Single Miller Capacitor Frequency Compensation Technique for Low-Power Multistage Amplifiers. *IEEE J. of Solid-State Circuits*, 40(3):584–592, March 2005.

[18] I. Galton. Spectral Shaping of Circuit Errors in Digital-to-Analog Converters. *IEEE Trans. On Circuits and Systems II*, 44(10):808–817, October 1997.

[19] F. Gerfers, M. Ortmanns, and P. Schmitz. A transistor-based clock jitter insensitive DAC architecture. In *ISCAS*, 2006.

[20] V. Gopinathan, M. Tarsia, and D. Choi. Design Considerations and Implementation of a Programmable High-Frequency Continuous-Time Filter and Variable-Gain Amplifier in Submicrometer CMOS. *IEEE J. Solid-State Circuits*, 34(12):1698–1707, December 1999.

[21] R. Gu, A. Yee, Y. Xie, and W. Lee. A 6.25GHz 1V LC-PLL in 0.13μm CMOS. In *IEEE ISSCC Dig. Tech. Papers*, 2006.

[22] M. Hovin, A. Olsen, T. Sverre, and C. Toumazou. Delta-Sigma Modulators Using Frequency-Modulated Intermediate Values. *IEEE J. Solid-State Circuits*, 32(1):13–22, January 1997.

[23] C. Hsu, M. Straayer, and M. Perrott. A Low-Noise, Wide-BW 3.6GHz Digital $\Delta\Sigma$ Fractional-N Frequency Synthesizer with a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation. In *IEEE ISSCC Dig. Tech. Papers*, 2008.

[24] J. P. Hurrell, D. C. Pridmore-Brown, and A. H. Silver. Analog-to-Digital Conversion with Unlatched SQUID's. *IEEE Trans. on Electron Devices*, ED-27(10):1887–1896, October 1980.

[25] A. Ismail and A. Abidi. Compact Realization of Active Channel-Select Filters in Wireless Receivers. In *IEEE ISSCC Dig. Tech. Papers*, 2004.

[26] A. Iwata, N. Sakimura, M. Nagata, and T. Morie. The Architecture of Delta Sigma Analog-to-Digital Converters Using a Voltage-Controlled Oscillator as a Multibit Quantizer. *IEEE Trans. On Circuits and Systems II*, 46(7):941–945, July 1999.

[27] J. Jussila, A. Parssinen, and K. Halonen. A Channel Selection Filter for a WCDMA Direct Conversion Receiver. In *IEEE ESSCIRC Dig. Tech. Papers*, 2000.

[28] W. Kester. ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications. http://www.analog.com/.

[29] J. Kim and S. Cho. A Time-Based Analog-to-Digital Converter Using a Multi-Phase Voltage Controlled Oscillator. In *Proc. IEEE Int. Symp. on Circuits and Systems*, 2006.

[30] I. Kipnis, S. Chiu, M. Loyer, J. Carrigan, J. Rapp, P. Johansson adn D. Westberg, and J. Johansson. A 900 MHz UHF RFID Reader Transceiver IC. In *IEEE ISSCC Dig. Tech. Papers*, 2007.

[31] S. Kousai, M. Hamada, R. Ito, and T. Itakura. A 19.7 MHz, 5th Order Active-RC Chebyshev LPF for IEEE802.11n with Automatic Quality Factor Tuning Scheme. In *IEEE ASSCC Dig. Tech. Papers*, 2006.

[32] S. Kousai, D. Miyashita, J. Wadatsumi, A. Maki, T. Sekiguchi, R. Ito, and M. Hamada. A 1.2V 0.2-to-6.3 GHz Transceiver with Less Than -29.5dB EVM@-3dBm and a Choke/Coil-Less Pre-Power Amplifier. In *IEEE ISSCC Dig. Tech. Papers*, 2008.

[33] N. Krishnapura and Y. Tsividis. Dynamically Biased 1-MHz Low-pass Filter with 61 dB Peak SNR and 112 dB Input Range. In *IEEE ISSCC Dig. Tech. Papers*, 2001.

[34] I. Kwon, H. Bang, K. Choi, S. Jeon, S. Jung, Y. Eo, H. Lee, and B. Chung. A Single-Chip CMOS Transceiver for UHF Mobile RFID Reader. In *IEEE ISSCC Dig. Tech. Papers*, 2007.

[35] M. Miller. Multi-Bit Continuous-Time Sigma-Delta ADC. U.S. Patent 6,700,520, March 2004.

[36] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, and E. Romani. A 20 mW 640-MHz CMOS Continuous-Time Sigma-Delta ADC with 20-MHz Signal Bandwidth, 80-dB Dynamic Range, and 12-bit ENOB. *IEEE J. Solid-State Circuits*, 41(12):2641–2649, December 2006.

[37] F. Montaudon, R. Mina, S. Tual, L. Joet, D Saias, R. Hossain, F. Sibille, C. Corre, V. Carrat, E. Chataigner, J. Lajoinie, S. Dedieu, F. Paillardet, and E. Perea. A Scalable 2.4-7.2GHz Wi-Fi/WiMAX Discrete-Time Receiver in 65nm CMOS. In *IEEE ISSCC Dig. Tech. Papers*, 2008.

[38] B. Murmann. ADC Performance Survey 1997-2008. http://www.stanford.edu/ murmann/adcsurvey.html.

[39] R. Naiknaware, H. Tang, and T. S. Fiez. Time-Referenced Single-Path Multi-Bit ADC using a VCO-Based Quantizer. *IEEE Trans. On Circuits and Systems II*, 47(7):596–602, July 2000.

[40] B. Nikolic, V.G. Oklobdzija, V. Stojanovic, W. Jia, J.K.-S. Chiu, and M.M.-T. Leung. Improved Sense-Amplifier Based Flip-Floop: Design and Measurements. *IEEE J. of Solid-State Circuits*, 35(6):876–884, June 2000.

[41] S. Norsworthy, R. Schreier, and G. Temes. Delta-Sigma Data Converters. Wiley blackwell, 1996.

[42] O. Oliaei and H. Aboushady. Jitter Effects in Continuous-Time $\Sigma\Delta$ Modulators with Delayed Return-to-Zero Feedback. In *Proc. of IEEE ICECS*, 1998.

[43] S. Ouzounov, R. Veldhoven, C. Bastiaansen, K. vongehr, R. Wegberg, G. Geelen, L. Breems, and A. Roermund. A 1.2V 121-Mode CT $\Delta\Sigma$ Modulator for Wireless Receivers in 90nm CMOS. In *IEEE ISSCC Dig. Tech. Papers*, 2008.

[44] Y. Palaskas, Y. Tsividis, V. Prodanov, and V. Boccuzzi. A "Divide and Conquer" Technique for Implementing Wide Dynamic Range Continuous-Time Filters. *IEEE J. Solid-State Circuits*, 39(2):297–307, February 2004.

[45] S. Paton, A. Di Giandomenico, L. Hernandez, A. Wiesbauer, T. Potcher, and M. Clara. A 70-mW 300-MHz CMOS Continuous-Time $\Delta\Sigma$ ADC With 15-MHz Bandwidth and 11 Bits of Resolution. *IEEE J. Solid-State Circuits*, 39(7):1056–1063, July 2004.

[46] S. Pavan, Y. Tsividis, and K. Nagaraj. Widely Programmable High-Frequency Continuous-Time filters in Digitlal CMOS Technology. *IEEE J. Solid-State Circuits*, 35(4):503–511, April 2000.

[47] M. H. Perrott. CppSim System Simulator. http://www.cppsim.com.

[48] M. H. Perrott. Fast and Accurate Behavioral Simulation of Fractional-N Synthesizers and other PLL/DLL Circuits. In *Design Automation Conference (DAC)*, 2002.

[49] R. Schoofs, M. Steyaert, and W. Sansen. A 1 GHz Continuous-Time Sigma-Delta A/D Converter in 90 nm Standard CMOS. In *IEEE MTTT-S Tech. Dig.*, 2005.

[50] R. Schoofs, M. Steyaert, and W. Sansen. A Design-Optimized Continuous-Time Delta-Sigma ADC for WLAN Applications. *IEEE Trans. Circuits Syst. I, Reg. Papers*, 54(1):209–217, January 2007.

[51] R. Schreier. Delta Sigma Toolbox. http://www.mathworks.com/.

[52] R. Schreier, N. Abaskharoun, H. Shibata, I. Mehr, S. Rose, and D. Paterson. A 375mW Quadrature Bandpass $\Delta\Sigma$ ADC with 90dB DR and 8.5MHz BW at 44MHz. In *IEEE ISSCC Dig. Tech. Papers*, 2006.

[53] Y. Shimizu, S. Murayama, K. Kudoh, and H. Yatsuda. A Split-Load Interpolation-Amplifier-Array 300MS/s 8b Subranging ADC in 90nm CMOS. In *IEEE ISSCC Dig. Tech. Papers*, 2008.

[54] Y. Shu, B. Song, and K. Bacrania. A 65nm CMOS CT $\Delta\Sigma$ Moudlator with 81dB DR and 8MHz BW Auto-Tuned by Pulse Injection. In *IEEE ISSCC Dig. Tech. Papers*, 2008.

[55] M. Z. Straayer and M. H. Perrott. A 12-bit 10-MHz Bandwidth, Continuous-Time Sigma-Delta ADC With a 5-bit, 950 MS/S VCO-based Quantizer. *IEEE J. Solid-State Circuits*, 43(4):805–814, April 2008.

[56] T. Toifl, C. Menolfi, P. Buchmann, M. Kossel, T. Morf, R. Reutemann, M. Ruegg, M. Schmatz, and J. Weiss. A 0.94-ps-RMS-jitter 0.016-mm^2 2.5-GHz multiphase generator PLL with 360 degree digitally programmable phase shift for 10 Gb/s serial links. *IEEE J. Solid-State Circuits*, 40(12):2700–2712, December 2005.

[57] Y. Tsividis. Continuous-Time Filters in Telecommunications Chips. *IEEE Communications Magazine*, pages 132–137, April 2001.

[58] Author(s) Unknown. Demystifying Sigma Delta ADCs. http://www.maxim-ic.com/.

[59] R. Veldhoven, R. Rutten, and L. Breems. An Inverter-Based Hybrid $\Sigma\Delta$ Modulator. In *IEEE ISSCC Dig. Tech. Papers*, 2008.

[60] D. Weber, W. Si, S. Abdollahi-Alibeik, M. Lee, R. Chang, H. Dogan, S. Luschas, and P. Husted. A Single-Chip CMOS Radio SoC for v2.1 bluetooth Applications. In *IEEE ISSCC Dig. Tech. Papers*, 2008.

[61] N. Yaghiniand and D. Johns. A 43mW CT Complex $\Delta\Sigma$ ADC With 23 MHz of Signal Bandwidth and 68.8 dB SNDR. In *IEEE ISSCC Dig. Tech. Papers*, 2005.

[62] H. Yamazaki, K. Oishi, and K. Gotoh. An Accurate Center-Frequency Tuning Scheme for 450-kHz CMOS $G_m - C$ Bandpass Filters. *IEEE J. Solid-State Circuits*, 34(12):1691–1697, December 1999.

[63] S. Yan. Baseband Continuous-Time Sigma-Delta Analog-to-Digital Conversion for ADSL Applications. Ph.D. Thesis.

[64] S. Yan and E. Sanchez-Sinencio. A Continuous-Time Modulator With 88-dB Dynamic Range and 1.1-MHz Signal Bandwidth. *IEEE J. Solid-State Circuits*, 39(1):75–86, January 2004.

[65] W. Yang, W. Schofield, H. Shibata, S. Korrapati, A. Shaikh, N. Abaskharoun, and D. Ribner. A 100mW 10 MHz-BW CT $\Delta\Sigma$ Modulator with 87dB DR and 91dBc IMD. In *IEEE ISSCC Dig. Tech. Papers*, 2008.

[66] A. Yoshizawa and Y. Tsividis. Anti-Blocker Design Techniques for MOSFET-C Filters for Direct Conversion Receivers. *IEEE J. Solid-State Circuits*, 37(3):357–364, March 2002.

[67] J.-R. Yuan, I. Karlsson, and C. Svensson. A True Single-Phase-Clock Dynamic CMOS Circuit Technique. *IEEE J. of Solid-State Circuits*, 22(5):899–901, October 1987.